Dynamic Supply Noise Measurement Circuit Composed of Standard Cells Suitable for In-Site SoC Power Integrity Verification

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Abstract— **This paper presents an all digital measurement circuit called "gated oscillator" for capturing waveforms of dynamic power supply noise. The gated oscillator is constructed with standard cells, and thus can be easily embedded in SoCs for design verification. The performance of the gated oscillator is verified with fabricated test chips in a 90nm process.**

I. Introduction

Power supply noise has become a serious problem in recent processes, and many circuits have been proposed for measurement of power supply noise [1]–[7]. However, most of existing measurement circuits require analog circuitry, and need dedicated analog power and bias lines. The additional area and routing costs restrict the number of measurement circuits integrated in a DUT and their placable positions.

In this paper, we present an all digital measurement circuit for dynamic noise waveform. Features of our circuit are: 1) including only digital standard cells, 2) no need for dedicated analog power supply and reference voltage, 3) small circuit area, and 4) operation with any external clock.

Our measurement circuit is easily embedded for SoC power integrity verification because it can be built only with standard cells. Its layout design is compatible with common cell-base design and the size and shape are flexible. Our measurement circuit does not need analog design techniques, and circuit and physical design is very easy.

II. Measurement circuit structure

A. Gated oscillator

Figure 1 shows the measurement circuit named "gated oscillator" for dynamic power supply noise measurement. The gated oscillator consists of only digital circuit components; inverters, a NAND gate, and transmission gates.

The operation of the gated oscillator is explained using Fig. 2. The gated oscillator operates only while 'enable'=1, and the oscillating signal is stopped by the transmission gates when 'enable'=0. Suppose a repetitive power supply noise waveform in Fig. 2. The cycle count of the oscillator depends on only the power supply voltage while enabled. The supply waveform while 'enable'=1 is sampled, and the operation of the gated oscillator is hold while 'enable'=0.

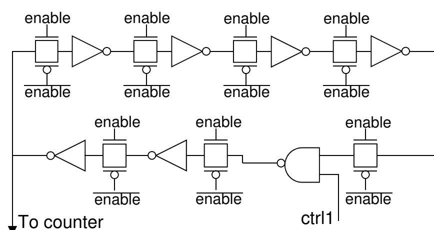

Fig. 1. Gated oscillator.

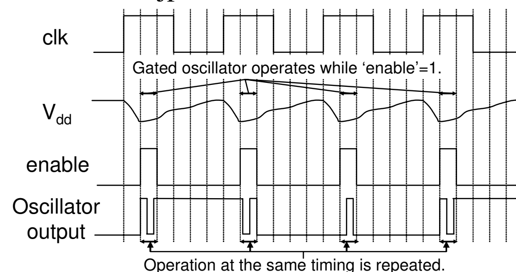

Fig. 2. Operation of the gated oscillator.

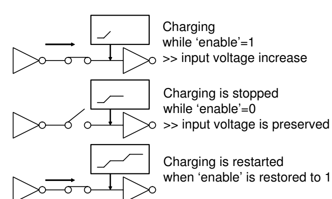

Fig. 3. Intermediate voltage preservation of gated oscillator.

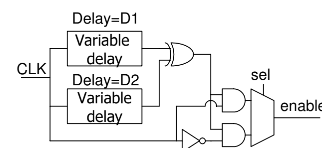

Fig. 4. Circuit for 'enable' signal generation.

Sufficient toggle count by repetitive operation is required for fine voltage resolution. The analog voltage of the power supply is translated into the toggle count. Therefore, the gated oscillator can be regarded as a sample and hold circuit with an A/D converter.

We also need to measure the cycle count beforehand varying supply voltage for making a calibration table of voltage vs. cycle count. When measuring an actual noise, the voltage at every timing is computed from the measured cycle count with the prepared calibration table. We then construct the dynamic power supply noise. The calibration for each die eliminates process variation effect.

An important metric of the measurement circuit is the voltage resolution. In the gated oscillator, the number of transmitting gate while 'enable'=1 is changed by the supply voltage. In addition, the gated oscillator can preserve the intermediate voltage of the transition at the timing when the oscillation is stopped (Fig. 3). When 'enable' is set from 1 to 0 while the inverter input is changing from 0 to 1 or 1 to 0, the input voltage is preserved at an intermediate level, whereas rigidly speaking, charge injection through the transmission gate slightly changes the voltage. After 'enable' is restored to 1, the transition restarts from the preserved intermediate level. This intermediate voltage preservation holds the ring oscillator state continuously, which improves the voltage resolution.

B. Implementation of measurement circuit

The circuits for 'enable' signal generation is needed for the gated oscillator. We designed an 'enable' signal generator in

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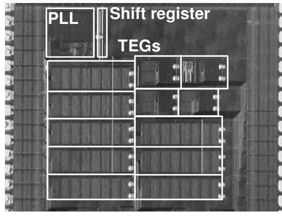

Fig. 5. Micrograph of the test chip.

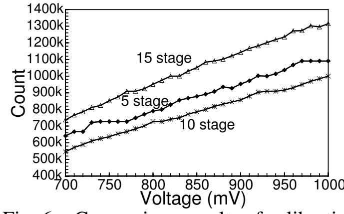

Fig. 6. Comparison results of calibration results. Timing widths of 'enable' pulse are set to 5, 10, 15-stage buffer delay.

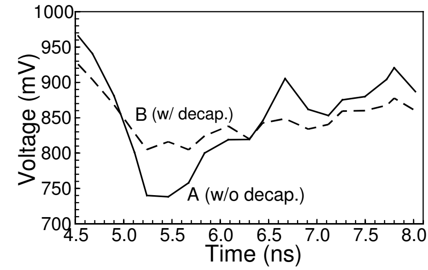

Fig. 7. Measurement results of noise waveform w/ and w/o decap.

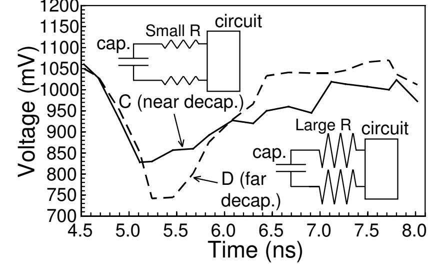

Fig. 8. Measurement results with near and far decap.

Fig. 4 that consists of VDC(Variable Delay Circuit), XOR, AND gates, and a selector. Note that other timing generators can be also used for measurement. This generator varies the pulse width and timing of 'enable' signal by controlling VDC. The generated pulse width is $|D1 - D2|$, where $D1$, $D2$ are the delays of VDC. The pulse timing of 'enable' from 'CLK' edge is $\min(D1, D2)$. The reference edge of 'CLK' is chosen from rise and fall transition by 'sel' signal. In this work, we adopted VDC which consists of buffers and selectors. $D1$ and $D2$ vary from 0- to 255-stage buffer delay. Power supply of the generator is separated from DUT to provide precise timing.

We fabricated a test chip in a 90nm CMOS process whose nominal supply voltage is 1.0V. Figure 5 is the micrograph of the test chip. The test chip also includes PLL and a shift register. The shift register is written and read by external signals. The shift register stores control signals of measurement circuits and PLL. A part of the shift register also operates as a counter, and counts the toggle of the gated oscillator.

The layout size of the gated oscillator is $11.76\mu\text{m}\times 15.12\mu\text{m}$, and comparable to the other analog measurement circuits [4], [6]. In this work, 4X inverters and transmission gates are used to suppress random process variation. Otherwise, the layout size can be shrunk to roughly one-fourth.

III. On-silicon evaluation

We evaluate measurement precision and reproducibility of the gated oscillator on silicon. Fabricated chips were mounted on QFP package and are controlled with external signals.

Fig. 6 shows the voltage resolution and sampling performance of the gated oscillator. The number of given 'enable' pulse whose width is 5-stage buffer delay is 4 million, and in other cases 2 million. The voltage resolutions of 10- and 15-stage pulse width are better and their resolutions are roughly 10mV. The buffer delay is measured using ring oscillator embedded in 'enable' timing generation circuit, and the 10-stage buffer delay is about 300ps-450ps. In summary, the implemented circuit performs 3G sample per second with 10mV voltage resolution.

Fig. 7 is the measurement result of dynamic noise waveform with the gated oscillator. The noise sources of Line A and B are 512 12-stage NAND gates, and the enough decoupling capacitance is attached to the noise source of Line B. The mitigation of power supply drop due to the decap is clearly observed. Fig. 8 compares the two decap condition, whose difference is the resistance between noise source and decap. The measurement results confirms that nearby decap (Line C) is more effective than far capacitance (Line D). In this way, the gated oscillator can be applied for evaluating the quality of power distribution network. A noise waveform was measured for 1000 times to evaluate the reproductivity. The maximum standard deviation at 10 timing points is 0.98%, and the gated oscillator has fine reproductivity.

IV. Conclusion

The gated oscillator which consists of standard cells and captures dynamic supply noise waveform is proposed. The gated oscillator does not require dedicated power and bias lines. The voltage resolution of 10mV and measurement reproductivity $\sigma = 0.98\%$ were confirmed, and the proposed circuit observed dynamic noise waveform successfully on the test chip fabricated in a 90nm CMOS process.

Acknowledgment

The VLSI chip in this study has been fabricated through the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo, with the collaboration by STARC, Fujitsu Limited, Matsushita Electric Industrial Company Limited., NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporation. This study was partly supported from NEDO of Japan.

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