PAPER Special Section on VLSI Design and CAD Algorithms

Timing Analysis Considering Spatial Power/Ground Level Variation

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SUMMARY Spatial power/ground level variation causes power/ground level mismatch between driver and receiver, and the mismatch affects gate propagation delay. This paper proposes a timing analysis method based on a concept called "PG level equalization" which is compatible with conventional STA frameworks. We equalize the power/ground levels of driver and receiver. The charging/discharging current variation due to equalization is compensated by replacing output load. We present an implementation method of the proposed concept, and demonstrate that the proposed method works well for multiple-input gates and RC load model.

key words: *timing analysis, power supply noise, gate delay model, power/ground level variation*

1. Introduction

As power/ground noise has been aggravated, power/ground-noise-aware timing analysis is eagerly demanded. This problem can be classified into two issues; how to find the worst-case noise pattern [1], and how to compute propagation delay [2]–[6]. Conventionally, power-noise-aware timing analysis assumes that ground levels of a driver and its receiver are the same. This is true when the driver and the receiver are placed in the neighborhood. However, if they are placed away, ground level as well as power level becomes different because power/ground noise varies spatially.

Some recent works on propagation delay computation focus on the mismatch problem of power/ground level between driver and receiver [3]–[6]. One of the difficulties to solve the mismatch problem is large number of parameters that affect propagation delay. The power and ground levels of the driver and the receiver as well as output capacitance and input transition time are parameters. Moreover voltage levels of other stable inputs change propagation delay, and they are also parameters. In the case of a 3-input gate, the number of parameters becomes seven, where 3 (#inputs) $\times$ 2 (power/ground levels of inputs) + 1 (power level of the gate itself) assuming the ground level of the gate is a reference voltage level. Thus, it is difficult to construct a gate delay model using look-up tables due to huge characterization cost. References [3]–[5] propose gate delay models that are derived by first-order expansion using the sensitivity. However, Refs. [3], [4], [6] focus on inverter and buffer, and they do not consider multiple-input gates explicitly. Reference [5] mentions multiple-input gates, but implementation issues are not explained clearly. Also in VDSM technologies, RC load, such as CRC π load model, must be handled to consider interconnect resistance. Reference [3] discusses RC load, but it is not clear whether Refs. [4]–[6] can cope with RC load in gate-level static timing analysis.

This paper discusses timing analysis that considers spatial power/ground level variation when power/ground levels of each gate are given. We propose a concept to solve the mismatch problem due to spatial PG noise. The proposed concept equalizes PG levels of driver and receiver. The charging/discharging current variation caused by the equalization is compensated by adjusting the output load. An implementation method is also presented. Thanks to the proposed concept, we can perform timing analysis with a compact gate delay model. We experimentally verify that the proposed concept works well for various gates, loads and paths.

This paper is organized as follows. We explain the motivation and the target problem of this paper in Sect. 2. We then propose a concept of "PG level equalization" to capture PG level variation with a compact gate delay model. An implementation method is also described in Sect. 3. Section 4 demonstrates experimental results of path delay calculation. Section 5 concludes the discussion.

2. Motivation and Target Problem

This section describes the motivation of this work, and clarifies the target problem of this paper.

2.1 Problem of Temporal and Spatial Power/Ground Variation on Timing

There are two obstacles to perform power/ground noise aware timing analysis when noise waveforms are given; temporal variation and spatial variation of PG noise. We here discuss both problems, and we explain our goal of this paper.

We first discuss temporal variation of PG noise. PG noise has various amplitude, shape and time constant. When the noise time constant is comparable with gate transition speed, gate delay calculation becomes complicated and rigid analysis for numerous noise shapes is difficult due to com-

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putational cost. Reference [7] shows a possible solution of this problem that replaces temporally-variant noise waveform with a constant voltage level.

The second problem is spatial PG variation, and it is the main topic of this paper. Gates in a path are not necessarily placed in the neighborhood, for example, repeaters are necessarily placed with a certain distance. Therefore in a general condition, the PG level of each gate is different. Figure 1 shows an example of input and output waveforms. The maximum and minimum voltage levels of input waveform (V_{dd1}, V_{ss1}) are the PG levels of the driver gate, and they are different from the PG levels of the receiver gate (V_{dd2}, V_{ss2}). The charging/discharging current strongly depends on the input voltage level, which results in gate delay variation. Also except inverter and buffer, there are multiple inputs. In this situation, gate delay t_d and output transition time t_{ro} are expressed as follows.

$$t_d = f_1(t_{ri}, C_o, V_{dd1}, V_{ss1}, V_{dd2}, V_{ss2}, V_{in1}, \ldots, V_{in(n-1)}),$$
$$t_{ro} = g_1(t_{ri}, C_o, V_{dd1}, V_{ss1}, V_{dd2}, V_{ss2}, V_{in1}, \ldots, V_{in(n-1)}),$$

where t_{ri} is the input transition time, C_o is the output load capacitance, n is the number of inputs, and V_{ink} is the k-th stable input. We can fix one of the voltage levels without losing generality. When we set V_{ss2} to zero, the equations are rewritten as follows.

$$t_d = f_2(t_{ri}, C_o, V_{dd1}, V_{ss1}, V_{dd2}, V_{in1}, \ldots, V_{in(n-1)}), \quad (1)$$
$$t_{ro} = g_2(t_{ri}, C_o, V_{dd1}, V_{ss1}, V_{dd2}, V_{in1}, \ldots, V_{in(n-1)}). \quad (2)$$

When the functions of f_2 and g_2 of a 3-input gate are expressed by a lookup table model, we have to generate nine dimensional tables and the characterization cost by circuit simulation is prohibitively large.

2.2 Target Problem

This paper focuses on spatial PG level variation. We propose a gate delay calculation method using a compact gate delay model that has just three parameters: output loading, input transition time and supply voltage. Our approach is compatible with the conventional static timing analysis, and the characterization cost does not increase drastically. We assume that the PG voltage levels of each gate are given throughout this paper.

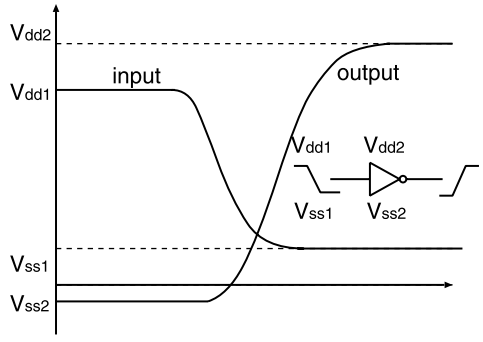

Fig. 1 Input and output waveforms with spatial PG level variation.

3. Gate Delay Calculation Considering Spatial P/G Level Variation

This section presents a concept to cope with spatial PG level variation. We then show an implementation method of the proposed concept.

3.1 Proposed Concept of "PG Level Equalization"

The PG level variation changes charging/discharging current, which results in gate delay variation. Basically, gate delay is the time required to charge/discharge output load. Therefore, even if the current increases/decreases by PG level variation, we can keep the gate delay unchanged by increasing/decreasing the output load in the same ratio.

Figure 2 shows the proposed concept. We set the PG levels of the input waveform to V_{dd2} and V_{ss2}. The equalization of the PG levels is compensated by the adjustment of the output load C. We calculate the equivalent output load C_{eq}, and replace C_{actual} with C_{eq}. The gate delay becomes unchanged when the following relation is satisfied.

$$I_{actual} : I_{eq} = C_{actual} : C_{eq}, \quad (3)$$

where I_{actual} is the actual charging/discharging current, and I_{eq} is the charging/discharging current after PG level equalization. Then C_{eq} is expressed by

$$C_{eq} = \frac{I_{eq}}{I_{actual}} \cdot C_{actual}. \quad (4)$$

An important point here is that charging/discharging current is not constant during the transition. Actually, the transient charging/discharging current depends on output load and input transition time as well as power/ground voltages. On the other hand, it is difficult to derive the transient current in a computationally efficient way. We thus in this paper use representative current values for I_{actual} and I_{eq} in Eq. (4). The detail will be explained first with a fast input case in this subsection followed by a slow input case in Sect. 3.4.

Thanks to PG level equalization, the gate delay and transition time calculation is simplified as follows.

$$t_d = f_3(t_{ri}, C_o, V_d), \quad (5)$$
$$t_{ro} = g_3(t_{ri}, C_o, V_d), \quad (6)$$

where $V_d (= V_{dd2} - V_{ss2})$ is the receiver supply voltage.

There are several proposals for gate delay calculation in

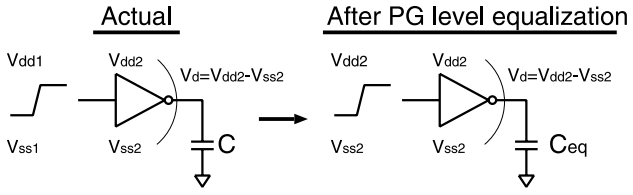

Fig. 2 Proposed concept called "PG level equalization."

Eqs. (5) and (6). For example, Ref. [2] proposes an interpolation method in voltage using usual two dimensional tables. A vendor proposes a scalable polynomial delay model that includes supply voltage and temperature as well as output load and input transition time as variables. We here think that the formulation of gate delay in Eqs. (5) and (6) is acceptable in LSI design.

The proposed concept of "PG level equalization" is quite simple and the necessity is the calculation of Eq. (4) only. The other part of timing analysis is basically the same with the conventional method, and thus the proposed method is compatible with the conventional STA framework. If we have STA tools that can handle Eqs. (5) and (6), we can perform static timing analysis considering spatial PG level equalization just with the pre-processing of Eq. (4). We think that the gate delay model of Eqs. (5) and (6) is or will be popular, and the proposed concept can co-work with current and future STA tools.

We here show a typical way that the proposed technique is used with conventional STA.

Step 1 Estimate power/ground levels of each cell.
Step 2 Replace output load of each cell by using Eq. (4).
Step 3 Perform STA.

Replacement of output load in Step 2, for example, can be realized by adjusting wire capacitance. In Step 2, we may have a limitation. When STA accepts two load capacitance values for rise and fall transitions, we can compute C_{eq} for rise and fall transitions separately. When STA uses a single capacitance value, we might choose the larger value for conservative timing analysis. In the case of multiple input cells, C_{eq} is different depending on the transitioning input pins. In this case, we should choose C_{eq} corresponding to the input pin whose latest arrival time is the largest. Since this choice requires at least two iterative execution of STA, another policy, such as the maximum capacitance selection, might be used conservatively. Though there may exist a limitation, we can perform timing analysis considering PG level variation with current STA tools. Another way to co-work with conventional STA could be as follows.

Step 2' Compute gate delay with Eq. (4) and generate SDF (Standard Delay Format) file.
Step 3' Perform STA with SDF file.

In this approach, the limitations described above can be solved.

Figure 3 shows input and output waveforms with and without PG level equalization. In this paper, we assume a 0.18 μm CMOS process in the experiments. The PG levels of the actual input waveform are different, and we equalize the PG levels of the input waveform to those of the receiver. PG level equalization without replacing output load C_{actual} gives the waveform that is far from the actual waveform, because the discharging current becomes different by PG level equalization. We then replace C_{actual} with C_{eq}. I_{actual} is calculated by DC analysis in the case that $V_{in} = V_{dd1}$ and $V_o = V_{dd2}$ in Fig. 4. I_{eq} is calculated in the case that

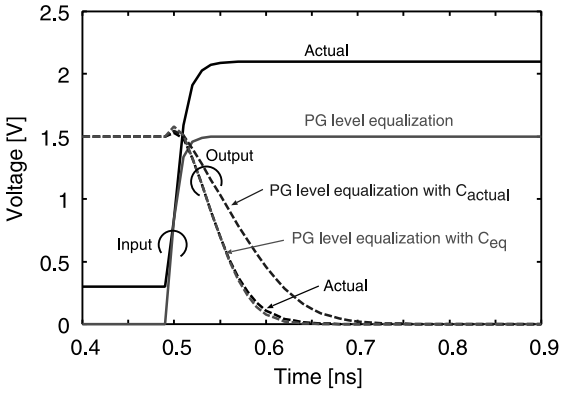

Fig. 3 Input and output waveforms with PG level equalization.

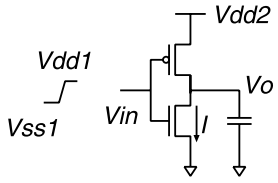

Fig. 4 Current flow.

$V_{in} = V_o = V_{dd2}$.

These current values of I_{actual} and I_{eq} are reasonable representative currents, because the input transition is fast, and the NMOS works like a constant current source in a saturation region. Slow input transitions will be discussed in Sect. 3.4.

Thanks to the replacement of output loading, the output waveform with PG level equalization gets close to the actual output waveform. We can see that the basic idea of PG level equalization works well. Hereafter we explain practical implementation issues of the proposed concept.

3.2 Delay and Transition Time Definition

We here explain the definitions of delay and transition times. The definitions are important to calculate path delay, because inconsistent definitions degrade accuracy or rather disable timing propagation. Figure 5 explains the definitions in this paper. Delay t_d is the time interval between the input crossing timing of $(V_{dd1} + V_{ss1})/2$ and the output crossing timing of $(V_{dd2} + V_{ss2})/2$. This definition is efficient, because the arrival time when the input goes across $(V_{dd1} + V_{ss1})/2$ is calculated before.

In this paper, we use a waveform expression composed of a linear (0–60%) and an exponential functions (60%–) with a single parameter of T_{12} [10], because ramp waveforms are not suitable for accurate analysis [12]. The parameter of T_{12} is originally defined as the crossing time difference between $0.4V_{dd}$ and $0.6V_{dd}$. The transition times t_{ri} and t_{ro} are calculated at the crossing timings of 40% and 60% of each voltage swing as shown in the right figure (Fig. 5). Please note that the proposed concept is independent of the definitions described here, although some modifications in

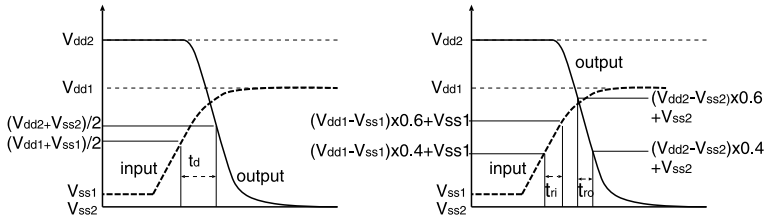

Fig. 5 Definitions of delay and transition time.

implementation may be necessary.

3.3 Current Calculation

The key of the proposed concept is the calculation of Eq. (4), and there are two problems; 1) how we should efficiently calculate current I_{actual} and I_{eq} even for multiple-input gates, and 2) of what timing we should calculate current I_{actual} and I_{eq} in the case that the input transition is slower than the output transition. Solutions of these two problems enable us to perform timing analysis considering spatial PG level variation. This section discusses the first problem, and the second one will be discussed in the next section.

The simplest way to calculate the current in Eq. (4) is to use analytic expressions proposed so far, for example, alpha-power model [8] and equivalent inverter transformation [9]. Alpha-power model [8] is very effective for inverter, but it does not cope with other gates directly, eg. NAND and NOR. Reference [9] proposes a method to replace series-connected MOSFETs with an equivalent MOSFET. This method assumes that the transition swing is between V_{DD} and V_{SS}, and other stable inputs are V_{DD} or V_{SS}. However in order to capture spatial PG level fluctuation, we need a current model that has all input voltage levels and its supply voltage levels as variables. The extension of Ref. [9] is not straightforward, and we hence adopt response surface method [11] as an alternative. We can use other methods if their accuracy is sufficient.

Figure 6 shows the structure of a 3-input NAND gate. Let us examine a fall transition case that the series-connected NMOSFETs discharge the output load as an example. The current I that flows through the series-connected NMOSFETs depends on four parameters, $V_g^{(1)}, V_g^{(2)}, V_g^{(3)}$ and V_o, when we fix the voltage of V_{SS} as a reference level. The response surface method is performed as follows. We first execute DC analysis varying $V_g^{(1)}, V_g^{(2)}, V_g^{(3)}$ and V_o. We next construct a polynomial response surface function $I_{RSM}(V_g^{(1)}, V_g^{(2)}, V_g^{(3)}, V_o)$, where the order of the polynomial function is decided such that necessary and sufficient accuracy can be obtained.

Figure 7 shows the accuracy of the current estimation by the derived response surface function. In this case, we vary V_o from 1.5 to 2.1 V and $V_g^{(1-3)}$ from 1.2 to 2.0 V. The order of the polynomial response surface function is three. The current I is accurately estimated with $R^2 = 0.9989$. The response surface method is a generic method, and we can apply it to various logic gates. The accuracy can be controlled by the order of polynomials.

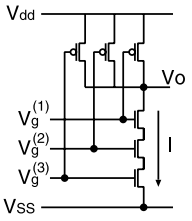

Fig. 6 3-input NAND gate.

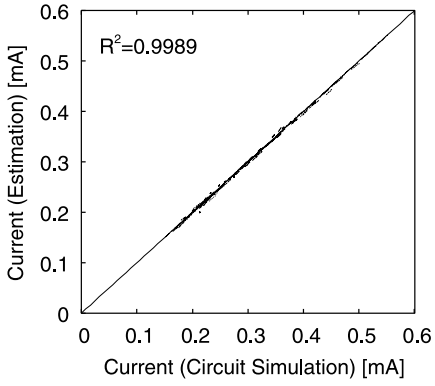

Fig. 7 Current estimation accuracy (3-input NAND).

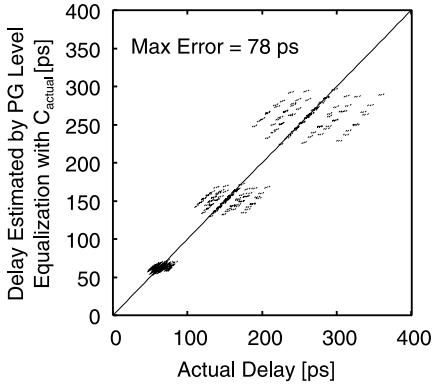

Fig. 8 Delay estimation accuracy of PG level equalization without Eq. (4). (3-input NAND, fall transition).

Figure 8 shows the error when we perform PG level equalization without the replacement of the output load. We vary V_{dd} and $V_g^{(2-3)}$ from 1.6 to 2.0 V. We use rise input waveforms whose minimum level is −0.2 to 0.2 V and whose maximum level is 1.6 to 2.0 V. The actual output load

is varied from 10 to 100 fF, and the input transition time is 30 ps. The absolute and relative maximum errors are 78 ps and 32%, respectively. On the other hand, Fig. 9 with the replacement of Eq. (4) indicates more accurate estimation results. The maximum errors are reduced to 14 ps and 13%. The delay variation due to PG level fluctuation is well captured by the proposed concept. We confirm that other transition direction and other type of gates, such as INV, NOR, AOI and OAI, can be treated similarly, and we verify the accuracy.

3.4 Slope Consideration

We will explain the second problem using an example of an inverter. In the experimental results shown in the previous section, when the input transition time is quite small compared with the output transition time, the representative condition for calculating I_{actual} and I_{eq} is easily decided. It is because the output is transitioning mainly after the input transition finishes. In this case, we can focus on the behavior after the input transition finishes.

Let us examine another case that the transition time of the input waveform is larger than the output transition time. Figure 10 shows an example. We give a rise transition to an inverter.

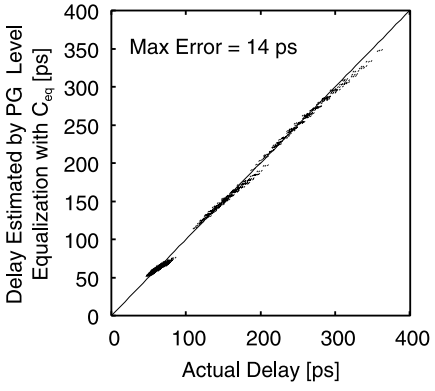

Fig. 9 Delay estimation accuracy of PG level equalization with Eq. (4). (3-input NAND, fall transition).

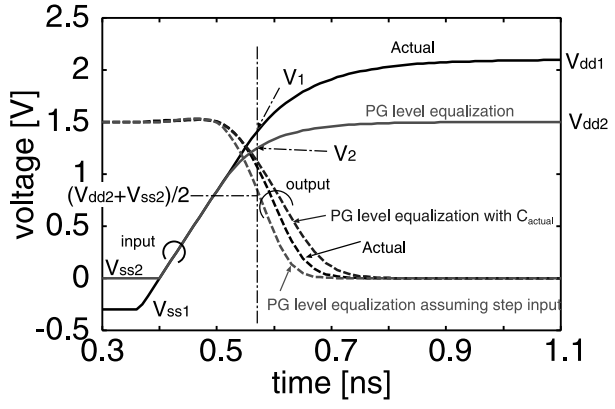

Fig. 10 Problem on long input transition time.

We equalize the input and output voltage levels, and generate the input waveform labeled "PG level equalization." In this process, we keep the following relation: $(V_{\text{dd1}} - V_{\text{ss1}})/T_{12\text{actual}} = (V_{\text{dd2}} - V_{\text{ss2}})/T_{12\text{eq}}$. This means that the slope is the same. We align the actual and the equalized waveform in time axis such that the linear parts of both the waveforms match as shown in Fig. 10. Figure 10 shows three output waveforms; the actual waveform and the waveforms calculated by PG level equalization with and without the replacement of the output loading. In this figure, the replacement assumes that the input transition is very fast, i.e. the current calculation in Eq. (4) uses V_{dd1} and V_{dd2} as the input voltage levels. We can see that the replacement of the output loading fails. This is because the output transition almost finishes before the input voltage gets close to V_{dd1} (V_{dd2}). The input voltage level that dominantly determines the output transition behavior is not V_{dd1} (V_{dd2}).

We intuitively think that the input voltage while the output is changing, especially before the output becomes $(V_{\text{dd2}} + V_{\text{ss2}})/2$, has a strong impact on the output behavior. We then choose a timing when the output crosses a voltage level V_{ref}, and use the currents at that timing as I_{actual} and I_{eq} in Eq. (4). In order to determine V_{ref}, we execute numerous experiments varying V_{ref} from $(V_{\text{dd2}} - V_{\text{ss2}}) \times 0.1 + V_{\text{ss2}}$ to $(V_{\text{dd2}} - V_{\text{ss2}}) \times 0.9 + V_{\text{ss2}}$ as well as the voltage level conditions and output load. We observe that the maximum error becomes the smallest when we set $V_{\text{ref}} = (V_{\text{dd2}} + V_{\text{ss2}})/2$. Another issue is how to calculate the output waveform to decide the crossing timing of V_{ref}. From experimental results, we decide to use the output waveform estimated by PG level equalization with C_{actual}, because we experimentally observe that even if the accurate output waveform would be obtained, the accuracy is almost the same. Figure 11 shows the output waveform calculated by the proposed concept with $V_{\text{ref}} = (V_{\text{dd2}} + V_{\text{ss2}})/2$. We can see that the output waveform derived by PG level equalization gets close to the actual output waveform.

We evaluate the accuracy in various conditions. We vary V_{dd2} from 1.6 to 2.0 V. We apply rise transitions whose minimum level is −0.2 to 0.2 V and whose maximum level

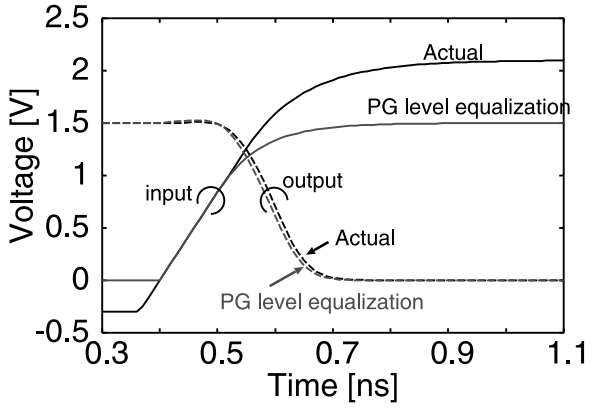

Fig. 11 Input and output waveforms by PG level equalization with slope consideration.

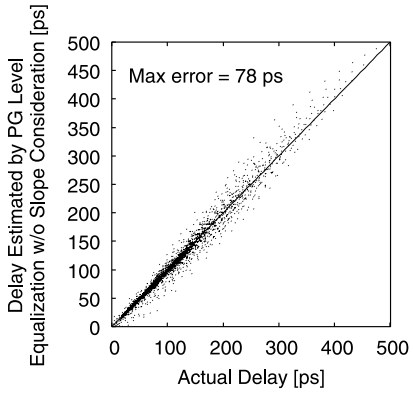

Fig. 12 Delay estimation accuracy of PG level equalization w/o slope consideration (INV, fall transition).

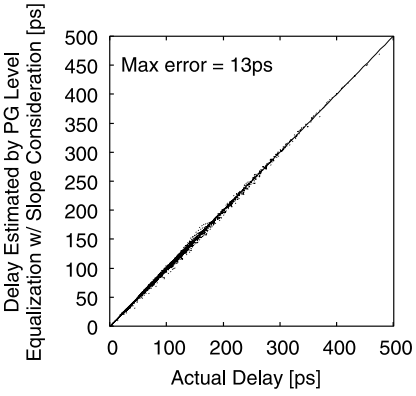

Fig. 13 Delay estimation accuracy of PG level equalization w/ slope consideration (INV, fall transition).

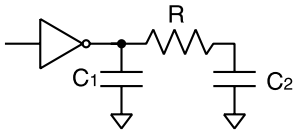

Fig. 14 CRC π model.

is 1.6 to 2.0 V. The actual output loading is varied from 10 to 100 fF, and T_{12} of the input transition is 5 ps to 200 ps, which roughly corresponds to 30 to 1,200 ps in 0–100% transition time. Figure 12 shows the error when assuming step input, and Fig. 13 indicates the accuracy when the slope of the input waveform is considered. Thanks to the consideration of the input slope, the maximum error is reduced from 78 ps to 13 ps.

3.5 Generic Output Load

In VDSM technologies, wire resistance affects propagation delay. The output load is once translated into a CRC π model (Fig. 14) [13], and the CRC π model is replaced with an effective capacitance [14] to obtain the gate output waveform.

We here show that the proposed concept can be applied consistently to generic output loading. Figure 15 shows the

Fig. 15 PG level equalization for generic load.

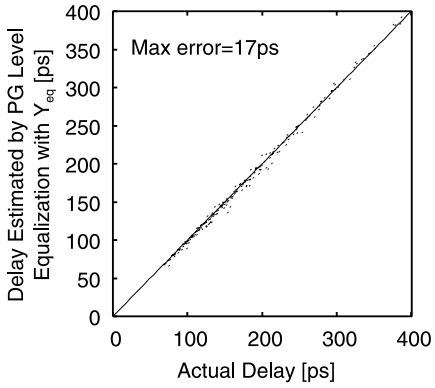

Fig. 16 Delay estimation accuracy for CRC π load model (4x INV, fall transition).

proposed concept for generic output loading, where Y_{actual} is the driving point admittance of the actual circuit, and Y_{eq} is the driving point admittance after PG level equalization. Similar to Sect. 3.1, Y_{eq} is calculated by

$$Y_{\text{eq}} = \frac{I_{\text{eq}}}{I_{\text{actual}}} \cdot Y_{\text{actual}}. \tag{7}$$

We can see that Eq. (4) is one of the special cases of Eq. (7). In the case of CRC π model, $C_{1\text{eq}}, C_{2\text{eq}}$ and R_{eq} can be simply expressed as follows.

$$\begin{aligned} C_{1\text{eq}} &= C_{1\text{actual}} \cdot I_{\text{eq}}/I_{\text{actual}} \\ C_{2\text{eq}} &= C_{2\text{actual}} \cdot I_{\text{eq}}/I_{\text{actual}} \\ R_{\text{eq}} &= R_{\text{actual}} \cdot I_{\text{actual}}/I_{\text{eq}} \end{aligned} \tag{8}$$

We evaluate the estimation accuracy. We generate CRC π load models of 1–2 mm long interconnect with 100 fF receiver input capacitance by Ref. [13]. The other evaluation conditions are the same with Sect. 3.4. Figure 16 shows the accuracy. The absolute and relative maximum errors are 17 ps and 6.2%, respectively. The proposed concept works well for CRC π load model. Subsequently the effective capacitance can be calculated by conventional methods such as Ref. [14].

We here summarize the proposed technique. Given the output load admittance and the power/ground levels, we replace the output load by using Eq. (7). I_{actual} and I_{eq} in Eq. (7) are the currents at the timing when the output crosses $(V_{\text{dd2}} + V_{\text{ss2}})/2$, as explained in Sect. 3.4. The values of I_{actual} and I_{eq} are computed with polynomial response surface functions characterized with DC analysis beforehand. After PG level equalization with the output load replacement, we can calculate gate delay considering PG level variation even with a conventional gate delay model.

As a special case, when the output load is CRC π model, Eq. (7) is transformed to Eq. (9). When the output load is capacitance, Eqs. (7) and (9) are simplified to Eq. (4).

3.6 Characterization Cost

We here briefly review the characterization cost. Suppose a 3-input gate, and compare seven-dimensional table model in Eqs. (1) and (2) with the proposed method. When we construct the model of Eqs. (1) and (2), we assume five sample points in output load and input transition time, and three sample points in voltage level. As for the proposed method, we assume five sample points in output and input transition time and three points in voltage level in Eqs. (5) and (6). When building the response surface function of current, we use five sample points for each voltage level. In summary, we have to execute 36,450 transient analysis for the seven-dimensional table model, whereas 1,250 DC analysis and 150 transient analysis for the proposed method. The computational times are 3,584 s and 15 s respectively. The proposed method is 240 times as efficient as the naive table look-up model in characterization cost.

4. Path Delay Calculation

We show the results of path delay calculation by the proposed concept. We evaluate the propagating waveform in the circuit of Fig. 17. The voltage levels of each gate and the capacitances are randomly varied, and the path delay is evaluated by a circuit simulator and by the proposed concept. The variation range is the same with Sect. 3.4. The total number of evaluation is 100. Figure 18 shows an example of propagating waveforms. The output waveform of each gate is shown, and the waveforms of the proposed method are close to the circuit simulation results. The average estimation error is 1.6% and the maximum error is 3.3%. The proposed concept with the implementation shown in this paper achieves accurate timing analysis.

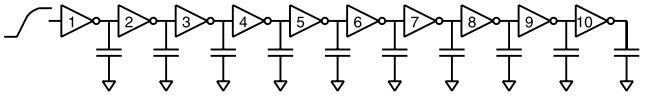

Fig. 17 Experimental circuit for path delay evaluation.

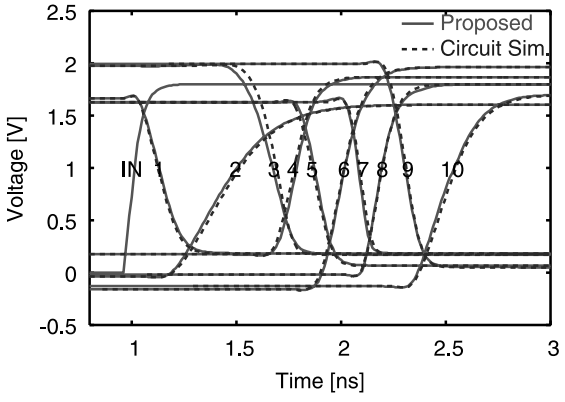

Fig. 18 An example of propagating waveforms.

5. Conclusion

This paper presents a concept of "PG level equalization" that aims to perform timing analysis considering spatial power/ground level variation. By equalizing power/ground levels of driver and receiver and compensating current change by output load replacement, we can consider spatial PG level variation with a common compact gate delay model that has three variables. We confirm that the error of each gate delay is below 20 ps in a 0.18 μm technology, and the maximum estimation error of path delay is 3.3%.

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