Analytical Eye-diagram Model for On-chip Distortionless Transmission Lines and Its Application to Design Space Exploration

Masanori Hashimoto*, Jangsombatsiri Siriporn* Akira Tsuchiya†, Haikun Zhu‡ and Chung-Kuan Cheng‡
*Osaka University, †Kyoto University, ‡University of California at San Diego
hasimoto@ist.osaka-u.ac.jp

***Abstract*— This paper proposes a closed-form eye-diagram model for on-chip distortionless transmission lines with intentionally inserted shunt conductance. We derive expressions of eye-opening both in voltage and time, by assuming a piece-wise linear waveform model. The model is experimentally verified. We also apply the proposed model to design trade-off analysis.**

I. Introduction

On-chip interconnection has become one of the problems preventing performance enhancement in advanced technologies. As one of promising solutions, high-speed signaling over on-chip transmission lines has been studied both in circuit and EDA communities [1]–[3]. In this scheme, performance of on-chip transmission lines is a primary concern. Reference [4] reports that, in the current technology, the interconnect performance is superior to that of transistors, and the signaling throughput is predicted to improve thanks to transistor performance enhancement in the future.

For further improvement of signaling throughput, intersymbol interference (ISI) is a critical obstacle. Due to frequency dependence of propagation characteristics, the pulse distorts. Pre-emphasis at a driver and equalization at a receiver are effective for suppressing ISI and widely used in chip-to-chip communication [5]. Recently, on-chip transmission line with less distortion has been also studied [6]–[9]. References [6], [7] demonstrate that nonlinear transmission lines with active variable capacitance enable signaling with less dispersion and loss.

References [8], [9] proposed on-chip transmission lines with shunt resistance intentionally inserted for suppressing distortion. Due to S_iO_2 characteristics, the conductance of on-chip transmission lines is quite small and usually negligible. According to transmission line theory, when a condition $RC = GL$ holds, attenuation and phase velocity become constant over all frequency range, and waveform distortion disappears. References [8], [9] intentionally insert shunt conductance, assuming shunt conductance is implemented by poly silicon. ISI reduction by shunt resistance is clearly demonstrated [8], [9], though the distortionless condition can not be satisfied in all frequency, because R and L are frequency dependent due to skin and proximity effects. In reality, as the shunt conductance approaches to to $G = RC/L$, the frequency dependence of attenuation and phase velocity are suppressed gradually. On the other hand, the inserted shunt conductance increases the attenuation, and hence the suppression of distortion and the signal magnitude are in a trade-off relationship. When ISI is severe, shunt conductance improves the eye-diagram. On the other hand, when ISI and signal magnitude are small, shunt conductance should not be inserted. Therefore, optimal shunt resistance value to maximize opening in eye-diagram depends on interconnect length and signaling throughput. In addition, resistive termination is widely used to reduce ISI for high-speed signaling. It is not clear how to determine termination resistance for shunt-inserted transmission lines.

This paper proposes an analytic eye-diagram model for shunt-inserted distortionless transmission lines. The proposed model can derive the optimal shunt resistance and termination resistance without time-consuming circuit simulation. We extend the model of voltage eye-opening [10] for the shunt-inserted transmission lines. We also derive a closed-form expression of eye-opening in time. We demonstrate that the optimal shunt resistance and termination resistance change drastically depending on interconnect length and signaling throughput. Our analytical model is useful for rough performance estimation and design space exploration early in a design stage.

This paper is organized as follows. Section II explains the proposed analytic model, and verifies the estimation accuracy. Section III shows a trade-off analysis in shunt and termination resistances by using the proposed model. Section IV concludes the paper.

II. Analytical Eye-diagram Model

This section describes an analytical eye-diagram model for shunt-inserted transmission lines, and experimentally validate the model.

A. Piecewise-Linear waveform model

We here introduce a piecewise-linear (PWL) waveform model proposed in Ref. [10]. The circuit model of terminated transmission-lines is shown in Fig. 1. The resistance, inductance, conductance and capacitance per unit length are R, L, G and C respectively. The impedance Z_0 is the characteristic impedance of transmission-line. At the receiver side, the interconnect is terminated by the resister and the resistance value is R_t. At the driver side, we assume that the driver of the interconnect achieves impedance matching. In other words, the output impedance of the driver is equal to the characteristic impedance Z_0. For simplicity, the supply voltage V_{dd} is 1V. This assumption does not lose the generality because the circuit model in Fig. 1 is a linear circuit.

We model the waveform at the receiver side of transmission-lines by the PWL waveform model shown in Fig. 2. Figure 2

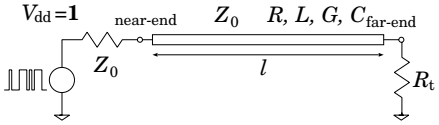

Fig. 1. Circuit model of a transmission-line with resistive termination.

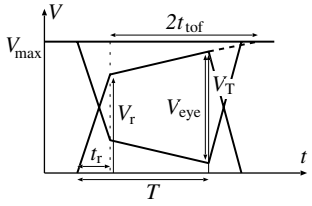

Fig. 2. PWL waveform model.

is the eye-diagram by two isolated pulse ($0\cdots010\cdots0$ and $1\cdots101\cdots1$). When noise is small, these isolated pulses determine the eye-opening in voltage. In Fig. 2, time t_r is the transition time of input pulse and period T is the minimum width of input pulse. Voltage V_r is rise voltage that is determined from the attenuation and the termination of the interconnect. The voltage V_T is the voltage at the time T. The voltage V_T decides the maximum eye-opening voltage. The voltage V_{max} is the voltage level when the continuous "1" is input to the interconnect. The voltage V_{max} is determined by the resistance of the terminator, the resistance and conductance of the interconnect and the output resistance of the driver. The time t_{tof} is the signal time-of-flight that is determined by the interconnect length and the velocity of electromagnetic wave. From Ref. [11], [12], when the driver achieves impedance matching, the voltage at the receiver side roughly reaches V_{max} when the time $2t_{tof}$ passed after the rising. By using this characteristic, we can derive the voltage V_T.

From the PWL waveform model in Fig. 2, the maximum eye-opening voltage V_{eye} is expressed as

$$V_{eye} = \begin{cases} \max\{V_{max} - 2\,(V_{max} - V_T)\,, 0\} & (T - t_r < 2t_{tof}) \\ V_{max} & (T - t_r > 2t_{tof}) \end{cases}. \quad (1)$$

The resistive termination changes V_T and V_{max}. The shunt conductance also varies V_T and V_{max}. Therefore, designers can tune the eye-opening by resistive termination and shunt resistance.

B. Derivation of eye-opening in voltage

The amplitude of the pulse injected to the interconnect is expressed as $V_{near} = V_{dd}/2 = 1/2$ because this paper assumes that the driver output impedance is equal to the characteristic impedance Z_0. The pulse attenuates as propagating on the lossy transmission-line. The amplitude of the attenuated pulse at the receiver side is expressed as

$$V_{far} = V_{near} \exp(-\alpha l) = n/2, \quad (2)$$

where the parameter α is the attenuation constant of the interconnect and the parameter n is the attenuation parameter defined as $n = \exp(-\alpha l)$. As the attenuation becomes weaker, the parameter n becomes larger. If the line is lossless, the parameter n is equal to 1. In RLGC transmission lines, α is expressed as follows.

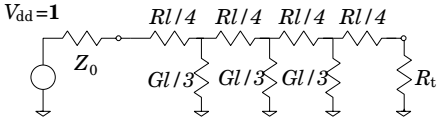

Fig. 3. Circuit model for V_{max} derivation.

$$\alpha = \mathrm{Re}\left[\sqrt{(R + j\omega L)(G + j\omega C)}\right], \quad (3)$$

$$= \sqrt{\frac{-\omega^2 CL + \omega C\sqrt{\omega^2 L^2 + R^2}}{2}}. \quad (4)$$

The reflection coefficient Γ at the receiver side is expressed as $(R_t - Z_0)/(R_t + Z_0)$. Therefore, the rise voltage V_r is calculated by

$$V_r = V_{far} \times (1 + \Gamma) = \frac{n}{2}\frac{2Z_n}{Z_n + 1}, \quad (5)$$

where the parameter Z_n is the normalized impedance defined as $Z_n = R_t/Z_0$. $Z_n = 0$ means short-circuit termination, $Z_n = 1$ means matched termination and $Z_n = \infty$ means open-ended.

The maximum voltage V_{max} is determined by DC characteristics of the transmission line, and hence it is expressed as R, G, R_t and l. V_{max} is derived with the RG ladder circuit shown in Fig. 3. Even when the number of shunt conductance is larger than three, V_{max} hardly changes, and hence we calculate V_{max} with Fig. 3. In this case, V_{max} is expressed as follows.

$$V_{max} = \frac{R_t}{(Z_0 + Rl/4)(1 + \frac{R_t + Rl/4}{Gl/3} + A + B) + B \cdot Gl/3}, \quad (6)$$

$$A = \frac{1}{Gl/3}\left(\frac{Rl}{2} + \frac{Rl}{4}\left(\frac{R_t + Rl/4}{Gl/3}\right) + R_t\right), \quad (7)$$

$$B = \frac{1}{Gl/3}\left(\frac{Rl}{4}\left(1 + \frac{R_t + Rl/4}{Gl/3} + A\right) + A \cdot Gl/3\right). \quad (8)$$

The voltage V_T is expressed in the PWL waveform model of Fig. 2 as

$$V_T = V_r + (V_{max} - V_r)\frac{T - t_r}{2t_{tof}}. \quad (9)$$

We thus calculate V_{eye} of Eq. (1) analytically.

C. Derivation of eye-opening in time

We next derive a closed-form expression for eye-opening in time. Without DC bias, the eye-opening in time becomes maximum when the voltage is $V_{max}/2$. As shown in Fig. 4, the latest rise transition starts from $V = 0$. On the other hand, the earliest transition begins at $V = V_{max} - V_T$. The jitter is the $V_{max}/2$ crossing time difference between the earliest and latest transitions. As indicated in Fig. 4, there are three regions for calculating jitter.

$$Jitter = \begin{cases} \frac{V_{max} - V_T}{V_r} t_r & \text{(Region1)}, \\ \frac{V_{max} - 2V_r}{V_{max} - V_r} t_{tof} + \frac{V_{max} - 2V_T + 2V_r}{2V_r} t_r & \text{(Region2)}, \\ \frac{V_{max} - V_T}{V_{max} - V_r} 2t_{tof} & \text{(Region3)}, \end{cases} \quad (10)$$

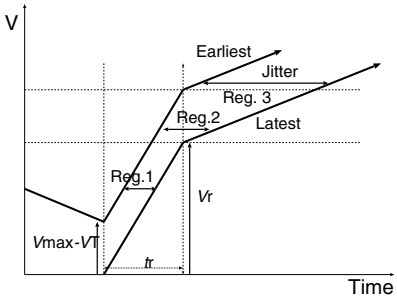

Fig. 4. Jitter model.

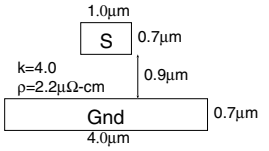

Fig. 5. Wire cross-section.

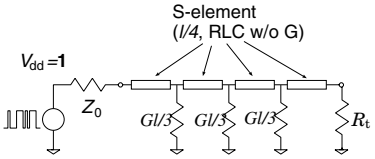

Fig. 6. Setup for model verification.

where $(V_r > V_{max}/2)$ in Region1, $(V_r < V_{max}/2, V_{max} - V_T + V_r > V_{max}/2)$ in Region2 and $(V_r < V_{max}/2, V_{max} - V_T + V_r < V_{max}/2)$ in Region3.

D. Model Verification

We verify the appropriateness of the proposed analytic model. We here use an on-chip microstrip transmission-line shown in Fig. 5 for experiments. The relative permittivity of insulator is 4.0, and the metal conductivity is $2.2\mu\Omega$·cm. The resistance, inductance and capacitance are computed by a commercial 2-D field solver. Figure 6 shows the circuit setup for simulation. We here model the RLC transmission line whose length is $l/4$ as an S-element implemented in HSPICE, where s-parameters are described in S-element. The simulation considers the frequency dependence of interconnect characteristics. Three shunt conductance of $Gl/3$ are inserted between the successive S-elements. We confirmed that the simulation results were almost unchanged even if the number of wire and shunt segments increased. PRBS pulses are given to the driver, and measure the eye-diagram at the far-end.

We first verify the accuracy of eye-opening in voltage. Figure 7 shows the eye-opening vs. transmission speed. The interconnect length is 6mm and R_t is 100Ω. Three lines correspond to the estimation results of the proposed model, and the conductance values are different. The dots are the circuit simulation results. The conductance value changes the eye-opening, and the proposed model estimates it well. As the transmission speed becomes faster, the eye-opening decreases. This tendency is also estimated by the model.

We next vary the shunt conductance and the termination resistance in 6mm-long 20Gbps transmission. In this configuration, larger termination resistance and smaller shunt conductance enlarge eye-opening (Fig. 8). In the case of R_t = 400Ω with small shunt conductance, the estimation error is large. Even if impedance mismatch at the far-end causes a large reflection, multiple-reflection would not arise because of impedance matching at the driver side. However, in reality, perfect impedance matching is impossible because

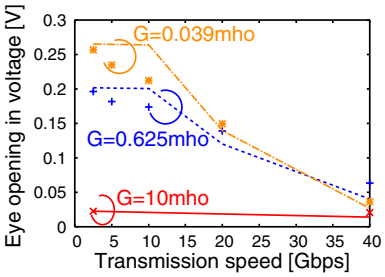

Fig. 7. Eye-opening in voltage vs. transmission speed (6mm, R_t = 100Ω).

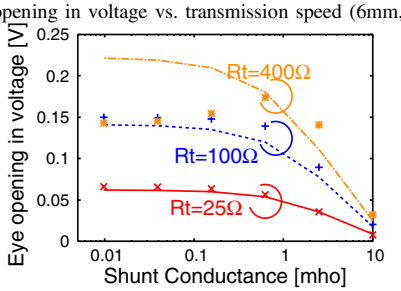

Fig. 8. Eye-opening in voltage vs. shunt conductance (6mm, 20Gbps).

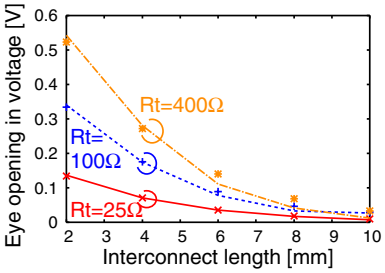

Fig. 9. Eye-opening in voltage vs. interconnect length (G=2.5mho, 20Gbps).

of frequency dependence of characteristic impedance. Thus, a certain amount of estimation error is introduced.

Figure 9 shows the eye-opening in voltage vs. interconnect length. The shunt conductance is 2.5mho, and the transmission speed is 20Gbps. We can see that the decreasing tendency of eye-opening is well estimated by the proposed model.

We finally verify the appropriateness of the eye-opening in time. Figure 10 shows the eye-opening in time estimated by the proposed model and circuit simulation. The vertical axis is the eye-opening in time normalized by the cycle time (1-$Jitter/T$). As the shunt conductance becomes small, the eye-opening decreases. This means the shunt conductance reduces ISI, whereas it decreases eye-height as shown in Fig. 8. The superiority of less ISI and the inferiority of eye-height decrease in shunt-inserted transmission lines are well modeled. We can thus use the proposed model for exploring the design space of on-chip transmission lines in terms of shunt conductance, termination resistance, transmission speed and so on.

III. Design Space Exploration

This section discusses shunt conductance and termination resistance that maximize signaling performance. When the signaling speed is not high and ISI is small, insertion of shunt conductance only reduces the signal magnitude, and it is not desirable. On the other hand, when bit-rate is high, ISI degrades signal integrity, and in this case, shunt insertion

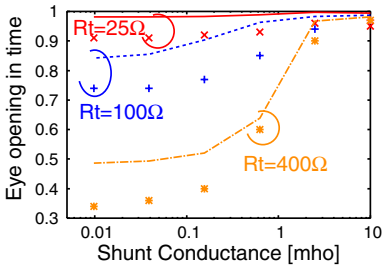

Fig. 10. Eye opening in time vs. shunt conductance (6mm, 20Gbps).

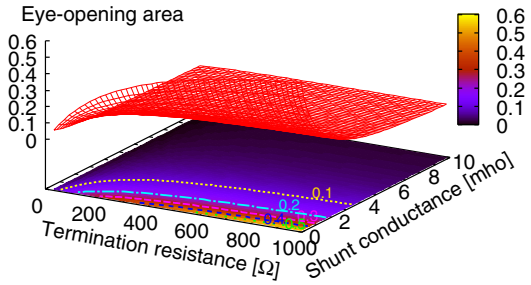

Fig. 11. Eye-opening area with various termination resistance and shunt conductance (6mm, 10Gbps).

is effective. We here evaluate the trade-off of signaling performance with respect to shunt conductance and termination resistance, and reveal that the proposed model is useful for the design space exploration early in the design stage.

Suppose 6mm-long 10Gbps signal transmission with the microstrip structure in Fig. 5. With the proposed model, we evaluate the area of eye-opening, where the area is defined as the product of the eye-opening in voltage and that in time normalized by the cycle time. The result is shown in Fig. 11. The contour lines of the eye-opening area are drawn on the bottom. In this configuration, high termination resistance and small shunt conductance enlarge the eye-area opening. On the other hand, when the signaling speed goes up to 40Gbps, the optimal values become much different (Fig. 12). Shunt conductance of 3.34mho and termination resistance of 114Ω maximize the eye-opening area. The optimal values depend on signaling speed and interconnect length. The proposed model can show the performance trade-off quickly, and hence it is helpful early in the design stage.

We finally show another performance analysis. Static power consumption is an important performance metric, and hence it is considered in this experiment. The vertical axis of Fig. 13 is the eye-opening area divided by static current. Here, the static current is the DC current of the voltage source in Fig. 3, and its analytic expression is easily derived. The optimal values of R_t and G are 81.5Ω and 2.97mho. We can easily analyze various performance trade-offs.

IV. Conclusion

This paper proposed a closed-form expression of eye-opening for shunt-inserted on-chip transmission lines. The eye-openings in voltage and time are derived analytically and experimentally verified in accuracy. We demonstrated trade-off analysis with the proposed model in terms of shunt conductance and termination resistance. The optimal values

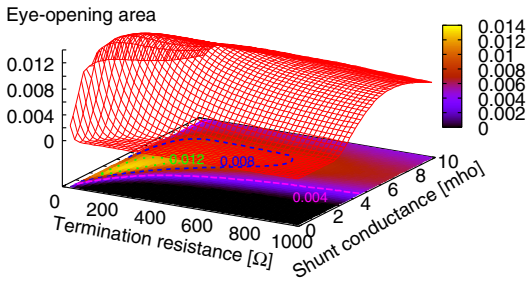

Fig. 12. Eye-opening area with various termination resistance and shunt conductance (6mm, 40Gbps).

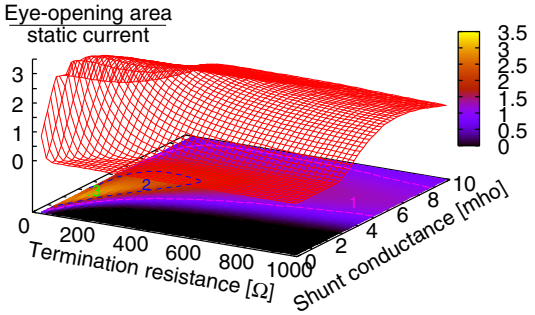

Fig. 13. Eye-opening area / static current (6mm, 40Gbps).

are dependent on signaling configuration, and the design space exploration early in the design stage is enabled by the proposed model.

Acknowledgment

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