Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect

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Abstract— **This paper proposes an all digital measurement circuit called "gated oscillator" for capturing waveforms of dynamic power supply noise. The gated oscillator is constructed with standard cells, and thus easily embedded in SoCs. The performance of the gated oscillator is testified with fabricated test chips in a 90nm process. Characteristics of decoupling capacitance are discussed focusing on channel length and distance, based on supply noise waveforms measured by the gated oscillator.**

I. Introduction

Power supply noise has become a serious problem in recent processes because of lowered supply voltage and increasing current consumption. Decoupling capacitance (decap) mitigates dynamic power supply fluctuation [1]–[4]. However, excessive decoupling capacitance consisting of MOS transistors involves severe gate leakage in advanced technologies [2]. To mitigate the gate leakage problem, efficient decap insertion, that is inserting necessary and sufficient amount of decap to a right place, is highly demanded. Developed decap insertion methods should be verified on silicon in terms of noise suppression efficiency.

For this purpose, a small measurement circuit suitable for embedding in a DUT is required. Easiness of circuit and layout design is another important factor to probe any points of interest inside a chip. Existing measurement circuits [4]–[10] require analog circuit techniques, and need dedicated analog power and bias lines. The additional routing and area costs restrict the number of measurement circuits integrated in a DUT and their placable positions. A common ring oscillator measurement [11], which can be easily implemented, observes averaged supply voltage, not dynamic noise waveform. Therefore, it cannot be used for evaluation of decoupling capacitance effect.

In this paper, we propose an all digital measurement circuit for dynamic noise waveform. Reference [12] proposed a measurement circuit for dynamic noise waveform with only digital circuit components. This circuit, however, has a limitation that DUT operation must synchronize with the clock generated inside the measurement circuit, and an external clock signal can not be given to the DUT. The proposed circuit is also a ring oscillator based circuit, but it accepts any external clock. Features of the proposed circuit are: 1) including only digital standard cells, 2) no need for dedicated analog power supply and reference voltage, 3) small circuit area, and 4) operation with any external clock.

The features are enabled by a new idea that the proposed circuit samples and holds ring oscillator state, whereas conventional circuits sample and hold analog voltage [4], [5]. Implementation of the proposed measurement circuit is very easy because design techniques for analog circuits and dedicated power lines for measurement circuit are not needed. Our measurement circuit can be built only with standard cells. Its layout design is compatible with common cell-base design and the size and shape are flexible. As our measurement circuit can synchronize with any reference clock, DUT operation frequency is freely changable.

We designed several types of TEGs varying design parameters of decoupling capacitance, and observed dynamic supply noise waveforms. Measurement results indicate that design of decoupling capacitance influecnes the peak voltage drop.

The remaining of this paper is organized as follows. Section II explains the proposed measurement circuit and verifies the performance on silicon. Section III discusses the decoupling capacitance effect based on measurement results. Section IV concludes this paper.

II. Measurement circuit structure

This section describes the measurement circuit to observe dynamic power supply noise. We first explain the proposed measurement circuit and the implementation. We then demonstrate the performance of the measurement circuit with measurement results.

A. Proposed gated oscillator

Figure 1 shows the proposed measurement circuit named "gated oscillator". The gated oscillator consists of only digital circuit components; inverters, a NAND gate, and transmission gates. The gated oscillator can observe waveforms of dynamic power supply noise. The gated oscillator is activated during the time period of interest ('enable'=1), and in the other period ('enable'=0), the oscillator is frozen by cutting off the transmission line. Conventional circuits sample and hold an analog voltage. However, the proposed circuit runs and holds the ring oscillator operation. Though conventional circuits need analog input/output or analog-to-digital/digital-to-analog converter, the proposed circuit requires a counter, where the counter is also composed of only digital components.

The operation of the gated oscillator is explained in detail using Fig. 2. The gated oscillator operates only while 'enable'=1, and the oscillating signal is stopped by the transmission gates when 'enable'=0. Suppose a power supply noise waveform in Fig. 2. The cycle count of the oscillator depends on only the power supply voltage while enabled. The supply waveform while 'enable'=1 is sampled, and the operation of the gated oscillator is hold while 'enable'=0. The analog

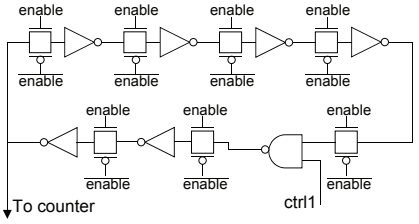

Fig. 1. Gated oscillator.

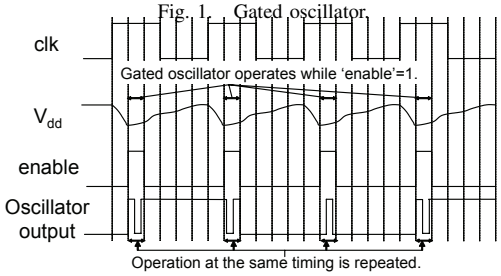

Fig. 2. Operation of the gated oscillator.

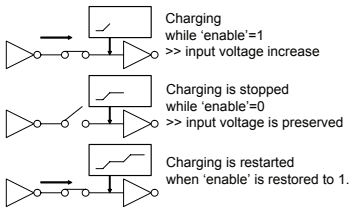

Fig. 3. Intermediate voltage preservation of gated oscillator.

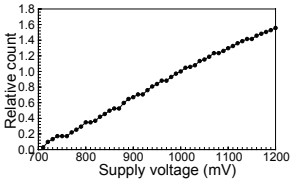

Fig. 4. Calibration table of gated oscillator in simulation.

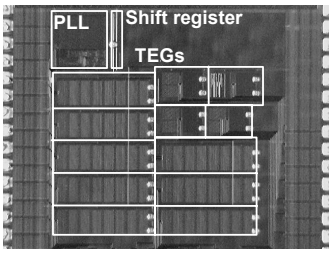

Fig. 5. Micrograph of the test chip.

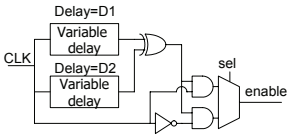

Fig. 6. Circuit for 'enable' signal generation.

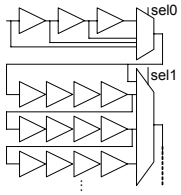

Fig. 7. Variable delay circuit.

voltage of the power supply is translated into the toggle count. Therefore, the gated oscillator can be regarded as a sample and hold circuit with an analog-to-digital converter.

To obtain enough cycle count for accurate measurement, the gated oscillator should be enabled repeatedly at the same timing. We also need to measure the cycle count without noise varying supply voltage for making a calibration table of voltage vs. cycle count. The voltage is computed from the measured cycle count with the prepared calibration table. We sweep the sampling timing and measure the count, and then construct the dynamic power supply noise.

An important metric of the measurement circuit is the voltage resolution. In the gated oscillator, the number of transmitting gate while 'enable'=1 is changed by the supply voltage. In addition, our gated oscillator can preserve the intermediate voltage of the transition at the timing when the oscillation is stopped (Fig. 3). When 'enable' is set from 1 to 0 while the inverter input is changing from 0 to 1 or 1 to 0, the input voltage is preserved at an intermediate level, whereas rigidly speaking, charge injection through the transmission gate slightly changes the voltage. After 'enable' is restored to 1, the transition restarts from the preserved intermediate level. This intermediate voltage preservation holds the ring oscillator state continuously, which improves the voltage resolution. Figure 4 shows the voltage resolution of the gated oscillator evaluated by circuit simulation. X-axis is the stable supply voltage, and Y-axis is the cycle count of the gated oscillator normalized by the count at 1.0V. The period and number of 'enable'=1 are 300ps and 250, respectively. The count increases linearly. The gated oscillator is expected to have a fine resolution of 20mV.

B. Implementation of measurement circuit

We fabricated a test chip in a 90nm CMOS process. The nominal supply voltage of this process is 1.0V. Figure 5 is the micrograph of the test chip. The test chip includes several TEGs, a PLL, and shift registers. The shift registers are written and read by external input and output. Control signals of TEGs and PLL are stored in the shift registers. A part of the shift register also operates as a counter, and counts the toggle of the gated oscillator.

Each TEG includes a DUT and a measurement circuit. The measurement circuit consists of the gated oscillator, and circuits for 'enable' signal generation. 'enable' signal of the gated oscillator should be synchronized with DUT operation clock. We designed an 'enable' signal generator in Fig. 6 that consists of variable delay, XOR gate, AND gates, and a multiplexer. This generator varies the pulse width and timing of 'enable' signal by controlling the variable delay circuits. The generated pulse width is $|D1 - D2|$, where $D1$, $D2$ are the delays of variable delay circuits. The pulse timing of 'enable' from 'CLK' edge is changed from $\min(D1, D2)$ to $\max(D1, D2)$. The reference edge of 'CLK' is chosen from rise and fall transition by 'sel' signal. In this work, we adopted variable delay circuit of Fig. 7, which consists of buffers and multiplexers. $D1$ and $D2$ vary from 0- to 255-stage buffer delay.

DUT includes switching circuits for noise generation, power supply line, and decoupling capacitance. The circuit for noise generation consists of 12-stage NAND gates. 64×8 cells of 12-stage NAND gates are placed in each TEG. The gated oscillator shares the power supply line with the noise generator inside a TEG. Each DUT has a dedicated external power supply respectively, and the substrate of each DUT area is isolated by triple-well.

The layout size of the gated oscillator is $11.76\mu\text{m}\times$

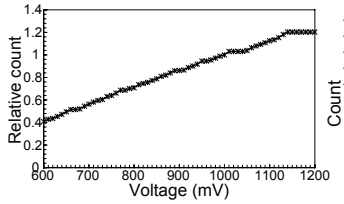

Fig. 8. Calibration result of the gated oscillator.

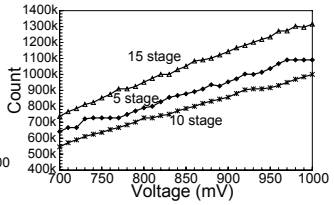

Fig. 9. Comparison results of calibration results. Timing widths of 'enable' pulse are set to 5, 10, 15 buffer stages.

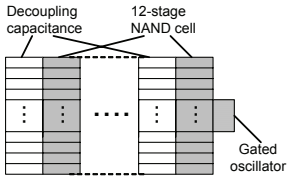

Fig. 10. Structure of DUT for TEG A-D.

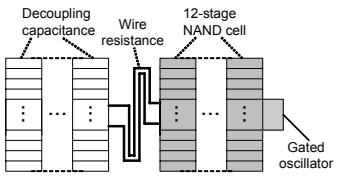

Fig. 11. Structure of DUT for TEG E and F.

15.12μm, and comparable to the other analog measurement circuits [4], [9]. In this work, 4X inverters and transmission gates are used to suppress random process variation. Otherwise, the layout size can be shrunk to roughly one-fourth. The gated oscillator consists of only digital standard cells, which yields layout flexibility and process portability.

C. Evaluation of proposed measurement circuit

We here evaluate the measurement precision and reproducibility of the proposed gated oscillator based on measurement results. The fabricated test chip was mounted on a QFP package. The external control signals are generated with a pattern generator, and output signal, which includes the gated oscillator counts, are observed with a logic analyzer. Figure 8 shows the measured cycle count of the gated oscillator without noise generation. The pulse width of 'enable' signal is 10-stage buffer delay. The voltage resolution of the gated oscillator is estimated to be 10-20mV below 1.0V, and is sufficient for measurement.

A noise waveform was measured for 1000 times to evaluate the reproductivity. The maximum standard deviation at 10 timing points is 0.98%, and the gated oscillator has fine reproductivity.

We compare the voltage resolution varying the pulse width of 'enable' signal in Fig. 9. The number of 'enable' pulse whose width is 5-stage buffer delay is 4 million, and in other cases 2 million. The voltage resolutions of 10- and 15-stage pulse width are better and their resolutions are roughly 10mV. In the rest of this paper, we use 'enable' signal of which width is 10-stage buffer delay. The buffer delay is measured using ring oscillator embedded in 'enable' timing generation circuit, and the 10-stage buffer delay is about 300ps-450ps.

III. Discussion about decoupling capacitance

This section discusses the effect of decoupling capacitance focusing on the channel length and the resistance between operating circuit and capacitors. The structure of DUT in each TEG is shown in Figures 10, 11, and TEG variation is summarized in Table I. We change the channel length of decoupling capacitance so that the area or the total capacitance becomes unchanged (TEG B-D). The resistance to decoupling capacitance is varied in TEG E and F. The cycle of the gated oscillator is measured for five times in the same condition and the average of five values are used for voltage computation. The pulse of the gated oscillator is counted for 20ms, and 'enable' signal is generated every 10ns.

TABLE I
TEG variation.

TEG	Decap ch. length	Note
A	-	No decap
B1	0.1μm	Decap capacitance is same as TEG C.
B2	0.1μm	Decap area is same as TEG C.
C	1μm	86.6pF
D1	5.98μm	Decap capacitance is same as TEG C.
D2	5.98μm	Decap area is same as TEG C.
E	1μm	Wire R is 1.7Ω. Decap is same as TEG C.
F	1μm	Wire R is 26.7Ω. Decap is same as TEG C.

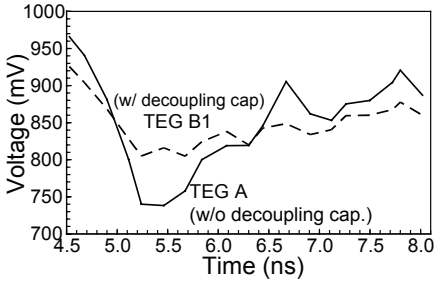

Fig. 12. Measurement results of TEGs w/ and w/o decap (B1, A).

A. Effect of decoupling capacitance

We first compare the noise waveform between TEG without decoupling capacitance (TEG A) and TEG with enough decoupling capacitance (TEG B1) in Fig. 12. The minimum supply voltages of TEG A and B1 are 730mV and 800mV. Decoupling capacitance reduces the voltage drop by 70mV.

B. Channel length of decoupling capacitance

We next discuss the channel length of decoupling capacitance. Figure 13 compares the noises in TEG B1 (L=0.1μm), TEG C (L=1μm), and TEG D1 (L=5.98μm). Total capacitance values of decoupling capacitors in three TEGs are almost equal. The peak voltage drop of TEG D1 is 20mV larger than those of other TEGs, which indicates that long channel length degrades RC time constant of decoupling capacitance. On the other hand, the peak voltage drop of TEG B1 and C are almost the same, though the channel length is different. We think RC time constant of L=1μm decap is small enough for noise suppression in this case.

We next keep the decap area unchanged for different channel lengths, and compare the noises (Fig. 14). Generally, larger capacitance can be integrated in the same area by using longer channel transistors. The ratio of total capacitance among TEGs is about B2:C:D2 = $2:6:9$. The peak voltage drop of TEG B2 is larger because of small total capacitance. On the other hand, the quite similar result is observed in TEG C and D2. Though TEG D2 has 1.5 times larger capacitance than TEG

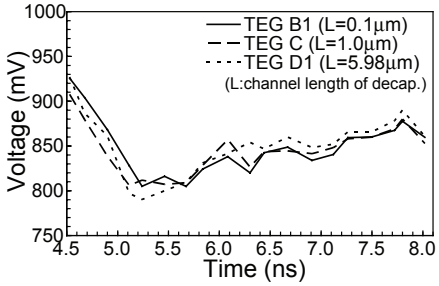

Fig. 13. Measurements results of TEGs with 0.1(B1)/1(C)/5.98(D1)μm. Total capacitance of decoupling capacitance is almost equal.

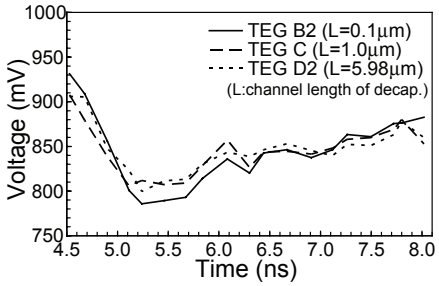

Fig. 14. Measurements results of TEGs with 0.1(B2)/1(C)/5.98(D2)μm channel length decoupling capacitance. The area of the capacitors is equal.

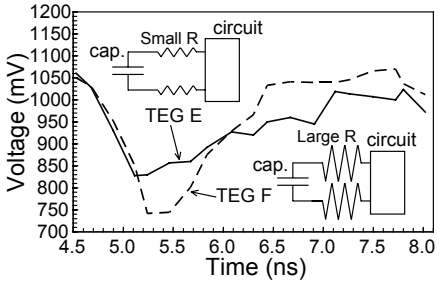

Fig. 15. Measurements results of TEGs E and F. The wire resistances between operating circuit and decoupling capacitance of TEGs E and F are 1.7 and 26.7Ω respectively.

C, the voltage drop did not decrease because of poor RC time constant.

This measurement result confirms that using decoupling capacitance with appropriate channel length can improve the area efficiency without degrading noise suppression effect. On the other hand, when channel length is too large, the performance of decoupling capacitor deteriorates.

C. Resistance between operating circuit and decoupling capacitance

Figure 15 compares the measured supply noise waveforms of TEGs E and F. The resistance difference between operating circuit and decoupling capacitance (1.7Ω and 26.7Ω) corresponds to the distance difference from decoupling capacitance in actual designs (16μm and 250μm). The difference of peak voltage drop between two TEGs is about 80mV. We have confirmed that wire resistance degrades RC time constant of decoupling capacitance and noise suppression effect. The resistance/distance from decoupling capacitance should be carefully examined to avoid unexpected large noise.

IV. Conclusion

We proposed the gated oscillator that captures dynamic supply noise waveform. The proposed gated oscillator holds the state of the ring oscillator instead of analog voltage. The noise waveform is reproduced from the measured cycle of ring oscillator. The gated oscillator consists of digital standard cells only, and does not require analog circuits dedicated power lines, and reference voltage. The voltage resolution and reproductivity of the proposed circuit were confirmed on the test chip fabricated in a 90nm CMOS process.

The characteristics of decoupling capacitance are evaluated with the gated oscillator. The measurement results indicated that the channel length of decoupling capacitance had a trade-off between area and response, and appropriate channel length could improve area efficiency without response degradation. We also observed that the resistance between decoupling capacitance and operating circuit deteriorated the effect of decoupling capacitance.

Acknowledgment

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