Impact of Well Edge Proximity Effect on Timing

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***Abstract*— This paper studies impact of the well edge proximity effect on digital circuit delay, based on model parameters extracted from test structures in an industrial 65nm wafer process. The experimental results show that up to 10% of delay increase arises by the well edge proximity effect in the 65nm technology, and it depends on interconnect length. Furthermore, due to asymmetric increase in pMOS and nMOS threshold voltages, delay may decrease in spite of the threshold voltage increase. From these results, we conclude that considering WPE is indispensable to cell characterization in the 65nm technology.**

I. Introduction

At front-end stages of CMOS wafer process, P and N types of ions are implanted to form wells. During the implantations, lateral scattering of the ions nearby edges of the photo-resist causes well doping concentration, as shown in Fig. 1 [1][2][3]. The well doping concentration mainly drifts the threshold voltage of MOS transistors. We call it "well edge proximity effect" (WPE). As advanced deep well implants with high-energy implanters are introduced to suppress parasitic bipolar gain for latch-up protection, WPE becomes severer. In circuit design, WPE can be suppressed by making a large separation between gate poly and enclosing well edge.

On the other hand, as shown in Fig. 2, common cell based designs intrinsically involve WPE, whereas analog circuit design can make use of the large separation. The figure depicts a part of standard cells placement. Since wells are continuous along the cell rows and then dummy cells are placed at the both ends of the cell rows for lithographical reasons, horizontal proximity between gate and well edges can be negligible. As for the vertical direction, the inner and the outer spacing shown in the figure are uniquely determined for cell by cell. Therefore, we should take care of WPE only for the vertical direction in the digital cell based design.

During circuit design, a lot of effort is put into timing convergence[4]. From a standpoint of circuit design, delay variation due to WPE is a matter of utmost concern. We evaluate the impact of WPE on circuit timing as a case study in an industrial 65nm technology, and demonstrate the delay increase quantitatively. We also point out that WPE decreases cell delay in some conditions of input waveform and output load.

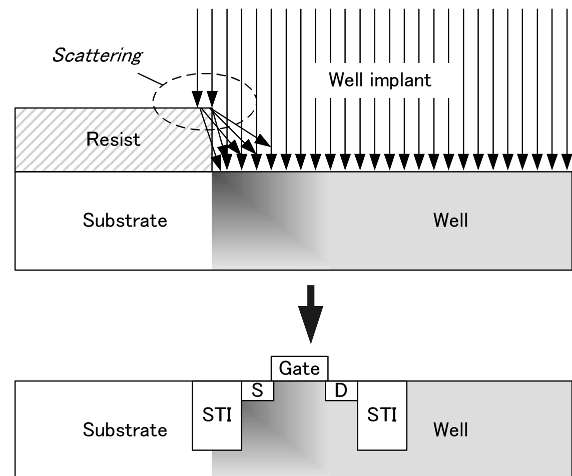

Fig. 1. Schematic representation of the well edge proximity effect.

II. Well Edge Proximity Effect Modeling

Threshold voltage V_{th} for MOSFETs with sufficiently long and wide channels are expressed by the following equation [5].

$$\begin{aligned} V_{th} &= VFB + \Phi_s + \gamma\sqrt{\Phi_s - V_{bs}} \\ &= VTH0 + \gamma(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}), \end{aligned} \quad (1)$$

where VFB is the flat band voltage, Φ_s is the surface potential, $VTH0$ is the threshold voltage of the device at zero substrate bias, and γ is the body bias coefficient which is proportional to square root of the substrate doping concentration. BSIM4.5 specifies the factor of increase in the substrate doping concentration due to WPE in terms of instance parameters SCA, SCB, SCC and model parameters K_{VTH0WE}, WEB, WEC[5][6][7]. Amount of the V_{th} shift is expressed by

$$dV_{th} = K_{VTH0WE} \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC). \quad (2)$$

Here, the instance parameters SCA, SCB, SCC correspond to profiles of the extra doped well ions due to WPE, and then they are determined by layout patterns of the MOS transistors. We derive the model parameters K_{VTH0WE}, WEB, WEC

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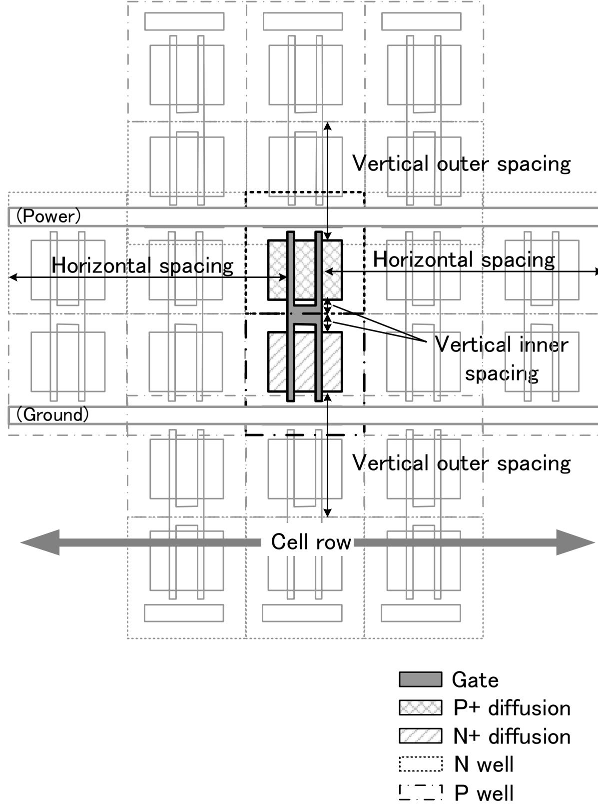

Fig. 2. Well edge proximity of the standard cell region.

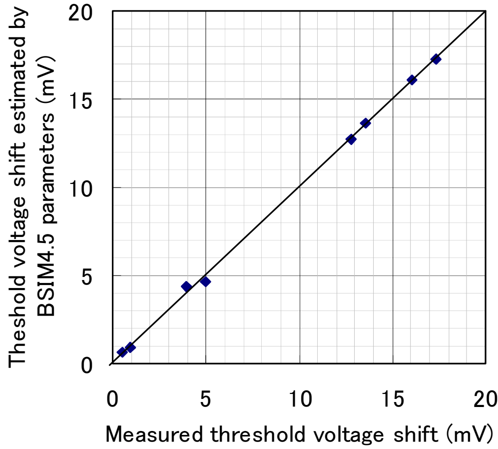

Fig. 3. dV_{th} estimation using BSIM4.5 parameters.

by fitting them to the measured dV_{th} for a set of layout patterns of test element groups. Figure 3 shows effectiveness of the dV_{th} fitting. X-axis is the measured Vth shift and Y-axis is the Vth shift in BSIM4.5 model with the derived parameters. We can see WPE modeling is well performed.

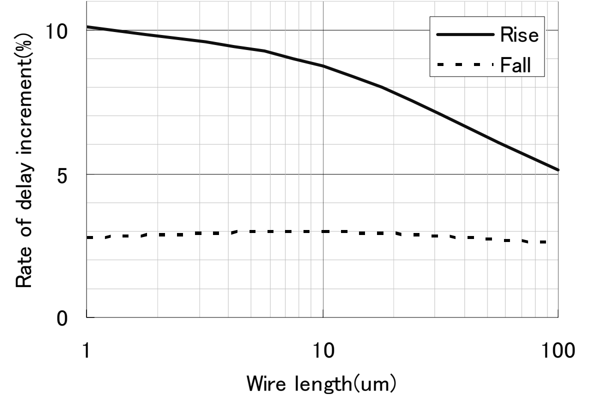

Fig. 4. Delay increment due to WPE (FO1 small inverters chain).

III. Impact of Well Edge Proximity Effect on Timing

We derive the model parameters explained in the previous section for a 65nm SoC process. As shown in [3], the threshold voltage shifts of p type MOS transistors are larger than n type MOS transistors due to difference in the substrate doping concentration. Actually, the maximum difference in the threshold voltage shift reaches three times. Using the model parameters and the instance parameters extracted from layout patterns of standard cells for the SoC process, we achieve the following experiments.

A. Wire length and fan-out dependency of the delay increase

First, we evaluate delay of two kinds of inverter chains by circuit simulation. The examined inverter cell is applied to within 100μm range of wire interconnections. One inverter chain includes the inverters with single fan-out (FO1), where each inverter drives single inverter with the same size. The other inverter has the inverters with 20 fan-out (FO20), where each inverter drives 20 same size inverters. Wires connecting the inverters, which are assumed to be in a semi-global layer [8], vary from 1μm to 100μm.

Figure 4 shows the simulated cell delay[9] of the FO1 inverter chain, where relationship between gate and well edges is as shown in Fig. 2. In the figure, “rise” and “fall” denote rising and falling transitions of output signal of the inverter. As seen in the figure, the delay increase due to WPE is up to 10% for this inverter chain, where the rising delay increase is larger than the falling delay increase. It is because the rate of the threshold voltage shift in pMOS is twice as large as the rate in nMOS. We also see in the figure that rate of the delay increase is reduced as the inverter drives longer wires. Buffers inserted in a short distance are sensitive to WPE.

Figure 5 shows the simulated cell delay of the FO20 inverter chain. This situation makes the input transient time of the inverter cell longer compared to the FO1 case. Wire length dependency is much smaller than the FO1 case since the output load capacitance of the inverter is almost determined by the FO20 of the gate capacitance.

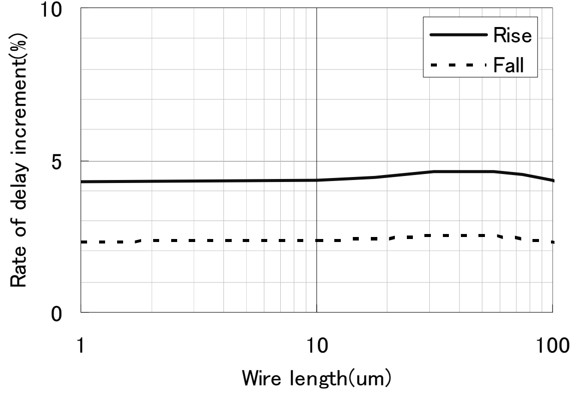

Fig. 5. Delay increment due to WPE (FO20 small inverters chain).

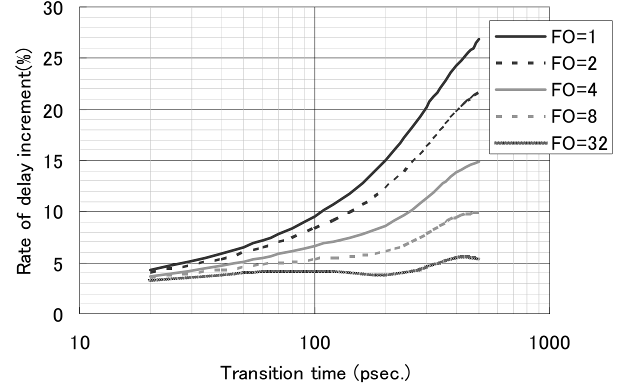

Fig. 6. Load capacitance and transient time dependency of delay increment due to WPE (Large inverter, rising delay).

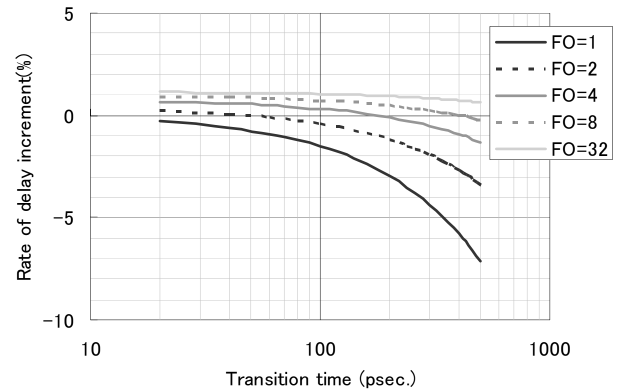

Fig. 7. Load capacitance and transient time dependency of delay increment due to WPE (Large inverter, falling delay).

B. Conditions of decreasing buffer delay

Next, we examine inverter chains with 24 times larger inverters than the previous ones. MOS transistors in each inverter cell form multiple fingers due to the limitation of cell height. The p type MOS finger has the same size as the p type MOS transistor in the previous inverter. On the other hand, the n type MOS finger is twice wider than the previous one. In general, wider MOS transistors are less affected by WPE[6]. However, the large standard cell inverter gets the same amount of WPE as the previous small inverter due to the finger division. We examine the impact of WPE along cell delay tables[9] in order to understand the impact of WPE systematically. The cell delay tables show that falling delay can decrease due to WPE when the input transient time is large and the output load (fan-out) is small (Fig. 7), unlike rising delay (Fig. 6). The reason is thought to be that decrease in leakage current of pMOS exceeds the decrease in pull-down current of nMOS. Figures 8 and 9 show current decreases due to WPE. Figure 8 shows that the leakage current of pMOS is highly suppressed by WPE, compared with current reduction of nMOS in Fig. 9.

Then, we examine whether the case of decreasing the delay appears in the inverter chain. Since the delay decrease can occur when the fan-out is small, we simulate the FO1 chain. Figure 10 shows the results. In the wire length range up to $800\mu m$, the falling delay decrease appears. As the wire becomes long, the wire capacitance increases the output load, and then the falling delay decrease becomes small. As the result, there are cases that delay decreases in spite of the threshold voltage increase.

IV. Conclusion

This paper has investigated the impact of WPE on circuit delay, applying the WPE model and extraction methodology to circuits supposing buffer insertion cases in a cell based design. The experimental results show that up to 10% of delay increments are caused by WPE in a 65nm SoC process. Further, the asymmetric increase in the threshold voltages between p and n type MOS devices causes the situation of decreasing delay because the decrease in leakage current of pMOS overwhelms the decrease in pull-down current of nMOS. From these results, we conclude that WPE in the 65nm technology should be taken into consideration. Especially, since the case of decreasing delay can happen, WPE should be cared for the hold time check in the timing verification, as well as the setup time checking. In general, since the delay change due to WPE varies instance by instance, it should be treated as one of the systematic variability factors[10]. As for the digital cell based design, considering WPE is indispensable to cell characterization in the 65nm technology.

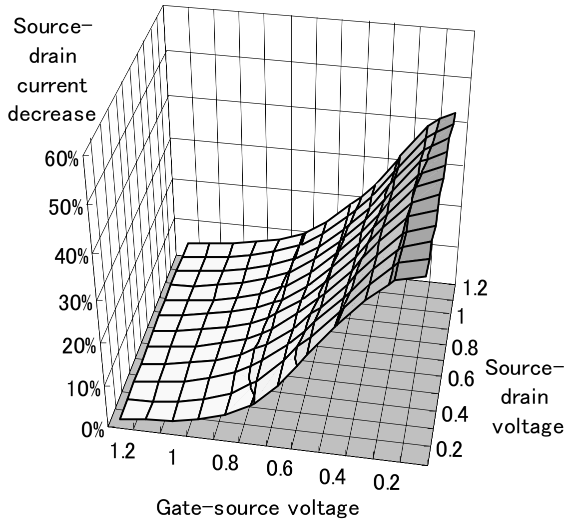

Fig. 8. Current decrease due to WPE (pMOS).

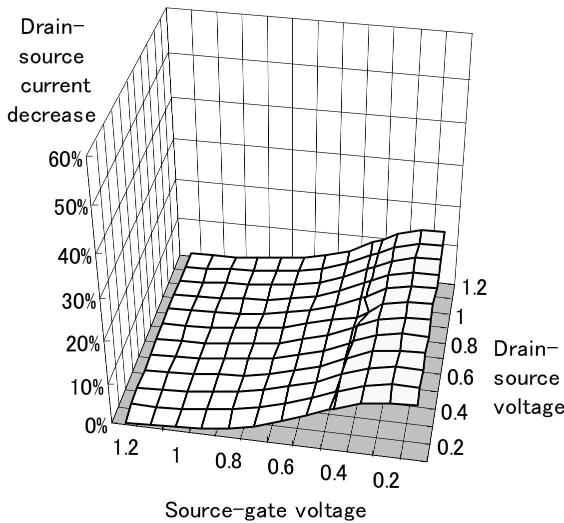

Fig. 9. Current decrease due to WPE (nMOS).

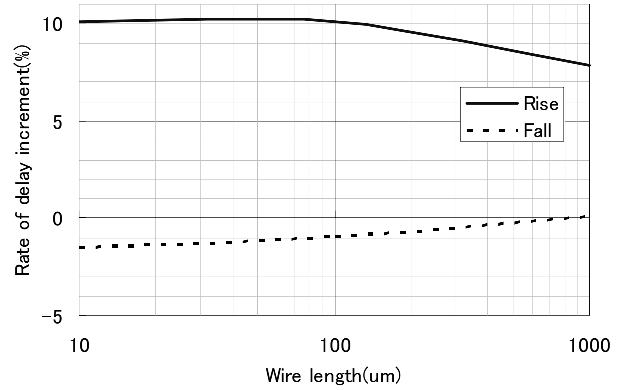

Fig. 10. Delay increment due to WPE (FO1 large inverters chain).

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