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LETTER *Special Section on VLSI Design and CAD Algorithms*

Effects of On-Chip Inductance on Power Distribution Grid

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SUMMARY With increase of clock frequency, on-chip wire inductance starts to play an important role in power/ground distribution analysis, although it has not been considered so far. We perform a case study work that evaluates relation between decoupling capacitance position and noise suppression effect, and we reveal that placing decoupling capacitance close to current load is necessary for noise reduction. We experimentally show that impact of on-chip inductance becomes small when on-chip decoupling capacitance is well placed according to local power consumption. We also examine influences of grid pitch, wire area, and spacing between paired power and ground wires on power supply noise. When effect of on-chip inductance on power/ground noise is significant, minification of grid pitch is more efficient than increase in wire area, and small spacing reduces power noise as we expected.

key words: *power distribution network, on-chip inductance, power supply noise, decoupling capacitance*

1. Introduction

On-chip power/ground network analysis currently considers inductances of package and bonding wires commonly. On the other hand, inductances of on-chip wires are hardly considered, because inductances of on-chip wires are smaller than those of package and bonding wires so far. In addition, in low clock frequency, impedance due to resistance is dominant. However, packages with low parasitic inductance, such as a flip-chip package, are becoming popular. As clock frequency increases, power supply noise contains higher frequency components, and reactance ωL dominates impedance of the power network instead of resistance. In the future, power/ground analysis for high-speed circuits needs to consider on-chip inductance.

Reference [1] gives an outline of LSI power distribution system with on-chip wire inductance and estimation of on-chip inductance in power grid. Reference [1] also shows that on-chip power grid behaves as a 2D transmission line, and noise propagates as a wave. Reference [2] proposes a fast simulation method for power grid based on transmission theory. Reference [3] discusses optimal wire structures of on-chip power/ground lines from the point of on-chip inductance. Reference [4] is a prior work that presents power distribution analysis without considering on-chip wire inductance underestimates voltage fluctuation by over 50%. Reference [4] also indicates that the effect of on-chip inductance becomes significant when package impedance is small. Although these works start to study power network analysis with on-chip wire inductance, it is still unclear in what conditions we must consider on-chip inductance. This paper discusses behaviors of power/ground network with on-chip inductance, and evaluates analysis error due to ignoring on-chip inductance. From our experiments focusing on distribution of power consumption and policy of decoupling capacitance insertion, we reveal conditions that on-chip inductance must be considered, and demonstrate that position of decoupling capacitance is important to mitigate on-chip inductance effect as well as to reduce power supply noise. We also study how we should design robust power distribution network in point of grid pitch, power/ground wire area, and spacing between paired power and ground wires.

Section 2 gives a description of an equivalent circuit used in LSI power/ground network analysis. Section 3 discusses response of power distribution network excited by one current source. Section 4 shows simulation results when power consumption is not uniform, and discusses relationship among on-chip inductance, power consumption distribution and decoupling capacitance positions. Section 5 examines the relation between physical parameters of power grid and voltage fluctuation. Finally, conclusion is remarked in Sect. 6.

2. Equivalent Circuit Model for Power Grid Analysis

Power distribution network in LSI is usually analyzed by using simplified equivalent circuit models since it is very complex and large. Figure 1 shows the power grid structure we analyze in this paper. Power wires and ground wires run in parallel in the same layer. In this paper, we consider

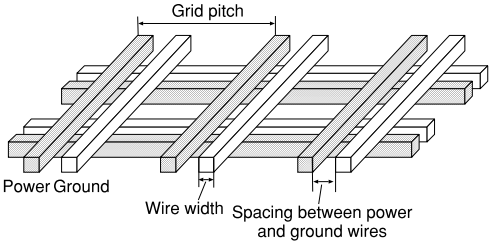

Fig. 1 Power grid structure.

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the topmost power grid only. Figure 2 is an example of a popular equivalent circuit[5]. On-chip power/ground wires are modeled in lumped resistance, self-inductance, mutual inductance, and capacitance. Junction capacitance and gate capacitance inside logic gates are connected between power and ground lines through on-resistance of MOS transistors. Well junction capacitance is also connected. Load current that working circuits consume is modeled in a current source. When we model silicon substrate, resistance mesh is connected to ground lines, although Fig. 2 does not include the substrate model. Power IOs, which supply current from PCB to LSI, are often modeled in series of an inductance and a resistance. This circuit corresponds to parasitic elements of bonding wire and package line. We often connect ideal voltage sources outside the package when we analyze on-chip power distribution network.

On-chip inductance is traditionally ignored, because on-chip inductance is smaller than package inductance and analyzing power network with on-chip inductance requires huge computational cost. However, flip-chip package using bump-arrayed power IO reduces parasitic inductance to below 1 nH. Thus, on-chip inductance is now comparable with package inductance. On-chip inductance depends on wire structure, especially length. When paired P/G wires with $10\,\mu$m width are routed with $100\,\mu$m pitch, the self-inductance is hundreds pH/mm. Another reason that makes the effect of on-chip inductance significant is improvement in circuit operation speed. In high frequency operation, reactance in power/ground lines becomes comparable with, or larger than resistance, and hence it has a significant impact on power delivery system.

Simulating a circuit with on-chip inductance expends much time than without on-chip inductance. Hence, some simplifications of circuits that have many inductances are proposed (survey is found in Ref. [6]). These methods reduce simulation time. There is, however, a problem that simplification may spoil accuracy and/or convergence. Therefore in this paper, we do not truncate any partial mutual inductances to accurately evaluate impact of on-chip inductance in Sects. 3 and 4. On the other hand, in Sect. 5, we use a simplification technique to analyze finer power grid.

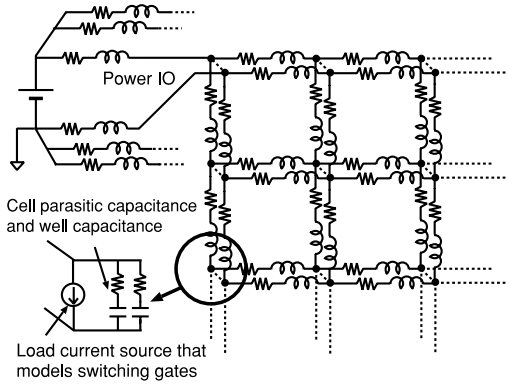

Fig. 2 A simple model of LSI power distribution circuits.

3. Dependency of Voltage Fluctuation on Slope of Load Current and Decap Position

Section 2 describes an equivalent circuit model of LSI power network. In this model, superposition theory holds, since it is a linear circuit. The overall voltage fluctuation can be computed by superposing every voltage fluctuation caused by each current source. This section discusses behaviors of power distribution circuits with a single current source in order to clearly evaluate impact of on-chip inductance on power voltage fluctuation.

3.1 Current Slope vs. Noise Amplitude

We first study a dependency of power supply fluctuation on current slope (di/dt). We vary transition time of load current T_r in Fig. 3 and evaluate the power supply noise assuming a $0.13\,\mu$m technology. The power grid network used in the experiment is as follows. The chip size is $2 \times 2\,\text{mm}^2$. Wire material is aluminium. Power grid is routed with $100\,\mu$m pitch. The wire width and thickness are $10\,\mu$m and $1\,\mu$m respectively. Ground wires are routed similarly. We calculate partial self inductance and partial mutual inductance between parallel lines using an analytic approach based on Geo-Metrical Distance (GMD) concept [7]. We then construct a full PEEC model [8], which means all mutual inductances are included. Partial self-inductance of power line is 585 pH/mm. Power source is 1.2 V. We attach nine paired power/ground IO-cells whose inductance and resistance are 0.5 nH and $1\,\Omega$. We assume that logic (NAND) gates occupy half of chip area, and the capacitance that those gates have is connected between power and ground lines. Silicon substrate is not considered in our analysis. A load current source is placed at center of the chip. The current is decided such that all NAND gates placed in $3000\,\mu\text{m}^2$ area switch. The transition time Tr of the current is set to 50, 66, 100 ps. When $Tr = 50$ ps, the peak current is 32.8 mA. In this paper, we assume simultaneous switching as a worst-case analysis although gate switching is distributed within a clock cycle in an actual chip. From another point of view, we can suppose that sharp current spike corresponds to high-speed operation in advanced technologies in the future.

Figure 4 shows the simulation results with and without on-chip inductance. Without on-chip inductance, the volt-

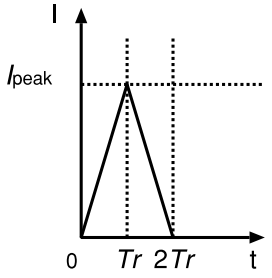

Fig. 3 Waveform of load current.

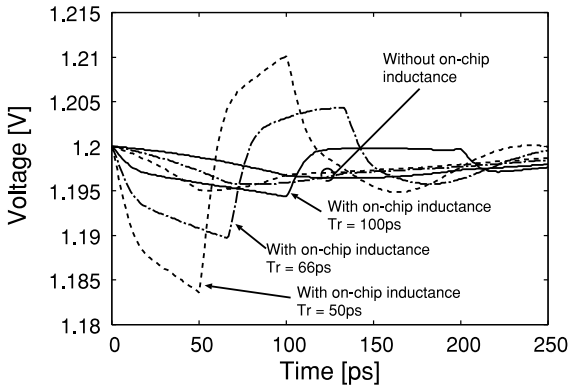

Fig. 4 Voltage fluctuation with and without on-chip inductance in various *Tr* conditions.

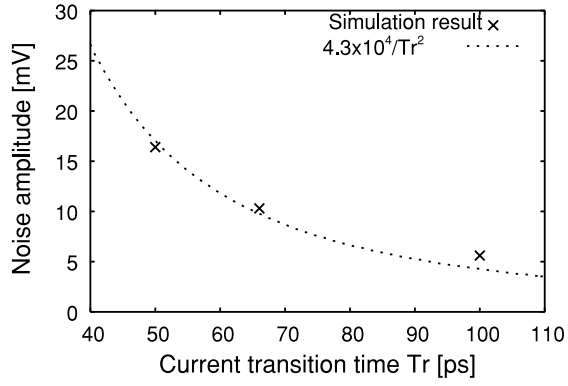

Fig. 5 Dependency of voltage fluctuation on transition time T_r.

age fluctuations are almost the same even though *Tr* varies. On the other hand, Fig. 5 shows that the voltage fluctuation with on-chip inductance changes and the peak values are 5.6 mV, 10.3 mV, and 16.4 mV, which are almost in inverse proportion to Tr^2. In this situation, a small portion of the circuit consumes power, and a lot of capacitance that works as decoupling capacitance is available on the chip. However there is not enough decoupling capacitance close to the current source, which causes excessively large voltage fluctuation due to on-chip inductance.

3.2 Relationship among Decap Size, Decap Position and Noise Amplitude

We next attach a decoupling capacitance to power grid, and evaluate effect of suppressing voltage fluctuation by circuit simulation. Results are shown in Fig. 6. We place a decoupling capacitor at two different positions; at the same place with the load current source, and the place 100 μm away from the load current source. The capacitance value is 68.4 pF, and it is large enough to suppress voltage fluctuation when it is placed at the same place with the load current source. The capacitance of 68.4 pF corresponds to MOS gate area of 5,000 μm^2. When the decoupling capacitance is placed at the load current source, the voltage fluctuation is substantially reduced. On the other hand, the capacitance placed 100 μm away from the current source can not suppress the voltage fluctuation effectively. Even if we increase the capacitance value to 684 pF, which is impossible to integrate in a grid, voltage fluctuation is not suppressed as long as the capacitor is placed 100 μm away from the current source.

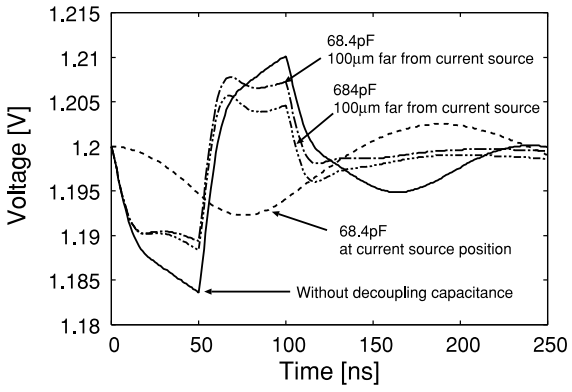

Fig. 6 The effect of decoupling capacitance away from load current (*Tr* = 50 ps).

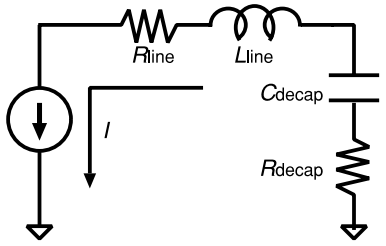

Fig. 7 An equivalent circuit of power line and decoupling capacitor.

3.3 Qualitative Analysis of Dependency on Current Slope and Decap Position

We analyze the simulation results in the previous subsections qualitatively. The effect of on-chip decoupling capacitance depends on inductance of power/ground lines as well as parasitic series resistance of the decoupling capacitance and resistance of power/ground lines between load source and decoupling capacitor. Figure 7 is a very simple equivalent circuit model of local power distribution network that includes a decoupling capacitor and a current source. We here focus on local mechanism of charge supply and use the equivalent circuit in Fig. 7, although it can not represents the behaviour of the entire power grid network. Impedance that excludes the capacitance, Z_{eff}, is expressed by the line resistance and the inductance between the current source and the capacitor (R_{line}, L_{line}) and the series resistance of the decoupling capacitance (R_{decap}). When the load current is triangle as shown in Fig. 3, the impedance Z_{eff} becomes

$$\frac{dI}{dt} = \frac{I_{\text{peak}}}{Tr} \qquad (1)$$

$$Z_{\text{eff}} = \frac{L_{\text{line}} \cdot dI/dt}{I_{\text{peak}}} + R_{\text{line}} + R_{\text{decap}}$$

$$= \frac{L_{\text{line}}}{Tr} + R_{\text{line}} + R_{\text{decap}}, \quad (2)$$

where Tr is the transition time of the load current, and I_{peak} is the peak current. If the decoupling capacitor is so large that the voltage across the capacitance is constant, the maximum drop voltage V_{drop} is expressed as follows.

$$\begin{aligned} V_{\text{drop}} &= I_{\text{peak}} Z_{\text{eff}} \\ &= L_{\text{line}} \frac{I_{\text{peak}}}{Tr} + (R_{\text{line}} + R_{\text{decap}}) I_{\text{peak}}. \end{aligned} \quad (3)$$

On-chip inductance adds the first term to the voltage drop. This term includes transition time Tr, and hence the voltage drop V_{drop} depends on not only I_{peak} but also Tr.

Resistance R_{line} and inductance L_{line} are in proportion to the distance between the current source and the capacitor. Therefore, the effect of decoupling capacitance becomes smaller as the distance increases, which is shown in Fig. 6. In other words, when on-chip inductance is taken into account and switching speed becomes faster, we must place decoupling capacitance at a closer place to current source.

When the number and the size of switching transistors are unchanged, which means that average power dissipation is the same and is the same situation in Fig. 5, the product of I_{peak} and Tr is constant. I_{peak} is inversely proportional to Tr. When Tr becomes smaller, the voltage drop due to resistance is in proportion to Tr, and the voltage drop due to inductance is proportional to Tr^2. This analysis is consistent with the result shown in Fig. 5.

From Eq. (2), the ratio of impedance caused by on-chip inductance L_{line} to the total impedance from current source is expressed as

$$Ratio = \frac{L_{\text{line}}/Tr}{L_{\text{line}}/Tr + R_{\text{line}} + R_{\text{decap}}}. \quad (4)$$

When we assume the decoupling capacitance 100 μm far from the current source used in the experiments in this section, the parameters become $R_{\text{line}} = 0.36\,\Omega$, $L_{\text{line}} = 117$p, and R_{decap}=0. The ratio is 0.87 and 0.76 for Tr=50 and 100 ps, which reveals that the impedance of on-chip inductance starts to shield distant decoupling capacitance dominantly as current spike becomes sharp. Please recall that the purpose of the discussion here is to analyze the effect of on-chip inductance on the charging characteristics in a qualitative way using a localized equivalent circuit. Thus a numerical example shown above does not necessarily represent the overall supply noise behavior of the entire power grid. This simple model, however, gives a good insight into the effect of a decoupling capacitor placed away from the current source.

3.4 Analysis of Decap Position in Frequency Domain

We here examine the noise dependency on decap position based on frequency domain analysis. We again assume the decoupling capacitance 100 μm far from the current source, and the equivalent circuit model in Fig. 7. The size of decoupling capacitance C_{decap} is 68.4 pF. Figure 8 shows the

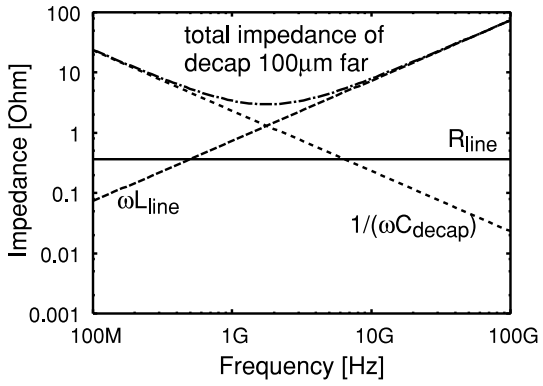

Fig. 8 Impedance of decoupling capacitance placed 100 μm away from the current source calculated in Fig. 7. $R_{\text{line}} = 0.36\,\Omega$, $L_{\text{line}} = 117$ pH, $C_{\text{decap}} = 68.4$ pF, R_{decap}=0.

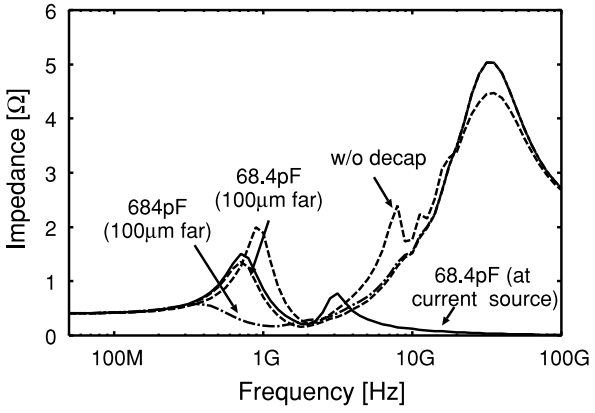

Fig. 9 Impedance at the current source.

impedance evaluated at the current source versus frequency. Below 2 GHz, the capacitance 100 μm far works as a decoupling capacitance, on the other hand, above 2 GHz, it does not. This is because impedance due to on-chip inductance increases linearly, and consequently it dominates other elements in high frequency range. This result indicates that when the noise component above 2 GHz is dominant, we must place decoupling capacitance at more adjacent position. Figure 9 shows the impedance of the entire power grid, which is the same as used in Fig. 6. The parasitic series inductance of decoupling capacitance itself is not considered. We can see that, in the frequency region below 2 GHz, a bigger capacitance of 684 pF placed 100 μm apart can reduce the impedance seen at the current source. However, in the frequency region above 2 GHz, the decoupling capacitance placed at 100 μm away can not suppress the impedance, whereas the smaller capacitance at the current source does reduce the impedance in the high frequency region.

4. Power Grid Analysis Focusing Distribution of Power Consumption

The previous section shows behaviors of power distribution circuits with a single current source. In actual chips, many load current sources work simultaneously. This section focuses on distribution of power dissipation, and evaluates supply voltage fluctuation. We vary circuit conditions such as switching activity of each circuit block, size and position of decoupling capacitors, and examine impact of on-chip inductance in each condition.

We use a chip model in a 0.13 μm technology that is similar with that used in Sect. 3. Power distribution topology is power grid. The pitch of power wires is 300 μm. The wire width and thickness is 30 μm and 1 μm. Ground wires are routed similarly. The power grid size is 20×20, and the chip size is $6 \times 6\,\mathrm{mm}^2$. We calculate on-chip inductance like Sect. 3, and then construct a full PEEC model. The supply voltage is 1.2 V. The power is supplied through 100 pairs of power IOs. Each power IO has 0.5 nH and 1 Ω. We assume that logic gates occupy half of the chip area, and their capacitance is connected between power and ground lines.

Load current sources, in which working circuits are modeled, are placed at each junction of the grid. The clock frequency is 500 MHz. We assume that load current flows at both rising and falling edges of the clock signal, and thereby the cycle of load current is 1 GHz. The transition time *Tr* of current sources is 50 ps. We simulate this chip with the following two conditions of switching activity; 1) uniform power consumption, i.e. power dissipation at each grid is the same (uniform case), and 2) the power consumption per grid at the center of the chip is five times larger than that at the periphery of the chip (unbalance case). The uniform case assumes that 20% of transistors are switching. As for the unbalance case, 50% of transistors are switching at the center as well, also 10% of transistors are switching at the periphery. In both cases, the peak current in the whole chip is 590 mA.

4.1 Without Decoupling Capacitance

Impact of on-chip inductance depends on distribution of load current source, i.e. power dissipation. Figures 10 and 11 show simulation results without decoupling capacitor. In the uniform case of Fig. 10, error caused by ignoring on-chip inductance is about 10% of voltage fluctuation. This error may not affect circuit delay considerably. However, in the unbalance case of Fig. 11, ignoring on-chip inductance causes 35% estimation error, and it is not acceptable in circuit design.

Figure 12 explains the reason. When load current at each grid is the same, almost all current comes from the capacitance at the same grid. The amount of current that flows through the branch is very small. That is why on-chip inductance hardly affects voltage fluctuation when power consumption is uniform.

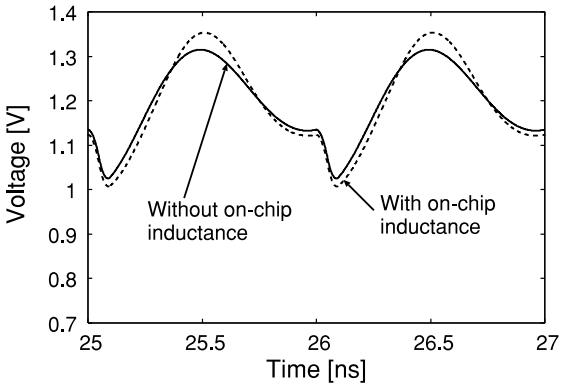

Fig. 10 Voltage fluctuation in power grid: uniform case (at center of chip).

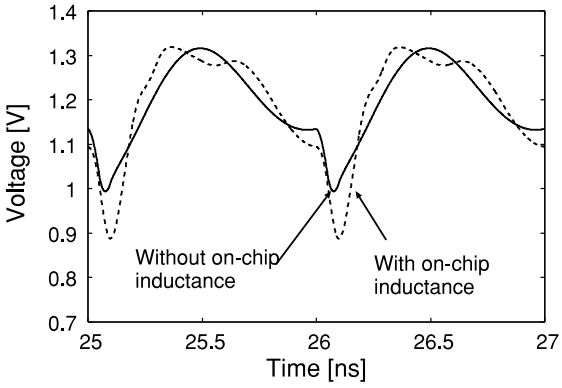

Fig. 11 Voltage fluctuation in power grid: unbalance case (at center of chip).

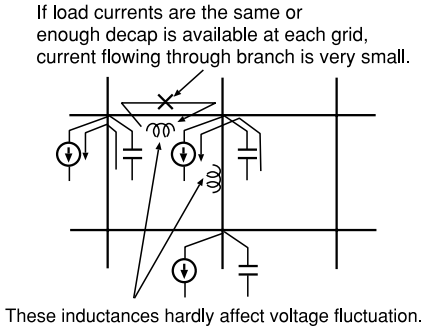

Fig. 12 Reason why on-chip inductance hardly affects voltage fluctuation.

In the balanced case, the effect of on-chip inductance is very small on the voltage waveform, and the major part of the voltage fluctuation is the result of bounce due to package and bonding wire inductances and on-chip capacitances distributed within the die.

Let us discuss the unbalance case. In this case, almost all capacitances that placed on the chip work to suppress voltage fluctuation, if on-chip inductance is not considered. However, when we consider on-chip inductance, capacitances far from current source hardly help to reduce voltage fluctuations.

When power consumption is uniform, error caused by ignoring on-chip inductance is small. When current consumption is not uniform, analysis without on-chip inductance is not accurate enough. Normally, power consumption of LSI is not uniform, and hence we need to consider on-chip inductance.

4.2 With Decoupling Capacitors

In modern LSI design, LSI power distribution network has numerous decoupling capacitors. We evaluate effect of on-chip inductance in power network with decoupling capacitance. We append intentional decoupling capacitors to power distribution network according to a simple method to calculate required capacitance size [9].

We calculate the amount of decoupling capacitance to suppress voltage fluctuations below 10% of supply voltage. We simulate three power distribution circuits that have different amount of decoupling capacitance; 25%, 50% and 100% of the calculated capacitance. Decoupling capacitors are placed in the following two strategies. One strategy places capacitors uniformly on the chip (uniform placement). In other words, this strategy does not consider power consumption distribution, but it performs chip-level capacitance insertion. The other strategy places large capacitor near large current source (adaptive placement). In both strategies, total amount of decoupling capacitance in the circuit is the same. We examine how the effect of on-chip inductance varies according to the design policy of decoupling capacitance in size and placement.

The method to calculate required decoupling capacitance [9] is briefly explained. Size of decoupling capacitor C is calculated from target of maximum voltage ripple δV and charge within one current cycle $Q = I_{\text{peak}} Tr/2$.

$$C = Q/\delta V. \tag{5}$$

From this formula, in the case that capacitors are placed uniformly, capacitance of 12.3 pF, which corresponds to MOS gate of 1,000 μm^2, is inserted at every 400 grid in the circuits. As for the adaptive placement, capacitance size varies from 6.15 to 30.7 pF according to load current at each grid.

Figure 13 shows the results of the uniform placement case, and Fig. 14 shows the result of the adaptive placement case. When decoupling capacitors is inserted according to the local load current and its size is enough (100% size in Fig. 14), the effect of on-chip inductance on voltage fluctuation is not significant. When decoupling capacitor size becomes smaller, ignoring on-chip inductance causes a large amount of error. We can also see that the placement of decoupling capacitance is very important, comparing Fig. 13 with Fig. 14. Even if size of decoupling capacitors is large enough to suppress voltage fluctuation, the bad strategy of the uniform placement cannot suppress voltage fluctuation well.

Figure 15 shows the relationship between size of decoupling capacitance and the maximum voltage drop. When decoupling capacitors are placed by the adaptive placement,

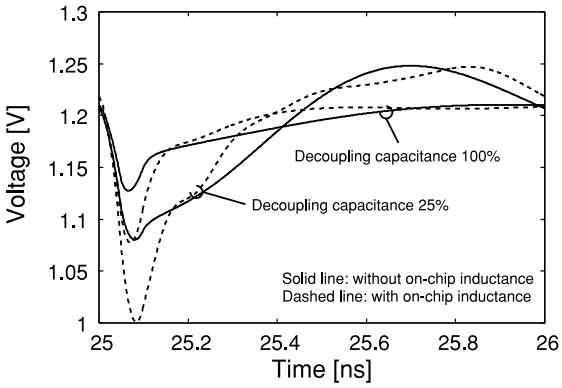

Fig. 13 Voltage fluctuation: uniform placement (at center of chip).

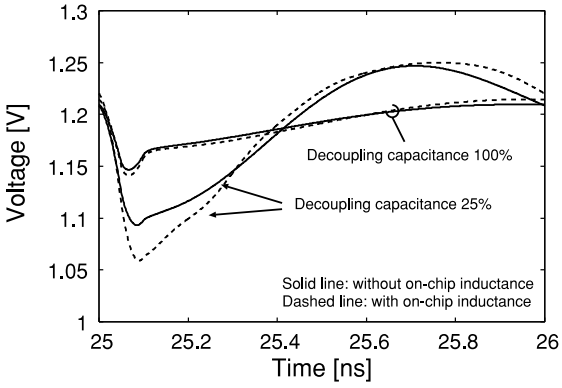

Fig. 14 Voltage fluctuation: adaptive placement (at center of chip).

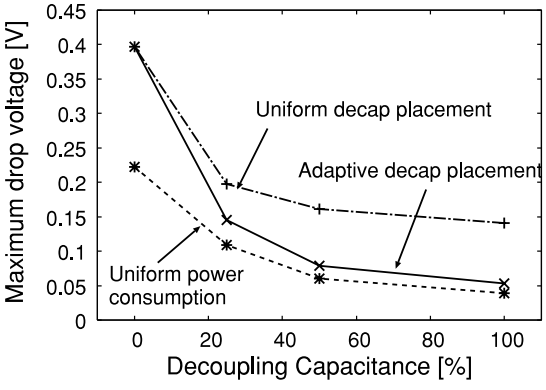

Fig. 15 Size of decoupling capacitor and voltage fluctuation.

voltage fluctuation becomes smaller rapidly as capacitor size increases. In the case of the uniform placement, enlarging capacitance decreases voltage fluctuation similarly, however its suppression effect is smaller than that of the adaptive placement.

With decoupling capacitance whose size is large enough compared with local load current, ignoring on-chip inductance does not affect voltage fluctuation seriously. In this situation, almost all load current comes from the neighboring decoupling capacitor. This means that the current that flows through branches is small and hence the effect of

on-chip inductance becomes small, which is similar with the discussion in the previous section (Fig. 12). As long as decoupling capacitor is well designed in size and placement, the accuracy of power analysis without on-chip inductance is acceptable. However, when estimation of load current is poor, the efficiency of decoupling capacitor insertion degrades and the effect of on-chip inductance becomes significant.

5. Power Grid Design for Robustness with On-Chip Inductance

This section evaluates the effect of on-chip inductance varying grid pitch, and wire area for power distribution (Fig. 1) in order to design robust power distribution network. The previous sections use the equivalent circuit that considers all mutual inductances in PEEC model in order to accurately evaluate the impact of on-chip inductance. However, the size of power distribution grid that can be analyzed is limited, because the inductance matrix is very dense. To evaluate finer power grid, this section uses a simplified equivalent circuit model that does not include mutual inductance.

We first demonstrate the error due to the simplified circuit model. When current loop is perfectly closed in paired power/ground wires, the inductively-coupled power/ground wires can be decoupled into two wires whose self- and mutual inductances are L-M and 0. Figure 16 shows the noise waveforms when PEEC and decoupled models are used. The experimental condition is the same with that in the previous section. The decoupling capacitance is not attached. Though the waveforms are partly different in unbalanced current distribution, we use the decoupled model in the following experiments, because the error is not significant and the computational time is reduced by 98%.

5.1 Power Grid Pitch and Wire Area

We first change power grid pitch and evaluate the effect of on-chip inductance while keeping the wire area of power grid unchanged. The wire resistance is determined by the wire area. On the other hand, inductance is not proportional to the wire area.

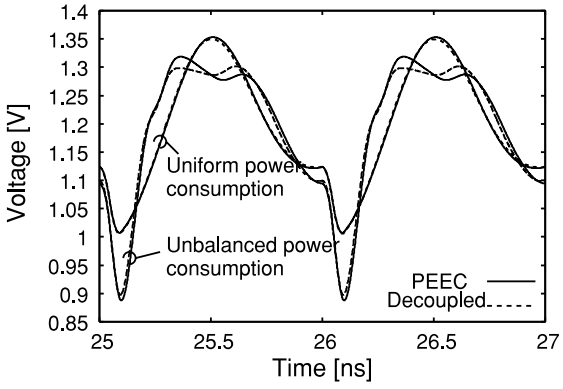

Fig. 16 Comparison between PEEC and decoupled models.

We change power grid pitch to 50 μm, 100 μm and 150 μm, and compare power noise with that in 300 μm pitch case in the previous section. The wire area ratio of power grid is 20%, where the wire area ratio is defined as 2×(wire width)/(grid pitch). The spacing between paired power/ground wires is 10 μm. The other conditions are the same with those in the previous section. The current distribution is unbalanced. Figures 17 and 18 show the results. Although the wire area is unchanged, the voltage fluctuation is reduced to 80% by changing grid pitch from 300 μm to 50 μm.

We examine the reason. The partial self inductance is expressed as follows [10]

$$L_{\text{partial}} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235(w+t)}{l}\right], \qquad (6)$$

where l, w, t and μ_0 are length, width and thickness of interconnect and permeability in vacuum. When $l \gg w$, which is common for PG wires, partial self inductance L_{partial} becomes a weak function of width w, i.e. L_{partial} does not vary much according to w. When the number of parallel PG wires is n_{wire} and L_{partial} is assumed to be independent of w, the effective inductance is roughly expressed as $L_{\text{partial}}/n_{\text{wire}}$. We can reduce the effective inductance by decreasing grid pitch. This is why the voltage fluctuation is reduced in finer power grid as shown in Fig. 18.

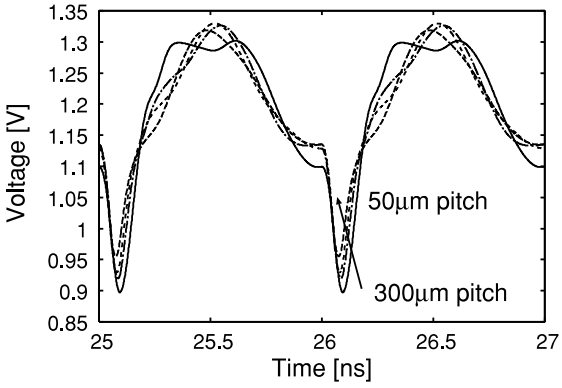

Fig. 17 Power noise waveforms when grid pitch is changed.

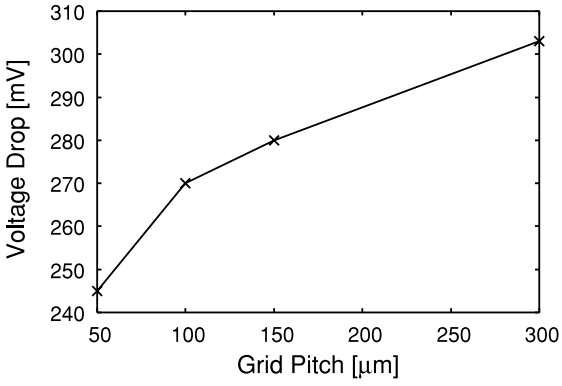

Fig. 18 Maximum voltage drop and grid pitch.

We next evaluate the effect of on-chip inductance when the wire area for power grid is varied. The variation of wire area ratio is 20%, 30%, 40% and 50%. The grid pitch is 300 μm and 50 μm. Figures 19, 20 show the simulation results. Figure 19 presents the voltage fluctuation when grid pitch is 300 μm, and Fig. 20 corresponds to the result in the case of 50 μm grid pitch. Figure 21 depicts the relationship between the maximum voltage drop and wire area ratio when on-chip inductance is considered. When grid pitch is large, the increase in wire area ratio from 20% to 50% reduces voltage variation by 10% when on-chip inductance is considered, and by 7% without consideration of on-chip inductance (Fig. 19). The noise reduction ratio with consideration of on-chip inductance is somewhat larger. When grid pitch is small, the amount of noise reduction is 7% both with and without considering on-chip inductance (Fig. 20).

Thus, making grid pitch smaller is very effective to suppress voltage fluctuation. Although increase in wire area suppresses power noise, its availability is smaller than that of minifying the grid pitch, because increase of metal area decreases resistance, but does not reduce inductance. When on-chip inductance dominates wire resistance, noise suppression due to resistance reduction is limited.

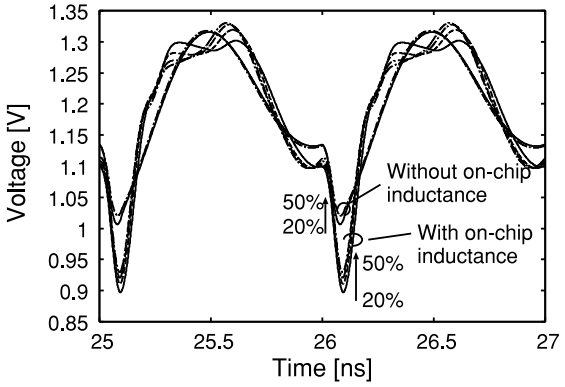

Fig. 19 Voltage fluctuation and wire area ratio (grid pitch 300 μm).

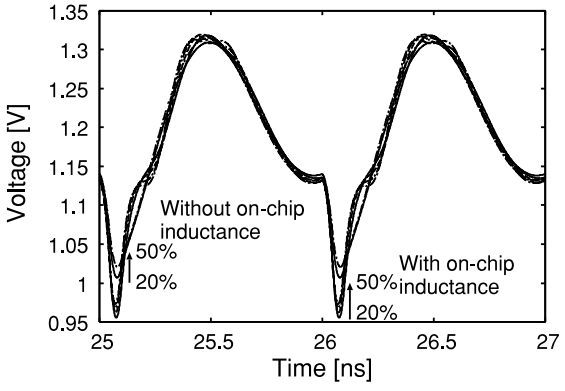

Fig. 20 Voltage fluctuation and wire area ratio (grid pitch 50 μm).

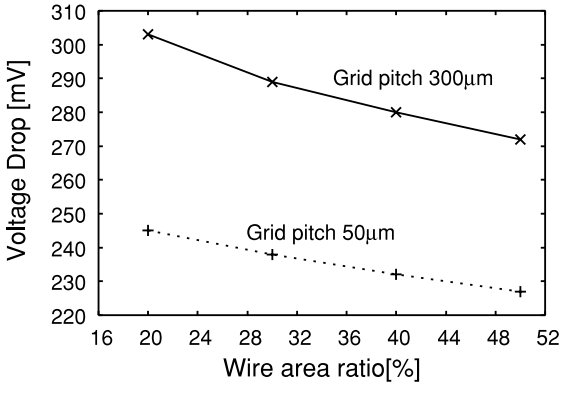

Fig. 21 Maximum voltage drop and wire area ratio (on-chip inductance is considered).

5.2 Spacing between Power and Ground Wires

In the experiments shown so far, the spacing between power and ground wires are small. In this case, wire inductance becomes small, since the current loop becomes small [1]. We here evaluate how important the spacing is for power supply noise. We assume that power grid pitch is 300 μm and 50 μm. The thickness of wires is 1 μm, and the wire area ratio is 20%. We then vary spacing between power and ground wires to 2, 5, 10, 30, and 120 μm, and evaluate the voltage fluctuation, where the spacing of 30 and 120 μm is evaluated only when grid pitch is 300 μm.

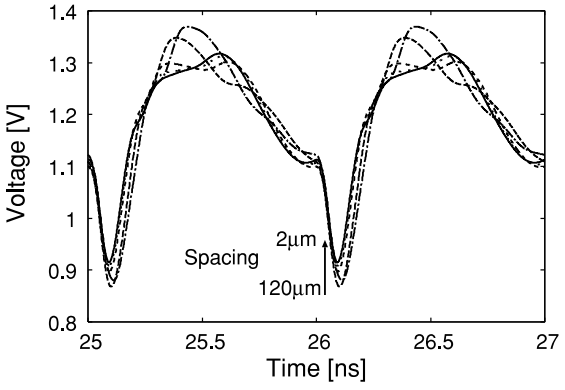

Fig. 22 Voltage fluctuation and spacing (grid pitch 300 μm).

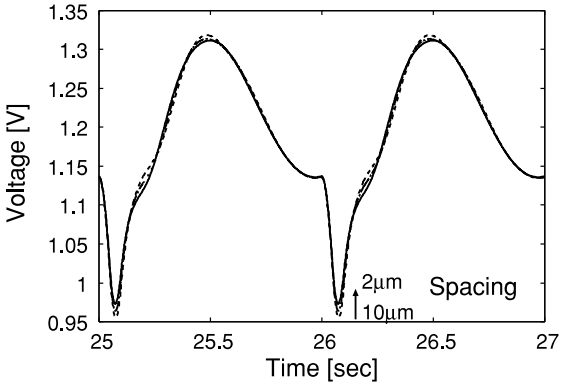

Fig. 23 Voltage fluctuation and spacing (grid pitch 50 μm).

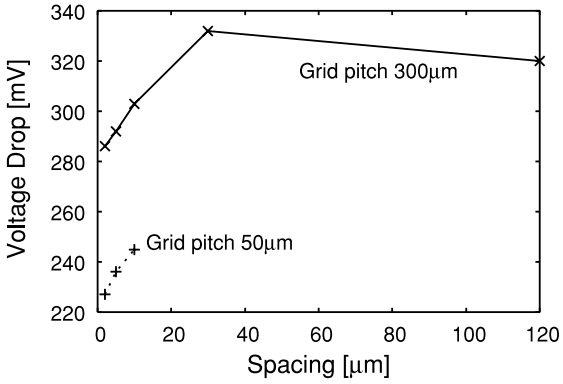

Fig. 24 Maximum voltage drop and spacing.

Figures 22, 23 show the noise waveforms. Figure 24 summarizes the relation between the maximum voltage and spacing. When grid pitch is 300 μm, the maximum noise voltage increases from 285 mV to 320 mV by changing the spacing from 2 μm to 120 μm. The variation ratio of noise voltage is ±5–6% compared with the noise of 303 mV in the case of 10 μm spacing. The voltage fluctuation is also reduced by 8% when the spacing decreases to 2 μm in the case of 50 μm grid pitch. Because noise waveforms depends on not only on-chip inductance but also package impedance, on-chip capacitance, etc. in a complicated manner, the relation between voltage drop and the spacing in Fig. 24 is not monotonic. However, when the spacing is small and the coupling between the power and ground wires is strong, we can see that noise voltage becomes small as the spacing decreases.

These results demonstrate that the spacing between power and ground wires affects power supply noise as we expected, and indicate that we should minimize the spacing to suppress power supply noise.

6. Conclusion

In this paper, the effect of on-chip inductance in power distribution network is discussed. This paper shows that voltage fluctuations are enlarged by on-chip inductance. Only capacitors that are placed close to load current source contribute to suppress voltage fluctuation effectively.

We evaluate the effect of on-chip inductance on voltage fluctuation under a power consumption distribution like a real chip operation. When chip power consumption is uniform, error caused by ignoring on-chip inductance is small enough. Even if power consumption is not uniform, as long as decoupling capacitors are designed appropriately in placement and size, ignorance of on-chip inductance does not cause a significant error. When we design power network considering on-chip inductance, not only size of decoupling capacitors but also place of capacitors is crucial to enhance power supply integrity.

We also examine the influence of grid pitch, wire area, and spacing between power and ground wires on voltage fluctuation. The results indicate that making grid pitch smaller is superior to increasing wire area in noise reduction effect when effect of on-chip inductance is significant. We also observe that smaller spacing between power and ground wires is preferable as we expected.

Acknowledgment

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