LETTER Special Section on VLSI Design and CAD Algorithms

Impact of Intrinsic Parasitic Extraction Errors on Timing and Noise Estimation*

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SUMMARY In this letter, we discuss the impact of intrinsic error in parasitic capacitance extraction programs which are commonly used in today's SoC design flows. Most of the extraction programs use pattern-matching methods which introduces an improvable error factor due to the pattern interpolation, and an intrinsically inescapable error factor from the difference of boundary conditions in the electro-magnetic field solver. Here, we study impact of the intrinsic error on timing and crosstalk noise estimation. We experimentally show that the resulting delay and noise estimation errors show a scatter which is normally distributed. Values of the standard deviations will help designers consider the intrinsic error compared with other variation factors.

key words: *interconnect, delay variation, parasitic capacitance, SoC*

1. Introduction

With the progress in wafer process technology, it becomes impossible to ignore on-chip variations of the interconnect delay. This variation also affects the analysis of signal integrity (SI) issues, including crosstalk noise. Smaller on-chip wire pitch causes increase in delay and crosstalk noise, which are mainly due to parasitic capacitance [1]. Figure 1 shows an example of the delay deviation in a 90 nm SoC process when interconnect resistance and capacitance increase by 20%, respectively. As can be seen in the figure, it is important to precisely estimate and control the interconnect capacitance when discussing the signal propagation delay even for long interconnects.

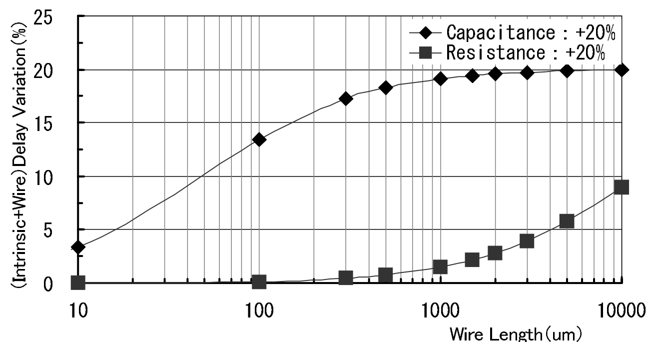

Fig. 1 Interconnect delay variation versus wire length for 20% change in R and C.

Systematic and random variations of interconnect capacitance regarding the actual wafers have been discussed using TEGs (test element group)s [2], [3]. Here, we discuss another source of variation due to errors in layout parasitic extraction (LPE) tools that are commonly applied to SoC design flows. We then show the impact of intrinsic error on timing and crosstalk noise estimation using the ITRS 90 nm SoC process.

2. Error Factors in Interconnect Capacitance Extraction

Most of the extraction programs [4]–[6] use pattern-matching methods that find a suitable primitive pattern in the pre-characterized library, where each primitive is characterized using field-solvers [7], [8]. The typical procedure of the primitive pattern matching is as follows.

Step1 Isolate geometries.
Step2 Allocate region of capacitance extraction for each geometry.
Step3 Decompose each region into primitives.
Step4 Look up primitives in the characterized library.
Step5 Combine primitive information to create an electric model.

Manuscript received March 10, 2006.
Final manuscript received June 8, 2006.
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DOI: 10.1093/ietfec/e89–a.12.3666

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Step6 Build the network and apply reduction for output.

Here, the major source of errors are in Step3 and Step4. In Step4, since the number of primitives is finite, errors are introduced due to interpolation. The number of primitives to be generated is determined considering the tradeoff between accuracy and library characterizing time. Here, it is important to make use of regularities of design in deciding primitive variation. In SoC design, one basic regularity is "HVH" routing [9], i.e. adjacent layer wires which are routed perpendicularly. Figures 2 and 3 show that layout patterns which do not obey "HVH" cause errors in interpolation. Since adjusting the primitive variation to design methods can reduce these errors, they are not intrinsic.

On the other hand, in Step3, since boundary conditions of the decomposed regions are different from the original layout patterns, unavoidable intrinsic errors occur. The amount of this error depends on the scale of the primitives which are determined considering the trade-offs. In the next section, we experimentally study what the error distribution is, and how large the impact on timing and crosstalk noise estimation is from this error in the current SoC technology node.

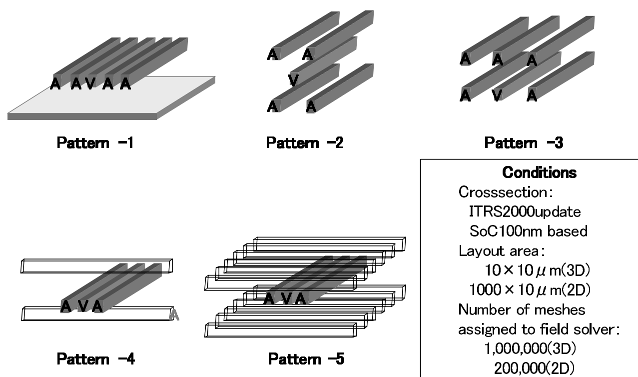


Fig. 2 Layout patterns to observe interpolation errors.

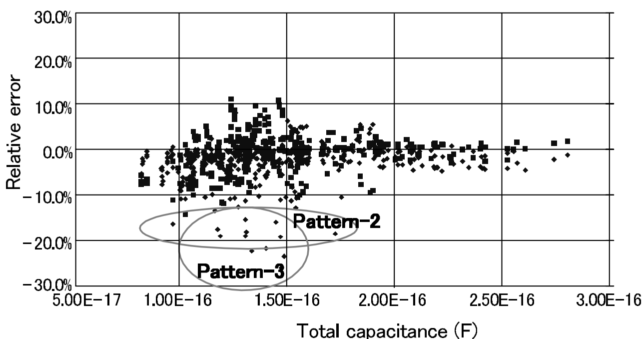


Fig. 3 Observed interpolation errors.

3. Impact of Intrinsic Extraction Errors on Timing and Noise Estimation

In this section, we experimentally show distributions of capacitance extraction errors, translating them to delay and crosstalk noise estimation errors. Translations have been achieved using analytical equation models [10], [11].

3.1 Experimental Conditions

Figure 4 shows an equivalent circuit to translate the extracted total capacitance into delay [10]. This model consists of a constant voltage source, source resistance R_s, wire loads, and receiver gate capacitance C_{rcv}. Transient voltage at the receiver input is expressed with the following equation.

$$V(t) = V_{dd}\left(1 - e^{\frac{-t}{R_s(C_1+C_2)+R_{wire}C_2}}\right) \quad (1)$$

where, C_1, C_2 are, $C_1 = C_{wire}/2, C_2 = C_{wire}/2 + C_{rcv}$, respectively. C_{wire} is the total interconnect capacitance. Here, we define delay as the transient time from $V_o = 0$ to $V_o = 0.5V_{dd}$ at the receiver input. From the standpoint of observing the range of the impact on delay, we set $C_{rcv} = 0$, which gives the maximum delay deviation for the same capacitance variation. Then, the delay T_{pd} is expressed as follows.

$$T_{pd} = 0.693(R_sC_{wire} + R_{wire}C_{wire}/2) \quad (2)$$

Figure 5 shows an equivalent circuit to translate extracted capacitances into crosstalk noise voltage [11]. Crosstalk noise peak voltage V_{peak} is express using the following equation.

$$V_{peak} = \frac{(R_{v1}+R_{v2})C_cV_{dd}}{\tau_v}\left(\frac{\tau_v}{\tau_a}\right)^{-\frac{\tau_a}{\tau_v-\tau_a}} \quad (3)$$

where, τ_a, τ_v are time constants of the aggressor and victim net, expressed as follows.

$$\tau_a = R_{a1}(C_{a1}+C_{a2}+C_c+C_{a3}) + R_{a2}(C_{a2}+C_c+C_{a3}) \quad (4)$$

$$\tau_v = R_{v1}(C_{v1}+C_{v2}+C_c+C_{v3}) + R_{v2}(C_{v2}+C_c+C_{v3}) + R_{v3}C_{v3} \quad (5)$$

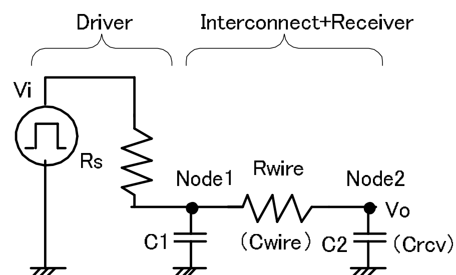


Fig. 4 Equivalent circuit to translate capacitance into delay.

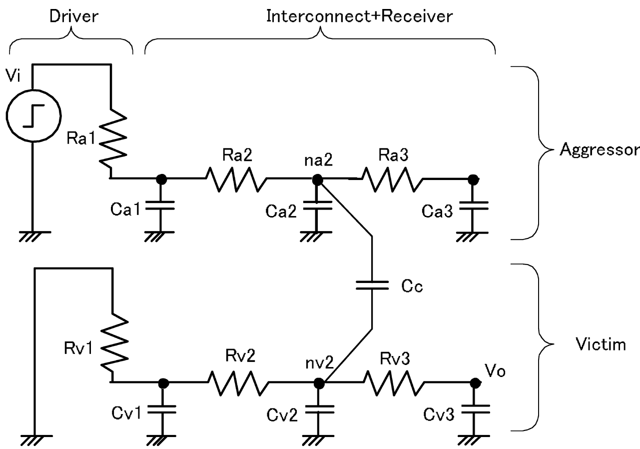


Fig. 5 Equivalent circuit to model crosstalk noise.

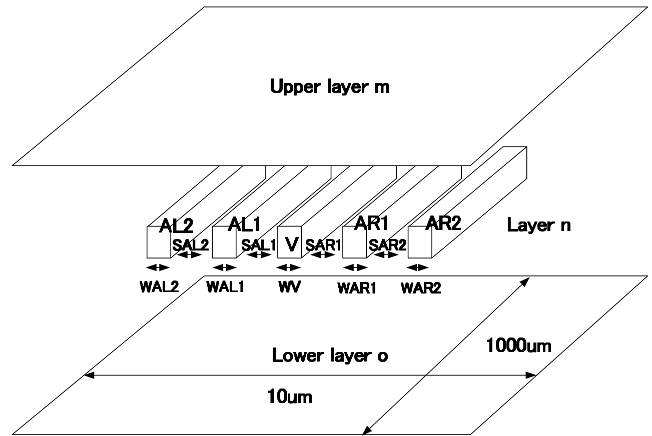
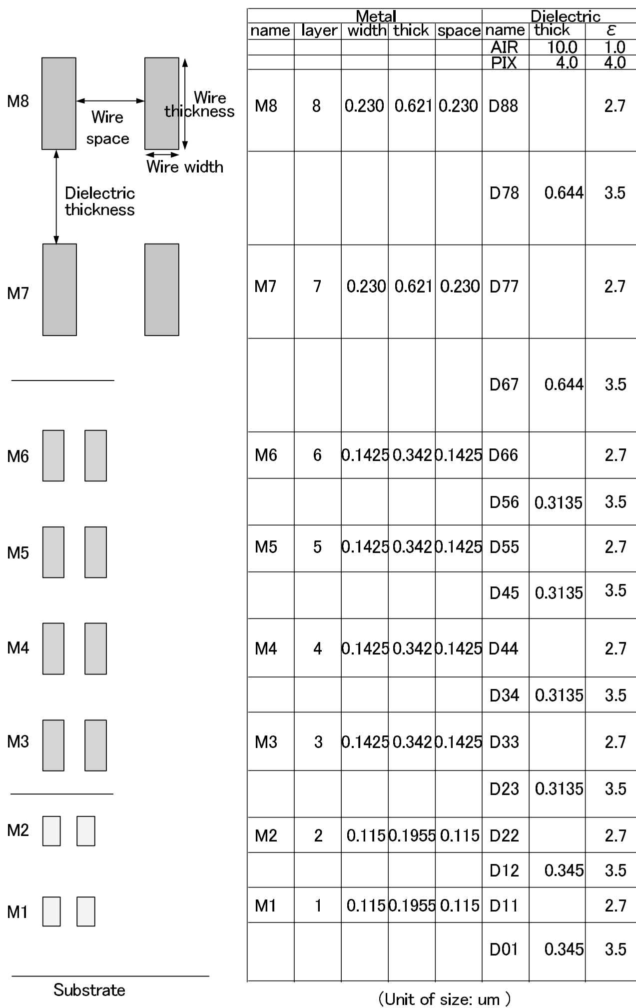


Fig. 7 Structures for testing 2-dimensional primitives.



Metal					Dielectric		
name	layer	width	thick	space	name	thick	ε
					AIR	10.0	1.0
					PIX	4.0	4.0
M8	8	0.230	0.621	0.230	D88		2.7
					D78	0.644	3.5
M7	7	0.230	0.621	0.230	D77		2.7
					D67	0.644	3.5
M6	6	0.1425	0.342	0.1425	D66		2.7
					D56	0.3135	3.5
M5	5	0.1425	0.342	0.1425	D55		2.7
					D45	0.3135	3.5
M4	4	0.1425	0.342	0.1425	D44		2.7
					D34	0.3135	3.5
M3	3	0.1425	0.342	0.1425	D33		2.7
					D23	0.3135	3.5
M2	2	0.115	0.1955	0.115	D22		2.7
					D12	0.345	3.5
M1	1	0.115	0.1955	0.115	D11		2.7
					D01	0.345	3.5

(Unit of size: um)

Fig. 6 Interconnect cross-section used in our experiments.

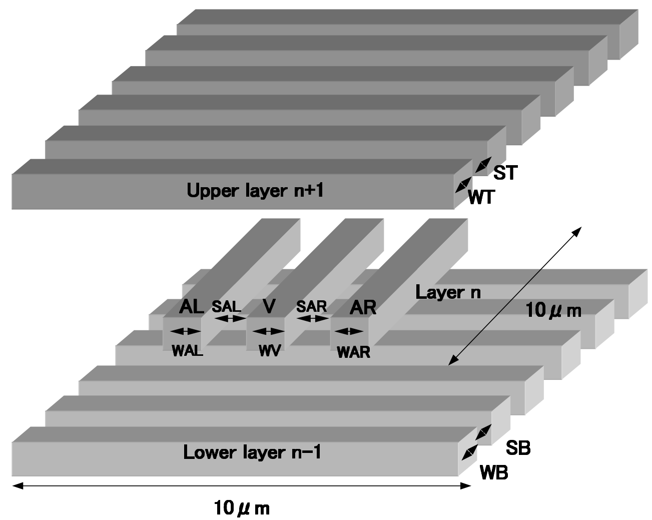


Fig. 8 Structures for testing 3-dimensional primitives.

From the standpoint of observing the range of impact on the noise peak voltage, we set $\tau_a = 0$, which gives the maximum crosstalk induced voltage deviation for the same capacitance variation.

In Fig. 6, we show an interconnect cross-section which is based on the ITRS [12] 2000 update SoC 100 nm node and used for our experiments. As a typical layer allocation, we assigned M1 and M2 to local interconnect layers, M3-M6 to intermediate layers, and M7-M8 to global layers, respectively. Along with the capacitive parameters, the source resistance of a minimum gate is set to 3.5 kΩ, and the conductivity value of copper is applied to every interconnect layer.

Test structures to observe capacitance extraction errors of 2-dimentional and 3-dimentional primitives are shown in Figs. 7 and 8, respectively. These patterns are based on HVH routing and included in the primitive libraries. In the 2D structure, effects of the second neighbors $AL2$ and $AR2$ are observed, varying the upper and lower layers as the first and second adjacent layers, i.e., $m = \{n+1, n+2\}$, and $o = \{n-1, n-2\}$. Here, most of the LPE tools do not directly extract coupling capacitance between the second neighbor

wires. On the other hand, the 3D structure is chosen such that the effects of crossing interconnect in the adjacent upper and lower layers are observed. For these structures, Raphael [8] 2D and 3D, two- and three-dimensional programs for solving Poissons's equation, are executed as the reference, setting the number of meshes so that the deviation of the resulting capacitance becomes less than 0.5%. Width and spacing of wires are varied as ×1, ×2, ×3 of minimum size. To randomize the parameters, each set of values is assigned using the 9-factor 3-level design table (L27) [13]. Layers *m*, *n*, *o* in Fig. 7 are allocated to cover every different combination of "local," "intermediate," and "global" layers. A total of 432 and 108 different patterns are used in the experiments as 2D and 3D structures, respectively.

3.2 Experimental Results

Experiments have been applied using 3 commercial LPE tools, Sequence Columbus-AMS [4], Synopsys Star-RCXT [5], and Cadence Fire&Ice QXC [6]. In this section, we show results from typical cases, while the other cases showed closely similar behavior.

Table 1 shows statistical data of the extracted capacitances, where σ is the standard deviation. As a result, values of σ are comparable with the variation of plate capacitance reported based on the actual measurement of TEG [1]. Figures 9 and 10 show the impact on delay, and Figs. 11 and 12 show the impact on crosstalk noise. In each graph, an additional histogram assuming the normal distribution is plotted using the values of average and variance. As shown in these figures, the experimental results correspond to the normal distribution very well. Table 2 shows a summary of the im-

Table 1 Extracted capacitances.

Item		2D	3D
Total capacitance	Average (F)	1.68E−13	1.74E−13
	σ of relative error (%)	0.38	1.58
	σ of absolute error (F)	6.24E−16	2.86E−15
Coupling capacitance	Average (F)	2.81E−14	4.33E−14
	σ of relative error (%)	5.69	5.12
	σ of absolute error (F)	1.58E−15	2.27E−15

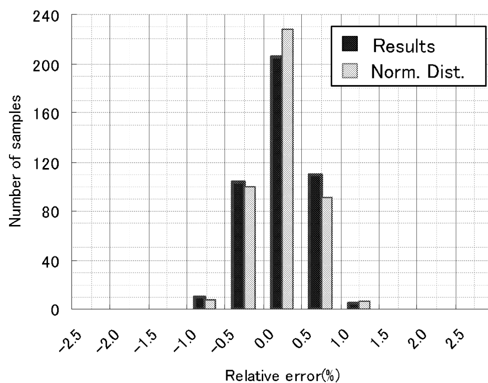


Fig. 9 Delay time error variation (2-dimensional).

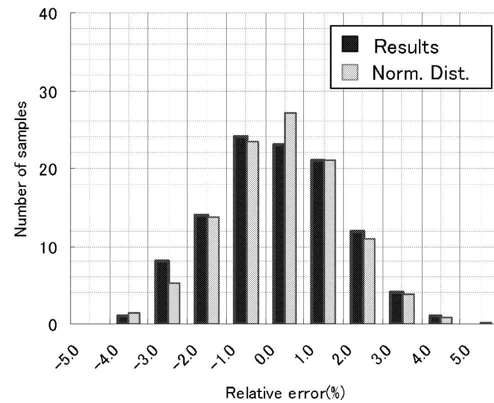


Fig. 10 Delay time error variation (3-dimensional).

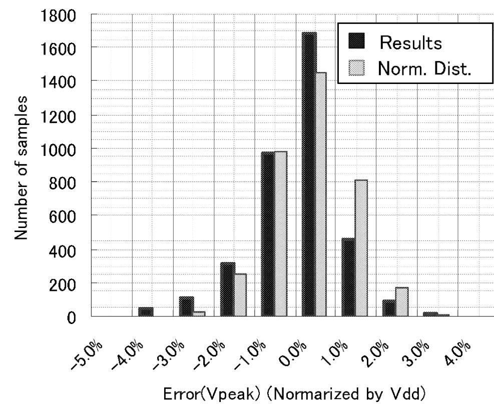


Fig. 11 Crosstalk noise error variation (2-dimensional).

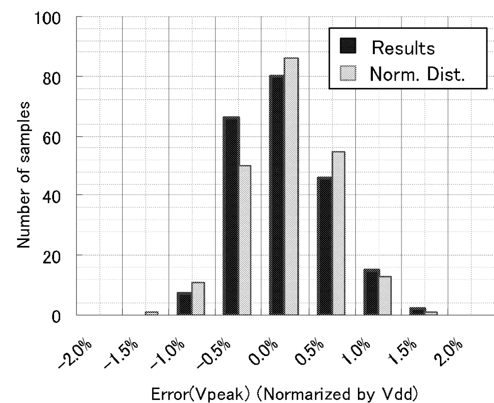


Fig. 12 Crosstalk noise error variation (3-dimensional).

Table 2 Error distribution.

Item	Pattern	3σ(%)
Delay	*2D*	1.13
	3D	4.74
Voltage of crosstalk noise	*2D*	3.04
	3D	1.50

pact as values of 3σ. Focusing on delay, 3D patterns show larger deviations of error compared to 2D, due to 3D effects of the crossing wire arrays. As for the voltage of crosstalk noise, on the other hand, 2D patterns show larger deviations of error than 3D. This implies that the second neighbors have larger influences than the vertical neighboring layers for individual coupling noises.

4. Conclusion

In this letter, we have shown the impact of the intrinsic errors on timing and crosstalk noise estimation. We experimentally show that the resulting delay and noise estimating errors follow a normal distribution. Values of the standard deviations will help designers to consider the intrinsic error compared with other factors of variations.

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