Post-Layout Transistor Sizing for Power Reduction in Cell-Based Design

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Abstract— We propose a transistor sizing method that down-sizes MOSFETs inside a cell to eliminate redundancy of cell-based circuits as much as possible. Our method reduces power dissipation of detail-routed circuits while preserving interconnects. The effectiveness of our method is experimentally evaluated using 5 circuits. The power dissipation is reduced by 77% maximum and 65% on average without delay increase.

I. Introduction

Cell-base design has a well-established framework for the development of ASICs, and has been widely adopted. On the other hand, cell-based circuits inherently contain redundancy, for example, in power dissipation. In this paper, we propose a post-layout transistor sizing method for power reduction. Our method aims to reduce the redundancy of cell-base design and to obtain high performance circuits close to full-custom quality while keeping the cell-base design framework. We down-size MOSFETs inside a cell continuously, and generate the corresponding cell layout on the fly. The cell layout generation system used in our method does not change the location of input and output pins while the transistor widths inside a cell are varied[1]. Exploiting this feature, we can optimize detail-routed circuits, without any modifications of interconnects, using the precise wire capacitance values extracted from the detail-routed circuits.

Many transistor sizing methods for delay and power optimization have been proposed[2, 3, 4, 5, 6]. These methods need to derive the delay time of each cell at any MOSFET size. Refs.[2, 3, 4] utilize Elmore delay model. In this delay model, we can get the optimal solution of the problem formulated using a simple variable-transformation method. However, the accuracy of the delay model is not high enough, and hence the optimized circuits may violate the delay constraints. In Refs. [5, 6], the cell delay is approximated as a linear function of the cell size, and transistor sizing is formulated as a linear optimization problem. This method also can obtain the optimal solution of the formulated problem. However, the linearization of the cell delay may introduce errors in timing analysis.

Recently, the delay time due to wire capacitance occupies a considerable part of the total circuit delay. Many of the previous transistor sizing methods[2, 3, 5, 6] concentrate on circuit-level optimization, and the consideration on layout is not enough. When the optimization result is applied to the layout, routing is affected, i.e. wire capacitances in the resulting layout become different from the initial circuit before transistor sizing. The variation of wire capacitance may cause a violation of delay constraints. In Ref. [4], transistor sizing, re-routing and compaction techniques are performed to the circuit repeatedly for better consideration on layout. In a DSM process, coupling capacitances between adjacent interconnects in the same metal layer or two successive metal layers become dominant. The accurate capacitance evaluation of all the interconnects influenced by re-routing and compaction becomes computationally intensive and hence the repeated evaluation inside the optimization loop may become impractical.

Our method handles detail-routed circuits designed in a cell-base design style. Our method down-sizes MOSFETs inside a cell for power reduction without any modifications of wiring using accurate values of wire capacitance. We use a cell layout generation system called VARDS[1] that can generate cell layout with variable transistor width while keeping the location of terminals unchanged. In order to get the accurate cell delay time, our method utilizes four-dimensional look-up tables with four variables; gate widths of PMOS and NMOS transistors, input transition time, and load capacitance.

This paper is organized as follows. Section II explains the post-layout transistor sizing method. Cell layout generation, cell delay model, and transistor sizing algorithms are discussed. Section III demonstrates some experimental results. Finally, Section IV concludes the discussion.

II. Post-Layout Transistor Sizing

In this section, we explain a transistor sizing method for power reduction preserving interconnects. We first discuss cell layout generation for post-layout transistor sizing. Next, we show a cell delay model that can calculate delay time for any PMOS and NMOS transistor sizes. Then, the noise margin constraints that guarantee the correct behavior of the circuits are discussed. Finally, we explain a transistor sizing algorithm for power reduction.

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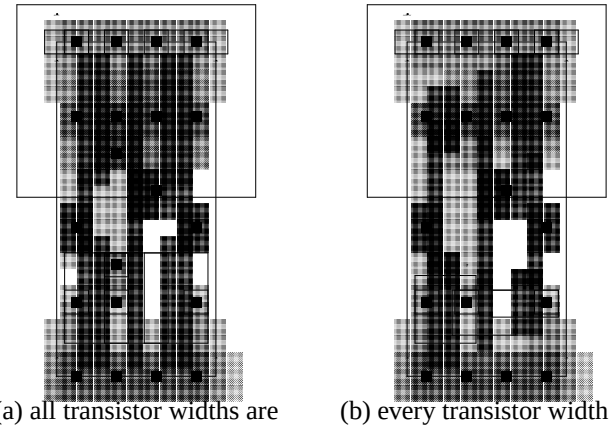


(a) all transistor widths are the maximum.

(b) every transistor width is different.

Figure 1: Examples of AOI21 Cell Layout.

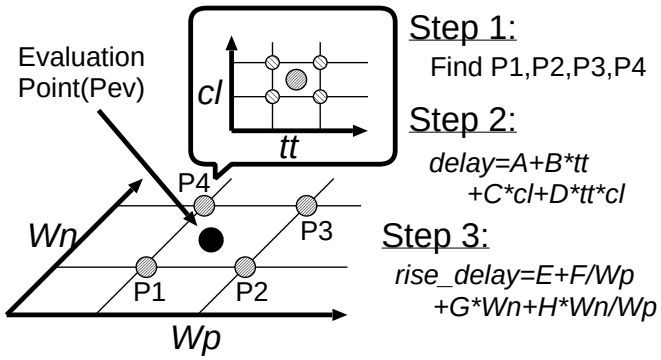


Figure 2: Derivation of Cell Delay.

A. Cell Layout Generation

In order to apply the optimization result to the layout without any modifications of interconnects, the following features are required for cell layout generation.

- Each transistor width can be varied easily and flexibly.
- The location of each pin is fixed even when transistor widths are varied.

The fixed locations of input/output pins are needed to preserve interconnects. A cell layout generation system VARDS, which satisfies the above two requirements, has been proposed[1]. Fig. 1 shows an example of AOI21 cells whose height is 9 interconnect pitches. The AOI21 cell in Fig. 1(a) is generated such that all transistor widths are the maximum. Fig. 1(b) is an example that every transistor width is different.

B. Cell Delay Model

In the proposed method, PMOS and NMOS transistors inside a cell are resized separately. Our method hence requires a cell delay model that has four variables, W_p, W_n, tt, and cl, where $W_p(W_n)$ is the gate width of PMOS(NMOS) transistor, tt is the transition time of the input signal, and cl is the capacitive load. We build four-dimensional look-up tables with four variables W_p, W_n, tt, and cl beforehand using a circuit simulator. Cell delay time is derived from the look-up tables using the following three-step interpolation(Fig. 2). In the case of a multi-stage cell, we divide the cell into single-stage cells, and calculate the delay time of each single-stage cell.

Step1: Find four neighboring points($\mathrm{P}_1, \mathrm{P}_2, \mathrm{P}_3, \mathrm{P}_4$) around the evaluation point(P_{ev}), in two-dimensional W_p-W_n space.

Step2: Calculate the delay time at each point of $\mathrm{P}_1, \mathrm{P}_2$, P_3, P_4 using Eq. (1) in two-dimensional tt-cl space .

Step3: Interpolate rise/fall delay time using Eq. (2/3) in W_p-W_n space from the four values at $\mathrm{P}_1, \mathrm{P}_2, \mathrm{P}_3, \mathrm{P}_4$ calculated at **Step2**.

$$delay = A + B \cdot tt + C \cdot cl + D \cdot tt \cdot cl, \quad (1)$$

$$rise\_delay = E + F \cdot \frac{1}{W_p} + G \cdot W_n + H \frac{1}{W_p} \cdot W_n, \quad (2)$$

$$fall\_delay = I + J \cdot W_p + K \cdot \frac{1}{W_n} + L \cdot W_p \frac{1}{W_n}, \quad (3)$$

$$energy = M + N \cdot W_p + O \cdot W_n + P \cdot W_p \cdot W_n, \quad (4)$$

where, $A, B, ..., P$ are coefficients to be determined such that the four values of the neighboring points are assigned to each interpolation equation. The transition time of the output signal is calculated similarly. In the case of the dissipated energy, Eq. (4) is used for the interpolation at **Step3**.

C. Noise Margin Constraints

Adequate amounts of noise margins are important to ensure the correct behavior of the circuits. The noise margins are defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. The noise margin depends on the ratio β_R, which is expressed as $\beta_n/\beta p$, where $\beta_{n(p)}$ is the n(p)-device transconductance. We calculate the range of β_R that guarantees proper noise margins. The upper bound $\beta_{R(max)}$ can be derived from the following two equations[7, 8].

$$V_{IL} = \frac{2V_{out} - V_{DD} + V_{Tp} + \beta_{R(max)} V_{Tn}}{1 + \beta_{R(max)}}, \quad (5)$$

$$\beta_{R(max)}(V_{IL} - V_{Tn})^2 = -(V_{out} - V_{DD})^2 + 2(V_{IL} - V_{DD} - V_{Tp})(V_{out} - V_{DD}). \quad (6)$$

Similarly, the lower bound $\beta_{R(min)}$ can be obtained from the following two equations.

$$V_{IH} = \frac{\beta_{R(min)}(2V_{out} + V_{Tn}) + V_{DD} + V_{Tp}}{1 + \beta_{R(min)}}, \quad (7)$$

$$\beta_{R(min)}[2(V_{IH} - V_{Tn})V_{out} - V_{out}^2] = (V_{IH} - V_{DD} - V_{Tp})^2, \quad (8)$$

where V_{Tp}, V_{Tn} are the threshold voltages of PMOS and NMOS transistors. We resize PMOS and NMOS transistors for power reduction within the range of $\beta_{R(min)} < \beta_R < \beta_{R(max)}$.

D. Transistor Sizing Algorithm

We device a transistor sizing algorithm for power reduction based on sensitivity calculation. Our algorithm executes iterative optimization that decreases δ_{size} gradually, where δ_{size} is a variable that represents the amount of transistor width reduced in a single iteration.

Step1: Set δ_{size} to an initial value.

Step2: If δ_{size} is smaller than a pre-defined value, the optimization procedure finishes.

Step3: At each cell, evaluate the sensitivity, i.e. the amount of power reduction when the transistor widths decrease by δ_{size}. If the violations of noise margin or transition time constraints occur, sensitivity calculation is not performed.

Step4: Select the cell with the best sensitivity. If there are no cells with positive sensitivity, halve δ_{size} and go back to **Step2**.

Step5: Decrease the transistor widths of the selected cell by δ_{size}, and update the timing information of the cells affected by the down-sizing. If delay violation occurs, cancel the down-sizing.

Step6: Find the cell with the next best sensitivity. If there are no cells with positive sensitivity, go back to **Step3**. Otherwise, go back to **Step5**.

First, the above algorithm is executed for power reduction such that PMOS and NMOS transistors are resized simultaneously with the same β_n/β_p ratio. We next optimize power dissipation resizing PMOS and NMOS transistors independently, and we then get the final optimization result.

III. Experimental Results

In this section, some experimental results are shown. We first demonstrate the accuracy of the cell delay model based on look-up tables. We next show the power optimization results.

We generate cell layouts using VARDS[1] in a 0.35μm process with three metal layers. The cell height is 13 interconnect-pitches, and the size ratio of PMOS and NMOS transistors is 1. In transistor sizing, we down-size MOSFETs within the range that VARDS can generate cell layouts. The maximum transistor width of standard driving-strength(x1) cells is 6.2μm, and the value of W/L is 15.5. The transistor width can be reduced to 0.9μm. Reference [9] reports that the optimal value of W/L around 20. The transistor width of our library is smaller than the reported value.

A. Accuracy of Cell Delay Model

We first examine the accuracy of the cell delay model. We use INV, 2-input NAND and 2-input NOR cells of standard driving-strength(x1) for this experiment. In the case of NAND and NOR cells, we evaluate the characteristics of the input pin that is close to the output terminal. We compare the delay time derived by the interpolation in Sec. II. B with the delay time evaluated by circuit simulation at the following 6561 points. The gate widths of PMOS and NMOS transistors (W_p, W_n) are varied to 0.9, 1.2, 1.5, 2.0, 2.5, 3.2, 4.0, 5.0, and 6.2μm, respectively. The evaluation points of the input transition time (tt) are 0.02, 0.125, 0.25, 0.375, 0.5, 0.65, 0.8, 1.0, and 1.2ns, also the points of load capacitance (cl) are 0.005, 0.025, 0.05, 0.075, 0.1, 0.15, 0.2, 0.35 and 0.5pF. The combinations of W_p and W_n that the noise margin becomes smaller than $0.25V_{DD}$ are excluded. When the absolute value of the delay time is extremely small, the relative error becomes meaninglessly large while absolute error is sufficiently small. We hence do not calculate the relative error when the delay time is less than 0.01ns. The size of look-up tables is 5x5x5x5. Table 1 shows the error of the cell delay model. The interpolation error of the delay time derived in W_p-W_n space is comparable with the error calculated in tt-cl space. We therefore can see that the interpolation in W_p-W_n space by Eqs. (1) and (2) is reasonable. The average error of the delay time calculated from 4-dimensional look-up tables of W_p, W_n, tt, and cl is less than 2%. Compared with the interpolation in tt-cl space, the average error increases by 0.5%.

Table 1: Average Error of Cell Delay Model Based on Look-up Tables.

Cell	Transition	Variables of Interpolation		
		W_p, W_n, tt, cl	tt, cl (W_p, W_n fixed)	W_p, W_n (tt, cl fixed)
INV	rise	0.003ns 1.9%	0.002ns 1.4%	0.001ns 1.0%
	fall	0.004ns 1.3%	0.002ns 0.9%	0.002ns 0.4%
NAND2	rise	0.003ns 2.1%	0.002ns 1.5%	0.001ns 0.9%
	fall	0.005ns 1.0%	0.002ns 0.6%	0.003ns 0.4%
NOR2	rise	0.002ns 1.2%	0.001ns 0.8%	0.001ns 0.6%
	fall	0.005ns 1.2%	0.002ns 0.7%	0.003ns 0.5%

B. Power Optimization Results

We show the results of power optimization. The circuits used for the experiments are an ALU in a DSP for mobile phone[11] (dsp_alu) and the circuits included ISCAS85 and LGSynth93 benchmark sets (C3540, alu4, C7552, des). These circuits are synthesized under two different constraints [10]: minimizing the circuit delay, and minimizing the circuit area. Also two transition time constraints, 0.5ns and 1.0ns are given. Thus, each circuit is synthesized under four different constraints in total. We generate the layouts of the synthesized circuits and utilize the wire capacitance values extracted from the layouts for transistor sizing. The circuit scale is 943 to 12460 cells. The cell library used for generating initial circuits includes six varieties in driving-strength for INV and

BUF (x1, x2, x3, x4, x6 and x8). In the case of NAND2, NAND3, AND2, AND3, NOR2, NOR3, OR2, OR3, AOI21, OAI21 cells, there are four varieties(x1, x2, x3, x4). The circuit delay time is evaluated by a transistor-level static timing analysis tool[12], and the power dissipation is estimated by a transistor-level power simulator[13]. The input patterns are randomly generated with a transition probability of 0.5. The number of applied patterns is 100, which is the adequate number for power estimation at circuit level[14]. The cycle time of the input patterns is 100ns.

We optimize power dissipation under the delay constraints of the initial circuits' delay time. The initial value of δ_{size} in the optimization algorithm(Sec. II. D) is 12.4μm, and the termination value is 0.1μm. The constraints that the noise margin is larger than $0.25V_{DD}$ are given. Table. 2 shows the power optimization results. The column "Total Width" represents the sum of the gate widths of MOSFETs in the circuit. "CPU Time" represents the CPU time required for power optimization on an Alpha Station. Our method reduces power dissipation by 77% maximum and 65% on average. The total transistor width is reduced to 25% of the initial circuits. The power reduction in small circuits is larger than the one in large circuits, because large circuits usually have heavier wire load. In the case of the largest circuit dsp_alu, the power dissipation is reduced by about 50%. In some circuits, the circuit delay increases though the initial delay time is given as the delay constraints. One reason is that the optimized circuits become sensitive to the error of cell delay model[15]. Further examination of the reasons is required, considering the accuracy of the delay calculation tool as well.

We examine the optimization result of des circuit generated for minimizing circuit delay under the transition time constraint of 0.5ns. Fig. 3(a) shows a part of the initial layout. Fig. 3(b) corresponds to the transistor-sized layout of the same location. The transistor sizes inside cells become different in instance by instance. PMOS and NMOS transistors inside each cell are resized separately. Also the routing is perfectly preserved. Our method generates cell layouts on the fly according to the optimization results, and replaces cells without any interconnect modifications.

We first demonstrate the relationship between the amount of power reduction and the increase of driving-strength varieties. Halving δ_{size} in the optimization algorithm(Sec. II. D) corresponds to halving the intervals of driving-strength and increasing driving-strength varieties twofold. We classify the driving-strength varieties into 10 levels(Table 3). Fig. 4 indicates the relationship between power dissipation and driving-strength level. The power dissipation is reduced as the driving-strength varieties increase.

We next show the distributions of transistor widths in the optimized circuit(Fig. 5). The transistor width of a standard driving-strength(x1) cell is 6.2μm, and the transistor width can be reduced to 0.9μm. Many MOSFETs are down-sized close to the lower limit of 0.9μm. Compared with PMOS transistors, the gate widths of NMOS transistors are small. The sum of PMOS gate widths is 11.2mm, which is 19% larger than the sum of NMOS gate widths(9.4mm).

Table 3: Driving-Strength Level.

Level	#driving-strength varieties(INV)	δ_{size} (μm)	PN ratio
Level 0	6 (Initial)	-	-
Level 1	11	12.4	Fixed
Level 2	23	6.2	Fixed
Level 3	44	3.1	Fixed
Level 4	85	1.55	Fixed
Level 5	166	0.775	Fixed
Level 6	332	0.388	Fixed
Level 7	659	0.194	Fixed
Level 8	1314	0.097	Fixed
Level 9	1.7M	0.097	Varied

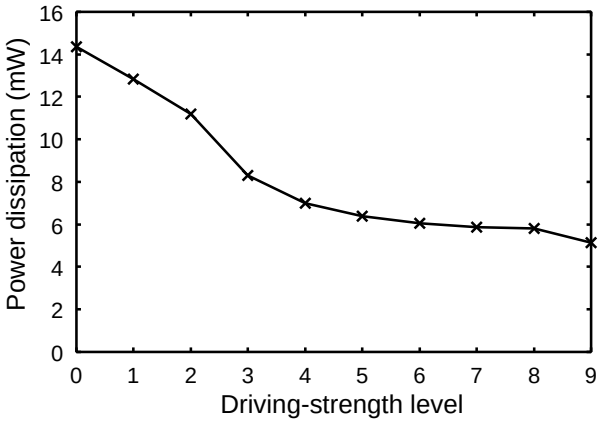


Figure 4: Relationship between Power Dissipation and Driving-Strength Varieties(des, Fastest, Transition Time Constraint 0.5ns).

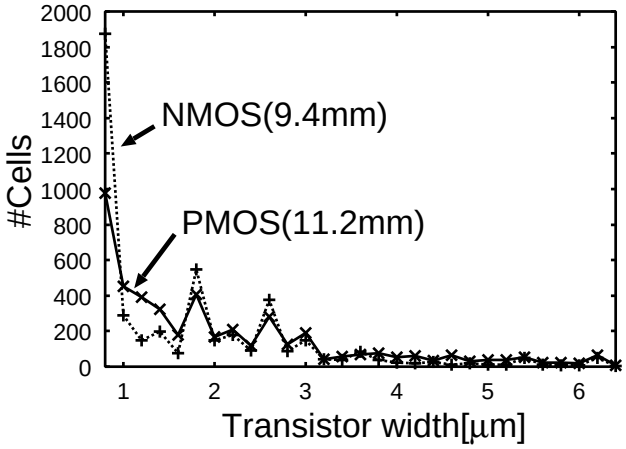
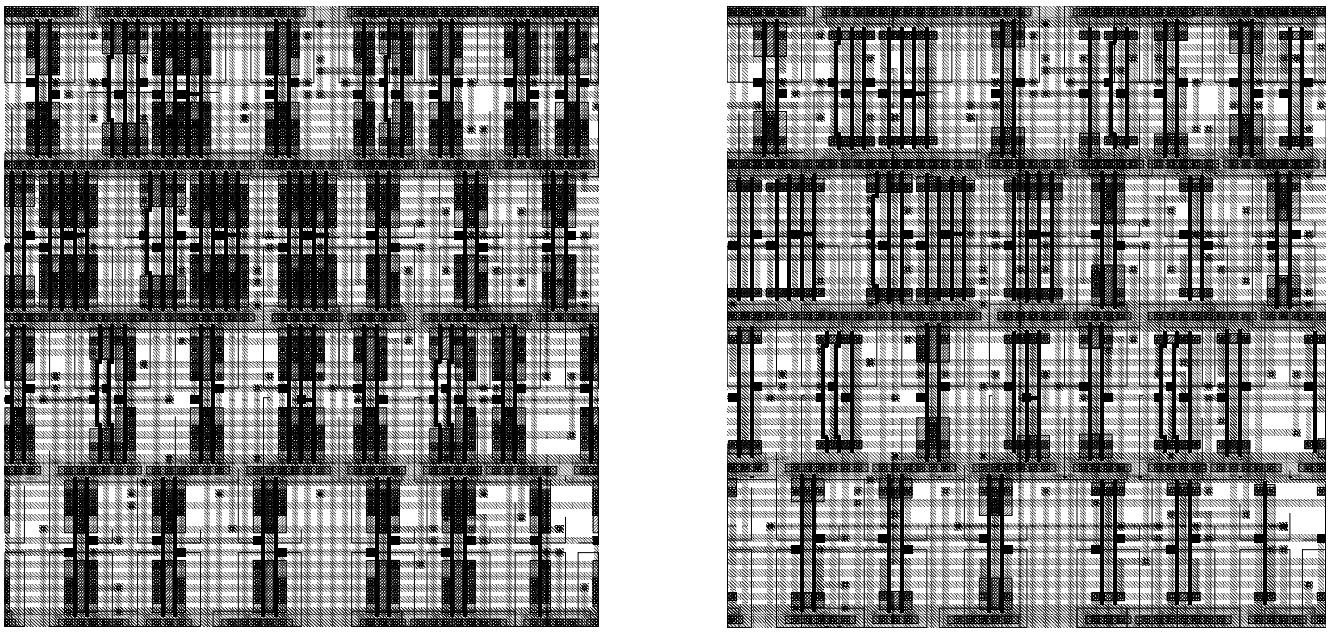


Figure 5: Distribution of Transistor Widths(des, Fastest, Transition Time Constraint 0.5ns).

Fig. 6 expresses the slack distributions of the initial and optimized circuits. By transistor sizing, the number of the cells with 0 or almost 0 slack increases drastically. The sum of slack in the optimized circuit is 1241ns, whereas the sum of slack in

Table 2: Power Optimization Results(Cell Height: 13 Interconnect Pitches).

Circuit	Transition Time Constraints (ns)	Design Constraints	Initial Circuits			Optimized Circuits				CPU Time (s)	#cells
			Delay (ns)	Power (mW)	Total Width (mm)	Delay (ns)	Power (mW)	Power Reduction (%)	Total Width (mm)		
C3540	0.5	Fastest	5.3	6.1	27.0	5.3	1.6	74	5.64	100	1039
		Min-Area	6.9	4.8	21.8	7.1	1.3	73	4.33	62	943
	1.0	Fastest	4.4	6.7	26.7	4.6	1.7	75	5.75	111	1207
		Min-Area	6.1	3.5	13.0	6.5	0.9	74	2.54	37	895
alu4	0.5	Fastest	2.9	5.1	42.6	3.1	1.9	63	12.6	213	1613
		Min-Area	4.0	4.2	33.8	4.1	1.4	67	8.70	145	1403
	1.0	Fastest	2.2	4.6	33.2	2.5	1.9	59	10.4	200	1568
		Min-Area	3.6	3.1	18.7	3.7	1.1	65	4.53	76	1361
C7552	0.5	Fastest	4.2	14.5	49.0	4.4	3.4	77	9.74	279	1995
		Min-Area	6.2	12.7	37.0	6.5	3.0	76	7.00	160	1687
	1.0	Fastest	3.3	14.1	44.6	3.5	3.2	77	9.21	275	2043
		Min-Area	5.1	8.5	22.1	5.1	2.1	75	4.38	97	1619
des	0.5	Fastest	3.2	14.4	84.7	3.4	5.1	65	20.6	925	3414
		Min-Area	4.2	11.1	63.4	4.5	4.3	61	15.3	560	2908
	1.0	Fastest	2.7	13.4	68.0	2.8	5.3	60	18.8	772	3327
		Min-Area	3.4	8.5	41.1	3.7	3.7	56	10.6	371	2859
dsp_alu	0.5	Fastest	8.8	79.8	347	9.4	37.1	54	115	20304	12547
		Min-Area	18.1	75.9	299	17.7	39.9	47	109	15436	11765
	1.0	Fastest	7.2	66.2	235	8.1	28.2	57	65.7	9203	12460
		Min-Area	15.3	54.3	169	15.8	26.3	52	44.9	4831	10892
Average	-	-	-	-	-	-	-	65	-	-	-



(a) Initial Circuit (b) Optimized Circuit

Figure 3: A Part of Layout(des, Fastest, Transition Time Constraint 0.5ns).

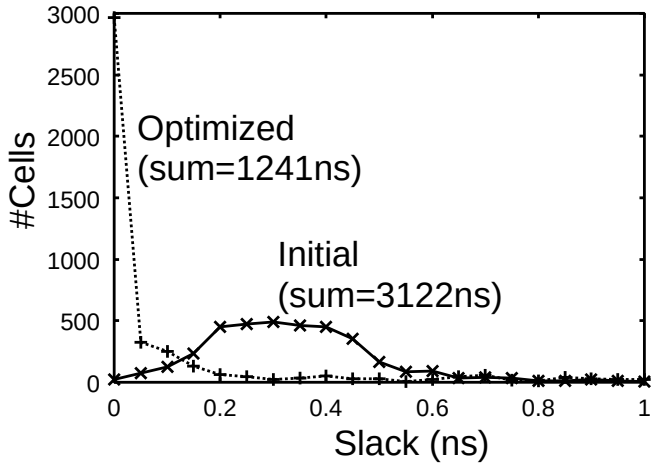


Figure 6: Distribution of Slack(des, Fastest, Transition Time Constraint 0.5ns).

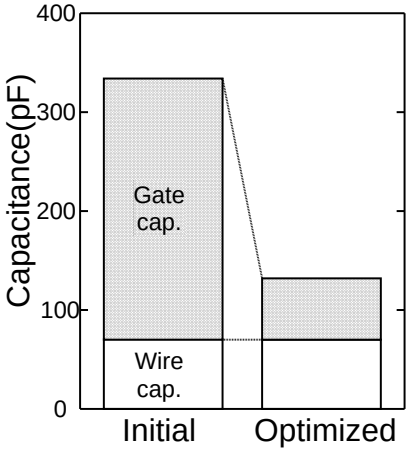


Figure 7: Capacitance Reduction(des, Fastest, Transition Time Constraint 0.5ns).

the initial circuit is 3122ns. The total slack is reduced by 60%.

We then demonstrate the capacitance reduction in the circuit(Fig. 7). Our method does not modify any interconnects, so wire capacitance does not change. The gate capacitance of MOSFETs is reduced by 77%, which results in 61% reduction of the total capacitance.

We show the peak current reduction. We apply 100 input patterns, and evaluate the peak current at each time-step within a cycle. Fig. 8 indicates the peak current of the initial and optimized circuits. The horizontal axis represents the time within a cycle of 3.4ns. The peak current is reduced by 74%. Path-balancing effect of our method contributes to the peak current reduction, as well as gate capacitance reduction. The transition timing of each cell is well distributed throughout a cycle. Reducing the peak current is effective to avoid IR drop problem. Also, the current reduction is a useful way to evade electromigration. The mean time to failure(MTF) of electromigration t_f is expressed as follows[16].

$$t_f = AW^p L^q J^{-n} exp(E_a/kT), \quad (9)$$

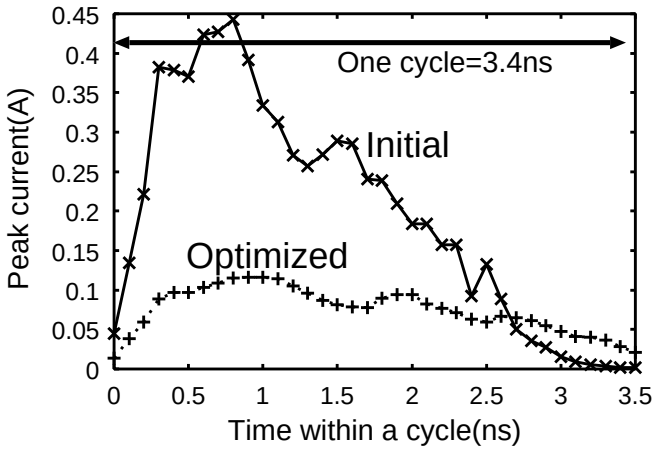


Figure 8: Peak Current Reduction(des, Fastest, Transition Time Constraint 0.5ns).

where J is current density, E_a is activation energy, W is the width of metal, L is the length, and n is a constant close to 2. The current reduction of 74% increases MTF 15 times. Thus, our method can increase the tolerance to IR drop and electromigration problems, and contribute to high-reliability LSI design.

We finally show the power optimization results when the initial circuits are generated using a low-power cell library. The delay time of each initial circuit is given as the delay constraint. The cell-height of this low-power library is 9 interconnect pitches, and the standard transistor size is 3.4μm. The results are shown in Table 4. Even when the low-power cell library is used for initial circuits, our method reduces power dissipation by more than 50% on average.

C. Effectiveness of Interconnect Preservation

The proposed method optimizes a detail-routed circuit without any wiring modifications. We verify the effectiveness of the interconnect preservation. In a conventional transistor sizing method, the layout is modified using an ECO(Engineering Change Order) technique in order to preserve the placement and wiring as much as possible. But a certain amount of variation in wire capacitance is not avoidable.

We examine the effect of this capacitance variation statistically. We assume that the wire capacitance varies according to a normal distribution N(m, σ) because of interconnect modifications, i.e. ECO. The mean m is the initial value used in transistor sizing, and the standard deviation σ is 20% of the initial value. The delay distribution is obtained using a Monte Calro technique. The number of delay evaluation is 10,000. Fig. 9 shows the delay variation in the optimized des circuit. As you see, the interconnect modifications increase the circuit delay. The circuit whose delay time is the same with the initial circuit(3.36ns) can be hardly obtained. The circuit delay of "mean+3σ" is 3.60ns, which is larger than the delay without wiring modifications by 7%. The proposed method can avoid this delay increase, thanks to the interconnect preservation.

Table 4: Power Optimization Results (Cell Height: 9 Interconnect Pitches).

Circuit	Transition Time Constraint (ns)	Design Constraint	Initial	Optimized	
			Power (mW)	Power (mW)	Power Reduction (%)
C3540	0.5	Fastest	5.0	1.7	66
		Min-Area	2.8	1.2	57
	1.0	Fastest	4.6	1.7	63
		Min-Area	2.1	0.84	60
alu4	0.5	Fastest	3.8	1.9	50
		Min-Area	2.7	1.4	48
	1.0	Fastest	3.5	1.8	49
		Min-Area	2.0	0.98	51
C7552	0.5	Fastest	11.0	3.9	65
		Min-Area	7.4	2.9	61
	1.0	Fastest	9.8	3.3	66
		Min-Area	5.5	2.2	60
des	0.5	Fastest	10.0	4.8	52
		Min-Area	6.9	4.0	42
	1.0	Fastest	10.9	5.2	52
		Min-Area	5.2	3.1	40
dsp_alu	0.5	Fastest	55.5	31.7	43
		Min-Area	52.2	34.0	35
	1.0	Fastest	45.5	23.7	48
		Min-Area	36.9	24.4	34
Average	-	-	-	-	52

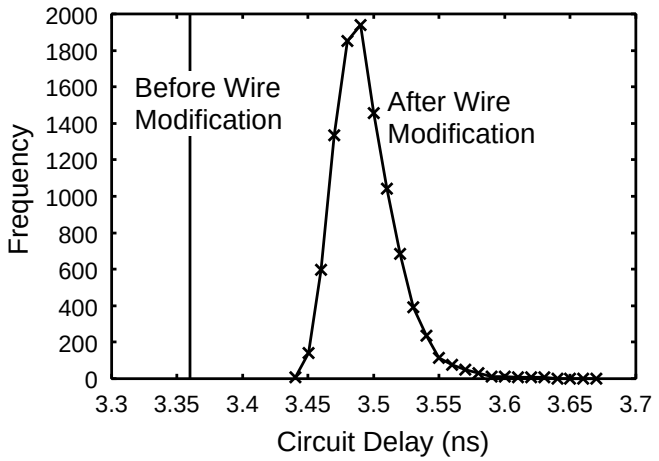


Figure 9: Delay Variation Caused by Interconnect Modifications(des, Fastest, Transition Time Constraint 0.5ns).

IV. Conclusion

We propose a power reduction method that down-sizes MOSFETs in a cell without any interconnect modifications. The effectiveness of our method is experimentally verified using 5 benchmark circuits. The power dissipation is reduced by 77% maximum and 65% on average without delay increase. We verify that our method also contributes to high-reliability LSI design.

Acknowledgments

This work is supported in part by Semiconductor Technology Academic Research Center (STARC).

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