INCREASE IN DELAY UNCERTAINTY BY PERFORMANCE OPTIMIZATION

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ABSTRACT

This paper discusses a statistical effect of performance optimization to uncertainty in circuit delay. Performance optimization has an effect of balancing the delay of each path in a circuit, i.e. the delay of long paths are shortened and the delay of short paths are lengthened. In these path-balanced circuits, the uncertainty in circuit delay, which are caused by delay calculation error, manufacturing variability, fluctuation of operating condition, etc., becomes worse by a statistical characteristic of delay. Thus, a highly-optimized circuit may not satisfy delay constraints. In this paper, we demonstrate some examples that uncertainty in circuit delay is increased by path-balancing, and we then raise a problem that performance optimization increases statistically-distributed circuit delay.

1. INTRODUCTION

In VLSI design, many techniques for reducing circuit delay are utilized at each design phase in order to satisfy given timing constraints. For example, division into pipeline stages, clock scheduling, logic composition, technology mapping, gate/transistor sizing, buffer insertion, wire sizing and timing driven layout synthesis are used. These methods detect the longest path and optimize the circuit for reducing the longest path delay. Recently, reducing power dissipation becomes one of the most principal subject in VLSI design. Many performance techniques, including the methods mentioned above, are hence utilized not only for delay reduction but also for reducing power dissipation. In some of these methods, blocks/cells, where timing constraints are not tight, are slowed down to reduce power consumption. Therefore, performance optimization can be regarded as a operation that shortens long paths and lengthens short paths in a circuit. The delay times of many paths in a circuit are equalized by performance optimization. This equalization is called path-balance.

There are several sources that cause uncertainties in circuit delay time, such as error in delay calculation, manufacturing variability, and fluctuation of operating conditions. The error in delay calculation includes error of delay model, diversity in signal waveforms, extraction error of wire capacitance, and so on. The manufacturing variability consists of fluctuations in transistor characteristics and wire shapes. Also the operating condition, i.e. supply voltage and temperature, varies. Due to these sources of delay uncertainty, the delay time of each gate and wire is not a deterministic value. It necessarily has a certain probability distribution.

In the circuits optimized for performance enhancement, the delay uncertainty of each gate influences the circuit delay strongly. It is because a path-balancing operation increases the number of long paths that have possibilities to become the longest path. Due to the statistical characteristic of delay, the average value of statistically-distributed circuit delay becomes large when the number of long paths increases. This statistical effect is discussed in detail in Sec. 2 using a simple example. So far, this increase of statistically-distributed circuit delay caused by path-balancing has not been well discussed. Unless the statistical delay increase is considered properly, optimized circuits may not work well. In order to guarantee the circuit speed, we have to understand and handle the statistical effect of path-balancing operation.

In this paper, we examine the effect of path-balancing to uncertainty in circuit delay. The influence on circuit delay is experimentally evaluated under some sources of delay uncertainty. We raise a notice that performance optimization increases statistically-distributed circuit delay, and hence give a caution that we have to pay more attention to the statistical effect of path-balancing in order to guarantee circuit delay time, when circuits are optimized for performance improvement. We finally introduce and evaluate a statistical static timing analysis method that can calculate statistically-distributed circuit delay [1].

This paper is organized as follows. Section 2 explains the statistical characteristic of circuit delay time. Section 3 shows the reason why performance optimization increases statistically-distributed circuit delay. Section 4 demonstrates some experimental results of statistical delay analysis and discusses the statistical effect of path-balancing to circuit delay uncertainty. Finally, Section 5 concludes the discussion.

2. STATISTICAL CHARACTERISTIC OF CIRCUIT DELAY TIME

The circuit delay, which is the maximum path delay time in a circuit, $D_{circuit}$ is represented as follows.

$$D_{circuit} = \max_i D_i \ \ (i = 1, 2, ..., n), \qquad (1)$$

where D_i is the path delay time of the i-th path, and n is the number of the paths in the circuit.

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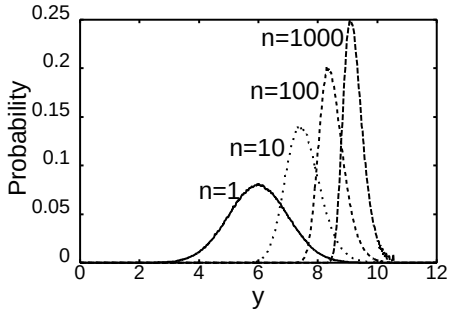

Figure 1: Effect of max operation(n is varied)

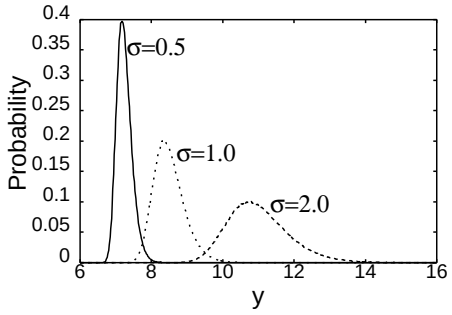

Figure 2: Effect of max operation(σ is varied)

Let us show a simple example of the statistical effect caused by the max operation.

$$y = \max_i x_i \ \ (i = 1, 2, ..., n). \tag{2}$$

Suppose that x_i is distributed according to a normal distribution N(6, 1). We examine the distribution of y under several values of n. Fig. 1 shows the distribution of y. When n increases, the average of y becomes large and the standard deviation of y becomes small. The increase of n corresponds to the increase of the number of long paths whose path delay times are close to the maximum path delay. From this example, we can see that the distribution of $D_{circuit}$ shifts to the right, i.e. in the direction that the circuit delay increases, when the number of the long paths increases.

We show another example. We fix n to 100, and vary the standard deviation σ of x_i. Fig. 2 shows the distribution of y. When the standard deviation of x_i increases, the average and the standard deviation of y becomes large. We can see that the average and the standard deviation of $D_{circuit}$ become large, when the standard deviation of x_i increases.

3. INCREASE IN CIRCUIT DELAY UNCERTAINTY BY PERFORMANCE OPTIMIZATION

Performance optimization generally consists of delay and power/area optimization. The delay optimization methods find long paths and optimize the circuit for reducing the longest path delay. Conversely, some of power/area optimization methods slow down the blocks/cells, where the given timing constraints are not tight, in order to reduce power dissipation, such as gate/transistor sizing [2–6], multiple supply voltage technique [7], multiple threshold voltage technique [8] and so on. Therefore, circuits are modified by performance optimization such that long paths are shortened and short paths are lengthened. This operation that the delay times of many paths in the circuit are equalized is called a path-balancing operation. Fig. 3 explains the concept of path-balancing.

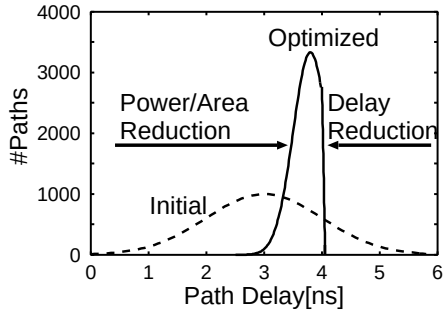

Figure 3: Path-Balancing Effect Caused by Performance Optimization

The path-balancing operation increases the number of the paths whose path delays are close to the maximum path delay(Fig. 3). These long paths have the possibilities of becoming the longest path in the circuit. So, the increase of the number of long paths corresponds to the increase of n in Fig. 1. Performance optimization therefore increases statistically-distributed delay by the statistical phenomenon shown in Fig. 1.

4. EXPERIMENTAL ANALYSIS

This section shows some experimental results of statistical delay analysis. We reveal that statistically-distributed circuit delay increases by path-balancing operation.

We use the ALU part of a vector processor(dsp_alu) [9] and the circuit(des) included in LGSynth93 benchmark set for the experiments. These circuits are synthesized and mapped by a commercial logic synthesis tool [10] under tight delay constraints. The target library is a standard cell library used for actual fabrication in a 0.35μm process with three metal layers. These circuits are placed and routed, and the wire capacitances are extracted from the layouts. We use these circuits as initial(not path-balanced) circuits. The number of gates used in dsp_alu and des are 14370 and 3837, respectively.

In order to obtain the path-balanced circuits, we utilize a transistor sizing method for performance optimization. We optimize the initial circuits by continuous transistor sizing for minimizing power dissipation under the delay constraint such that the delay does not increase from the initial value. The optimization method used for the experiments is a heuristic method that reduces power dissipation greedily based on the result of sensitivity analysis [6]. Figs. 4 and 5 represent the distributions of path delay in the initial and optimized circuits. The number of paths whose path delays are close to the longest path delay increases drastically, which corresponds to the increase of n in Fig. 1.

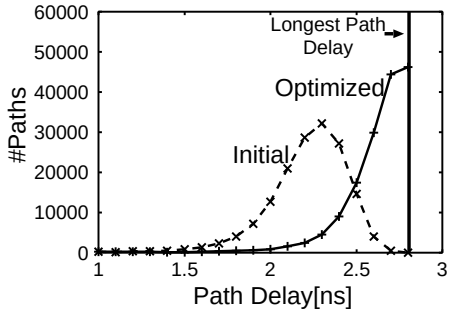

Figure 4: Distributions of Path Delay(des)

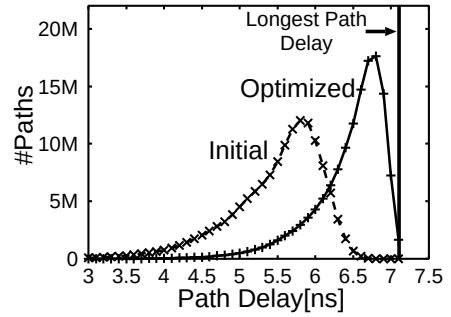

Figure 5: Distributions of Path Delay(dsp_alu)

4.1. Analysis of Delay Uncertainty

We first evaluate the impact of delay calculation error to the circuit delay uncertainty in the initial and optimized circuits. We assume an error model of gate delay such that the error of each gate is distributed according to a normal distribution with 3σ=10% of its typical(no error) delay. The distribution of circuit delay is obtained by a Monte Carlo analysis as follows. We assign delay fluctuation to each gate in the circuit randomly according to the given normal distribution, and evaluate the circuit delay using a static timing analysis technique. The number of delay evaluation is 10,000. The results are shown in Figs. 6 and 7. The bar labeled "Typical" represents the delay time calculated using the typical(no error) delay time for each gate. The statistically-distributed delay of the optimized circuit increases as we expected. In des circuit(Fig. 6), the average delay of the optimized circuit is 2.98ns, whereas the average of the initial circuit is 2.90ns. The average delay increases by 3% by path-balancing although the circuit delay calculated from the typical delay for each gate does not change after the optimization. Also, the delay distribution of path-balanced circuit moves far to the right of the typical delay. Therefore, in the case that the circuit is optimized considering only the typical delay, the statistically-distributed delay of the optimized circuit hardly satisfy the delay constraints.

Next, we examine the relationships between the accuracy of gate delay and the distribution of circuit delay. We assume three models of gate delay uncertainties such that each gate delay fluctuates normally with 3σ=5, 10 and 15% of its typical delay. In the case of a convex gate delay model for continuous transistor sizing, it is reported that 3σ of the estimation error in simple gates is 5 to 23% [11]. In this gate delay model, the error model of 3σ=15% might be a reasonable assumption. We guess that the model of 3σ=5% corresponds to the delay calculation using well-designed look-up tables characterized at many points (capacitive load, input transition time, transistor sizes). Fig. 8 expresses the distributions of circuit delay under three error models. As the value of 3σ increases, the average and standard deviation of the circuit delay distribution becomes large, which is the same phenomenon shown in Fig. 2. Compared with the initial circuits, the increase of the statistically-distributed delay in the optimized circuit is large. Even when the accurate delay model with 3σ=5% is used in performance optimization, there is a distinct delay difference between the statistically-distributed delay and the typical delay in the optimized circuit.

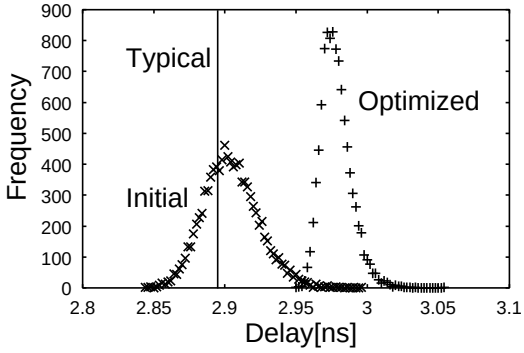

Figure 6: Circuit delay distributions under a delay error model of 3σ=10%(des)

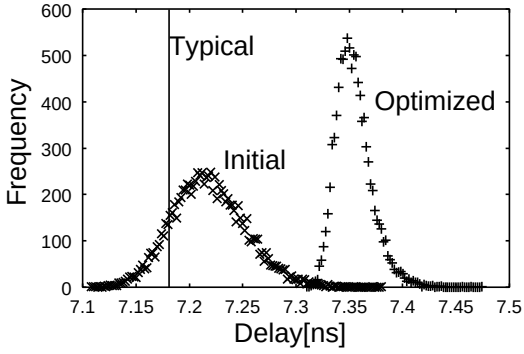

Figure 7: Circuit delay distributions under a delay error model of 3σ=10%(dsp_alu)

4.2. Worst-Case Delay Calculation

The increase of statistically-distributed circuit delay is different between the initial and the path-balanced circuits(Figs. 6, 7, 8). So, setting a design margin to avoid the delay violation is difficult and seems not to be a good way. To avoid this problem, statistical delay calculation [12] and the performance optimization based on statistical delay model [1, 13] are desired. We then apply the statistical static timing analysis(SSTA) method [1] to the initial and optimized circuits. The circuits and the error models

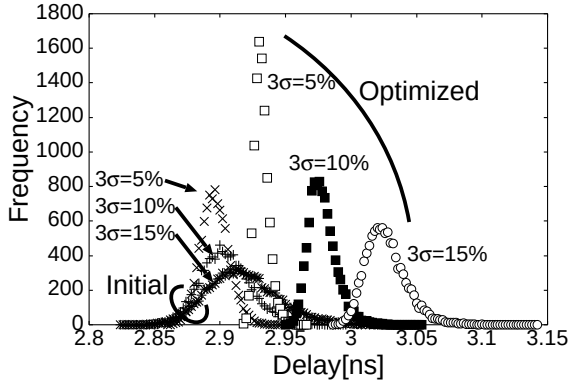

Figure 8: Circuit delay distributions under three delay error model of 3σ=5, 10, 15% (des)

Table 1: Accuracy of Statistical Static Timing Analysis in Worst-Case Delay Calculation

Circuit	3σ of Gate Delay Error (%)	Monte Carlo Worst-Case Delay (ns)	SSTA Worst-Case Delay(ns)	SSTA Error (%)
Initial	5	2.93	2.93	0.0
	10	2.97	2.97	0.0
	15	3.01	3.02	0.3
Optimized	5	2.96	2.96	0.0
	10	3.02	3.02	0.0
	15	3.09	3.10	0.3
Average	-	-	-	0.1

of gate delay are the same with those used in the previous experiment. We evaluate the worst-case delay D_{worst}. The worst-case delay D_{worst} is defined such that the probability of $D_{circuit} \leq D_{worst}$ becomes 99.87%, which corresponds to the value of $m + 3\sigma$ in a normal distribution.

Table 1 shows the accuracy of the statistical static timing analysis(SSTA) method [1]. The column "3σ of Gate Delay Error" represents the value 3σ of gate delay uncertainties. SSTA method computes the worst-case delay D_{worst} within 0.3% error, and the average error is 0.1%. SSTA method can calculate the worst-case delay accurately irrespective of the initial and the optimized circuits. Table 2 represents the comparison of CPU time needed to derive the worst-case delay. The column "Monte Carlo" corresponds to the Monte Carlo simulation whose number of delay evaluation is 10,000. Each CPU time is the average CPU time of six calculations shown in Table 1. SSTA method calculates the worst-case delay as more than three thousand times as fast as the Monte Carlo simulation with 10,000 delay evaluations. SSTA method requires only threefold CPU time of the Monte Carlo simulation whose evaluation number is one. In other words, SSTA needs threefold CPU time of the usual static timing analysis, although the average error of SSTA is 0.1%.

5. CONCLUSION

This paper examines the statistical effect of path-balancing operation to uncertainty in circuit delay. We demonstrate some examples that uncertainty in circuit delay is increased by path-balancing. We raise a notice that path-balancing increases uncertainty in circuit delay, and demonstrate a problem that a highly-optimized circuit may not satisfy delay constraints.

Table 2: CPU Time of Worst-Case Delay Analysis.

Monte Carlo		Statistical Static Timing Analysis
#evaluation: 10k	#evaluation: 1	
6044s	0.6s	1.9s

ACKNOWLEDGMENTS

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