Crosstalk Noise Estimation for Generic RC Trees

Masao Takahashi Masanori Hashimoto Hidetoshi Onodera
Dept. Communications & Computer Engineering, Kyoto University
{takahasi, hasimoto, onodera}@vlsi.kuee.kyoto-u.ac.jp

Abstract— **We propose an estimation method of crosstalk noise for generic RC trees. The proposed method derives an analytic waveform of crosstalk noise in a 2-π equivalent circuit. The peak voltage is calculated from the closed-form expression, and the crosstalk induced delay is estimated using the derived noise waveform. We also develop a transformation method from generic RC trees with branches into the 2-π model circuit. The proposed method can hence estimate crosstalk noise for any RC trees. Our estimation method is evaluated in a 0.13μm technology. The peak noise of two partially-coupled interconnects is estimated with the average error of 13%. Our method transforms generic RC interconnects with branches into the 2-π model with 14% error on average.**

I. Introduction

Crosstalk noise has become a critical problem in DSM LSI design. Recently, several crosstalk noise models are proposed. By solving telegraph equations, the analytical formula for peak noise is obtained [1, 2]. But these methods handle only fully-coupled interconnect structure, and can not be applied to general RC trees. In Refs. [3, 4], the aggressive wire and the victim wire are transformed into the L-type RC circuit, and the closed-form expressions of peak noise are obtained. However, the resistance of the interconnect is not well considered in this model. In DSM technology, the wire resistance is not negligible, and the coupling location becomes one of the important factor for crosstalk noise estimation. Reference [5] assumes that the input signal is a step function, which results in overestimation of noise voltage. Recently some estimation methods that can handle distributed RC network and saturated-ramp input signal are proposed [6, 7]. In Ref. [6], moment matching technique is utilized for deriving transfer functions. Moment matching technique requires high computational cost, and hence this method can not be used inside the optimization that needs to calculate crosstalk noise innumerably. Reference [8] reports that Ref. [7] overestimates crosstalk noise when the transition time of the aggressor is much larger than the victim net delay.

This paper proposes an estimation method of crosstalk noise for general RC trees. We develop a 2-π noise model with improved aggressor modeling. The 2-π noise model is first proposed in Ref. [8]. This model can consider the location of coupling, the effect of distributed RC networks and the slew of input signal, which are not well characterized in previous models [1–7]. However, in Ref. [8], the voltage waveform of the aggressor wire at the coupling point is approximate as a saturated ramp waveform. But in reality, the waveform is close to the exponential function, which yields estimation errors of crosstalk noise. Also the derivation of the slew of the ramp signal is not discussed. Another issue arises in the transformation of general RC trees to the 2-π noise model. Ref. [8] neglects the resistive shielding effect of the branches, which causes the underestimation of crosstalk noise. In addition, not all types of RC trees are discussed in Ref. [8]. In the proposed method, the exponential waveform is adopted as the signal of the aggressors for accuracy improvement of crosstalk noise estimation. The Elmore-like derivation method of the aggressive waveform is devised. We develop a transformation method that can apply all types of RC trees to the 2-π noise model considering the resistive shielding effect. Due to these advancements, the proposed method can estimate the crosstalk noise analytically for any RC trees.

This paper is organized as follows. Section 2 explains the modeling of crosstalk noise. Section 3 shows the transformation method of generic RC trees. Section 4 demonstrates some experimental results. Finally, Section 5 concludes the discussion.

II. Crosstalk Noise Modeling of Two Partially-Coupled Interconnects

This section explains the crosstalk noise modeling. The interconnect structure that two interconnects are partially coupled in Fig. 1 is considered. The partially-coupled interconnects in Fig. 1 are modeled as an equivalent circuit shown in Fig. 2. R_{v1} is the effective driver resistance of the victim net. The node n_{v2} corresponds to the middle point of the coupling interconnects. R_{v2} is the resistance between the source and n_{v2}, and R_{v3} is the resistance between n_{v2} and the sink. C_c is the coupling capacitance between the victim and the aggressor. The capacitances C_{v1}, C_{v2} and C_{v3} are represented as $C_1/2$, $(C_1 + C_2)/2$, and $C_2/2 + C_l$ respectively, where C_1 is the wire capacitance from the source to n_{v2}, C_2 is the wire capacitance from n_{v2} to the sink, and C_l is the capacitance of the receiver. The parameters of the aggressive wire, R_{a1}, R_{a2}, R_{a3}, C_{a1}, C_{a2}, C_{a3}, are determined similarly.

The proposed estimation method separates the victim net and the aggressive net into two equivalent circuits, as one of the approximate solutions for deriving a simple closed-form expression of noise waveform; the victim is represented as the circuit of Fig. 4, and the aggressor is Fig. 3. At the victim wire(Fig. 4), the aggressive wire is replaced as a voltage source. The model circuit of the victim interconnect in Fig. 4 becomes the same with the 2-π noise model proposed in Ref. [8], The proposed method approximates the signal of the aggressors as not a saturated-ramp but an exponential function for improving accuracy. We derive the analytic waveform expressions for the aggressors and the victim.

A. Aggressor Waveform

In the proposed crosstalk noise model, the voltage source of V_{agg} is assumed to be an exponential function. V_{agg} is expressed

0-7695-1200-3/01$10.00 © 2001 IEEE

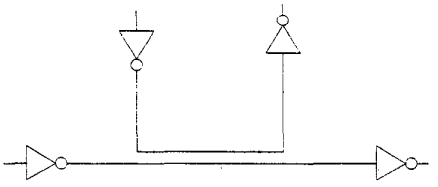

Fig. 1. Two Coupled Interconnects.

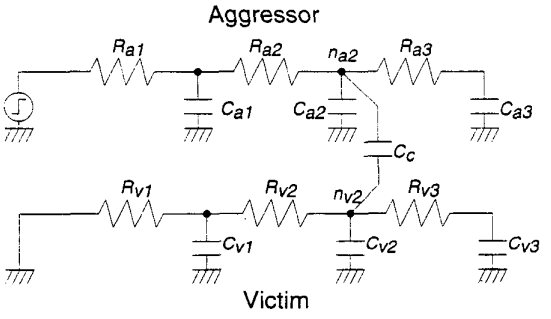

Fig. 2. An Equivalent Circuit of Two Partially-Coupled Interconnects for Crosstalk Estimation.

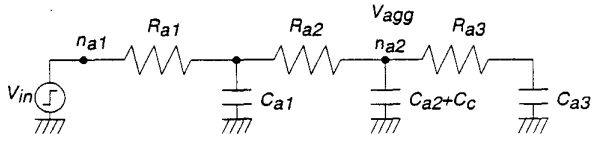

Fig. 3. Model of Aggressive Wire.

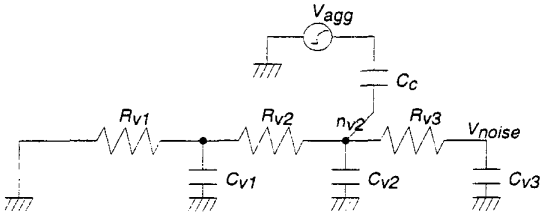

Fig. 4. Model of Victim Wire.

as follows.

$$V_{agg}(t) = V_{dd}\left(1 - e^{-t/\tau_a}\right) \quad \text{(time domain)}, \quad (1)$$

$$V_{agg}(s) = \frac{V_{dd}}{(\tau_a s + 1)s} \quad (s \text{ domain}). \quad (2)$$

Here, deriving the time constant τ_a, that is to say, the time constant at node n_{a2} in Fig. 3, is explained. In Elmore delay model, the delay time between node n_{a1} and node n_{a2}, $D_{1\to 2}$, is represented as follows [9].

$$D_{1\to 2} = R_{a1}(C_{a1} + C_{a2} + C_c + C_{a3}) + R_{a2}(C_{a2} + C_c + C_{a3}). \quad (3)$$

In lumped RC networks, RC product means the transition time that a signal changes from 0% to 63%. Therefore, $D_{1\to 2}$ corresponds to the time constant at node n_{a2}, i.e. τ_a.

$$\tau_a = R_{a1}(C_{a1} + C_{a2} + C_c + C_{a3}) + R_{a2}(C_{a2} + C_c + C_{a3}). \quad (4)$$

The relative inaccuracy of Eq. (4) increases as R_{a3} becomes large compared with R_{a1} and R_{a2}. This is because the capacitance C_{a3} is shielded by the resistance R_{a3}, and the effective capacitance of C_{a3} becomes small. In Ref. [10], a method to calculate an effective capacitance of RC networks is proposed. Using this method, the downstream network from node n_{a2} can be replaced by an effective capacitance C_{a3eff}. The effective capacitance C_{a3eff} is derived such that the amount of charge accumulated in C_{a3} and the amount of charge accumulated C_{a3eff} become the same until a time T, where T is the Elmore delay time from node n_{a1} to node n_{a2}. The effective capacitance C_{a3eff} is given by

$$C_{a3eff} = C_{a3}\left(1 - e^{-T/\tau_{dj}}\right), \quad (5)$$

$$T = R_{a1}(C_{a1} + C_{a2} + C_c + C_{a3}) + R_{a2}(C_{a2} + C_c + C_{a3}), \quad (6)$$

$$\tau_{dj} = R_{a3}C_{a3}. \quad (7)$$

Eq. (4) then becomes as follows.

$$\tau_a = R_{a1}(C_{a1} + C_{a2} + C_c + C_{a3eff}) + R_{a2}(C_{a2} + C_c + C_{a3eff}). \quad (8)$$

B. Analytic Waveform on Victim Interconnect

The analytic voltage waveform at the end of the victim net, that is to say, the waveform of crosstalk noise is derived in the 2-π victim wire model. In the circuit of Fig. 4, V_{noise} in s domain is represented as follows.

$$V_{noise}(s) = \frac{(R_{v1}R_{v2}C_{v1}s + R_{v1} + R_{v2})C_c s}{as^3 + bs^2 + ds + 1}V_{agg}(s), \quad (9)$$

where a, b, d are represented as follows.

$$a = R_{v1}R_{v2}R_{v3}C_{v1}(C_{v2} + C_c)C_{v3}, \quad (10)$$

$$b = R_{v1}C_{v1}(R_{v2}(C_{v2} + C_c + C_{v3}) + R_{v3}C_{v3}) + R_{v3}C_{v3}(C_{v2} + C_c)(R_{v1} + R_{v2}), \quad (11)$$

$$d = R_{v1}(C_{v1} + C_{v2} + C_c + C_{v3}) + R_{v2}(C_{v2} + C_c + C_{v3}) + R_{v3}C_{v3}. \quad (12)$$

Eq. (9) can be converted as follows.

$$V_{noise}(s) = \left(\frac{k_1}{s - s_1} + \frac{k_2}{s - s_2} + \frac{k_3}{s - s_3}\right)V_{agg}(s), \quad (13)$$

where the poles s_1, s_2, and s_3 are the roots of $as^3 + bs^2 + ds + 1 = 0$. When the relationship of $s_1 \ll s_2 \ll s_3$ is satisfied, the most dominant pole s_3 is represented as $1/d$. In this case, Eq. (13) can be approximated as follows.

$$V_{noise}(s) = \frac{(R_{v1} + R_{v2})C_c s}{\tau_v s + 1}V_{agg}(s), \quad (14)$$

where $\tau_v = d$. Using Eq. (2), Eq. (14) is converted as follows.

$$V_{noise}(s) = \frac{(R_{v1} + R_{v2})C_c V_{dd}}{(\tau_v s + 1)(\tau_a s + 1)}. \quad (15)$$

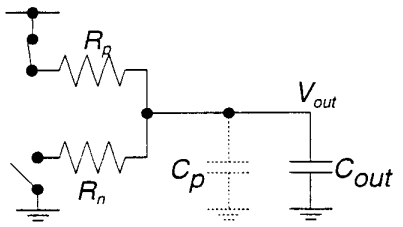

Fig. 5. Driver Model.

The equation of the noise voltage in time domain $V_{noise}(t)$ is represented as follows.

$$V_{noise}(t) = \frac{(R_{v1} + R_{v2})C_c V_{dd}}{\tau_a - \tau_v}(e^{-\frac{t}{\tau_a}} - e^{-\frac{t}{\tau_v}}). \quad (16)$$

From the result of differentiating Eq. (16), the noise voltage becomes the peak voltage V_{peak} at the time t_{peak}.

$$V_{peak} = \frac{(R_{v1} + R_{v2})C_c V_{dd}}{\tau_v}\left(\frac{\tau_v}{\tau_a}\right)^{-\frac{\tau_a}{\tau_v - \tau_a}}, \quad (17)$$

$$t_{peak} = \frac{\tau_a \tau_v}{\tau_a - \tau_v}\log\frac{\tau_a}{\tau_v}. \quad (18)$$

C. Driver Modeling

The proposed noise model replaces a driving CMOS gate as a resistance. The characterization of driving gates is explained. Replacing MOSFETs with resistors, a single-stage gate can be modeled as a pull-up resistance R_p, a pull-down resistor R_n, and an intrinsic output capacitance C_p(Fig. 5). C_{out} is the load capacitance. The resistance R_p and R_n are represented as two values; the driving resistance of aggressors R_{Dp}, R_{Dn}, and the holding resistance of victims R_{Hp}, R_{Hn}.

First, the driving resistance R_{Dp} is discussed. The propagating delay t_{PD}, which is the time difference between an input trip point of $0.5V_{DD}$ and output trip points of 0.37(falling, t_{PDf}) and 0.63(rising, t_{PDr}), is examined. Suppose the output signal changes low to high. The output voltage V_{out} is represented by

$$V_{out}(t) = V_{DD}\left(1 - \exp^{-t/R_{Dp}(C_p + C_{out})}\right). \quad (19)$$

From the definition, the equation of $V_{out}(t_{PDr}) = 0.63V_{DD}$ is satisfied. The delay time t_{PDr} is represented as $R_{Dp}(C_{out} + C_p)$. The pull-up resistance R_{Dp} is determined by evaluating t_{PDr} under two conditions of C_{out} with circuit simulator. The pull-down resistance R_{Dn} can be calculated similarly.

The holding resistance can be obtained by the operating condition analysis of circuit simulation. The resistance R_{Hp} and R_{Hn} is represented as the resistance characterized in the case that the output voltage is V_{DD} or V_{SS}.

D. Crosstalk Induced Delay

We explain the estimation method of the delay variation caused by crosstalk noise. We assume that the transition waveform affected by crosstalk noise $V_{affected}$ is represented as the superposition of the noise waveform V_{noise}(Eq. 16) and the transition waveform without crosstalk noise V_{tran}. In order to consider the non-linearity of CMOS gates, we choose the proper resistance from the driving and holding resistances according to the operating condition of the driver.

$$V_{affected}(t) = V_{victim}(t) \pm V_{noise}(t - t_0), \quad (20)$$

where t_0 is the timing difference between the transition of victim wire and that of aggressive wire. The sign of $\pm$ varies according to the transition direction. As for the transition waveform V_{tran}, various estimation methods have been proposed so far [11, 12], and our method can utilize those methods. Using Eq. (20), we can calculate the crosstalk induced delay.

III. Application to Generic RC Trees.

In practical circuits, many of RC trees have multiple sinks and multiple aggressors. Multiple sinks means that the tree contains branches. This section discusses transformation methods from general RC trees into the 2-π model circuits.

A. Multiple Sinks

First, the transformation method from RC trees that contains branches into the 2-π model circuit is discussed. The noise at the i-th sink S_i caused by the j-th aggressor is considered. In this case, the trees are separated into two cases; Fig. 6 and Fig. 7. In Case 1 of Fig. 6, the path between the source SO and the sink S_i contains the node connected with the aggressor, n_{cc}. Conversely, in Case 2 of Fig. 7, the node n_{cc} is not on the path between the source SO and the sink S_i. The node n_{cc} is included within the k-th branch B_k. We first explain the method to apply RC trees of Case 1 to the 2-π victim model. Next, we discuss the translation method from the trees of Case 2 to those of Case 1.

First, the method to build the 2-π victim models(Fig. 4) from the trees of Case 1 is explained. We replace each branch with an effective capacitance. Reference [8] proposes a method that each branch is replaced with a capacitance whose amount is the total capacitance of the branch. This replacement, however, ignores the resistive shielding effect, which results in the underestimation of crosstalk noise. In our approach, we first calculate the admittance of each branch at the junction [13]. We then compute the effective capacitance C_{Beff_k} of the k-th branch by the method of Ref. [10]. C_{Beff_k} is calculated such that the amount of the charge poured into the branch and the amount of the accumulated change in C_{Beff_k} become equal at a time T. The important parameter here is T, and our method utilizes the Elmore delay from n_{cc} to S_j as T. The effective capacitances C_{Beff_k} are added into C_{v1}, C_{v2}, and C_{v3} in Fig. 4 in the following manner:

- When a branch B_k is between SO and n_{cc}, the resistance between SO and n_k, R_{SO-n_k}, is represented as $R_{SO-n_k} = \alpha \cdot R_{SO-n_{cc}}$, where $0 \leq \alpha \leq 1$. Then $\alpha \cdot C_{Beff\_k}$ is added to C_{v2}, and $(1-\alpha) \cdot C_{Beff\_k}$ is added to C_{v1}.
- When a branch B_k is between n_{cc} and S_i, the resistance between n_{cc} and S_i, $R_{n_{cc}-S_i}$, is represented as $R_{n_k-Si} = \beta \cdot R_{n_{cc}-S_i}$, where $0 \leq \beta \leq 1$. Then $\beta \cdot C_{Beff\_k}$ is added to C_{v2}, and $(1-\beta) \cdot C_{Beff\_k}$ is added to C_{v3}.

Next, the transformation method from Case 2 to Case 1 is explained. Reference [8] does not consider the trees of Case

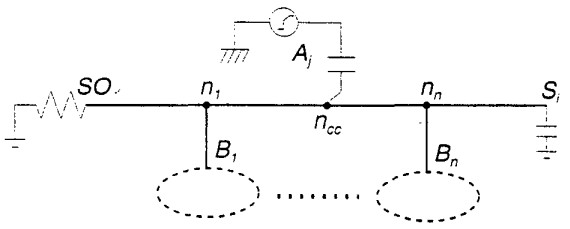

Fig. 6. An Interconnect with Branches(Case 1).

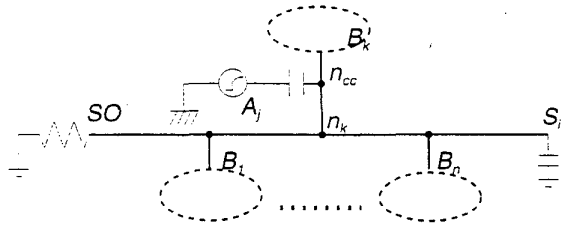

Fig. 7. An Interconnect with Branches(Case 2).

2. We therefore devise a transformation method from the trees of Case 2 to the trees of Case 1. After this transformation, the method explained above is applied to RC trees. We first move the coupling capacitance from the node n_{cc} to the node n_k(Fig. 7). The capacitance between n_{cc} and n_k is added to C_{v2}. We calculate the effective capacitance of the downstream network from n_{cc}, C_{Beff_k}, in the similar way with Case 1. The effective capacitance C_{Beff_k} is added to C_{v2}. The distance between n_{cc} and n_k is considered in the amount of C_{v2}. The appropriateness of this transformation is experimentally verified in Sec. IV-B.1.

B. Multiple Aggressors

We next discuss interconnects coupled with several interconnects, that is RC trees with multiple aggressors. In linear systems, a noise waveform on victim net is derived superposing of every noise waveform caused by each aggressor. The proposed method assumes crosstalk noise can be estimated by the superposition although CMOS circuits are non-liner systems. Sec. IV-B.2 experimentally demonstrates that this assumption of the superposition is reasonable.

IV. Experimental Results

This section shows some experimental results. First the accuracy of the crosstalk noise model is demonstrated. Next we examine the transformation method of generic RC trees.

A. Two Partially-Coupled Interconnects

The accuracy of the crosstalk noise model is discussed. We here estimate crosstalk noise of two partially-coupled interconnects shown in Fig. 1. First, we evaluate the peak voltage of the crosstalk noise. Next, some error sources of crosstalk noise estimation are discussed. We then estimate the delay variation caused by crosstalk noise.

Crosstalk noise is evaluated under the following conditions. We assume local and intermediate interconnects in a 0.13μm technology. The supply voltage V_{dd} is 1.2V. The electrical parameters of interconnects are evaluated by a 3D field solver. Table I lists the parameters of two fully-coupled interconnects. The pull-up and pull-down resistances of a standard inverter are 3.4kΩ and 1.1kΩ. The resistance of the drivers varies from 7Ω, corresponding to x64 inverter, to 3.4kΩ. The wire length is from 50μm to 3.3mm, and the coupling position and the coupling length are variously changed. The total number of noise evaluation is about 1,000.

TABLE I
Electrical Parameter of Interconnects.

	Local	Intermediate
Wire Resistance[Ω/μm]	0.367	0.0846
Coupling Capacitance[fF/μm]	0.0606	0.0575
Grounded Capacitance[fF/μm]	0.0716	0.0960

A.1 Peak Noise Estimation

We evaluate the peak noise voltage in the model circuit of Fig. 1 by circuit simulation, the conventional method [8] and the proposed method. In the conventional method [8], the signal from the aggressive wire $V_{agg(t)}$ is represented as a saturated lump function.

$$V_{agg}(t) = \begin{cases} \frac{t}{t_r} \cdot V_{DD} & (0 \le t \le t_r), \\ V_{DD} & (t \ge t_r). \end{cases} \quad (21)$$

However the calculation method of t_r is not explained. In this experiment, the transition time t_r is calculated as $\tau_a \times 1.7$. The coefficient of 1.7 is determined such that the sum of the absolute error between the simulation results and the results estimated by Ref. [8] is minimized.

Fig 8 shows the estimation results by the proposed method. The horizontal axis represents the noise voltage estimated by circuit simulation and the vertical axis is that of the proposed method. The diagonal line indicates the ideal line with 0 error. The proposed method estimates the peak noise voltage accurately. The average estimation error is 4.7% . Fig 9 shows the results of the conventional method [8]. Compared with the proposed method, the estimation accuracy is not high. The average error is 15.8% . The estimation accuracy is improved by adopting an exponential function as the signal waveform from the aggressor V_{agg}. Fig 10 shows an example of the waveforms of crosstalk noise evaluated by circuit simulation and the proposed method. The waveform of the crosstalk noise is precisely estimated by the proposed method.

The proposed method uses an effective capacitance in Eq. (8) for deriving the aggressor signal V_{agg}. We examine the efficacy of this method. The model circuit used for this experiment is Fig. 2. We evaluate the peak noise in the following circuits; the coupling length is 10% of the total length, and the length of the aggressive wire after coupling is 90%. This example is one of the most effective cases of C_{a3eff}, i.e. R_{v3} becomes relatively large compared with R_{v1} and R_{v2}. Fig. 11 shows the estimation error of the peak noise by the proposed method using C_{a3eff} and the method using C_{a3}. We vary the length of the aggressive wire and the driver strength, and evaluated the peak noise

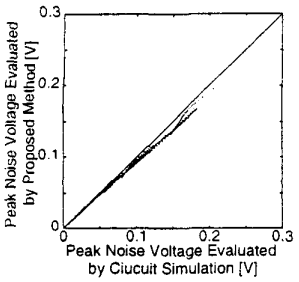

Fig. 8. Peak Noise Estimation in Model Circuit of Fig. 2 by Proposed Method.

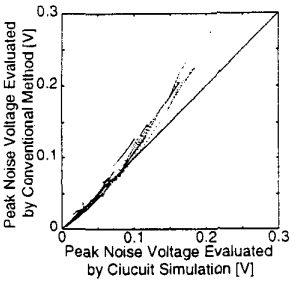

Fig. 9. Peak Noise Estimation in Model Circuit of Fig. 2 by Conventional Method [8].

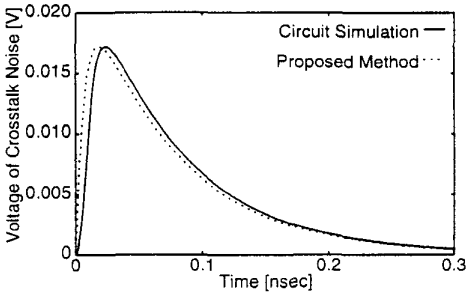

Fig. 10. An Example of Crosstalk Noise Waveform.

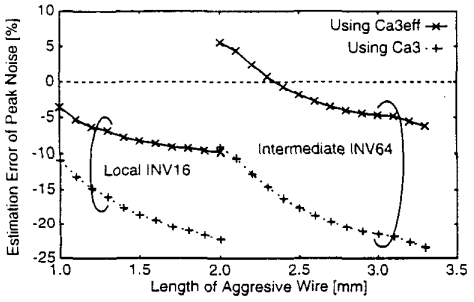

Fig. 11. Accuracy Comparison of Peak Noise Estimation.

voltage. When C_{a3} is used, the peak noise is underestimated, because the time constant of V_{agg}, τ_a, is overestimated. On the other hand, the proposed method estimates the peak noise accurately. The maximum error is decreased from 24% to 10%.

Fig. 12 shows the estimation error including the transformation of an actual two partially-coupled interconnects into Fig. 2, i.e. the replacement of CMOS gates with resistors and mapping distributed RC interconnects into the 2-π noise model. The horizontal axis represents the results of circuit simulation with CMOS gates and detail-segmented RC network. The average estimation error is 11%. We analyze this estimation error in the following section.

A.2 Examination of Error Sources

We examine the error sources of the proposed crosstalk noise model. We take up the following three steps that may cause estimation error.

Step 1: Replacing a CMOS gate as a resistance and a voltage source.

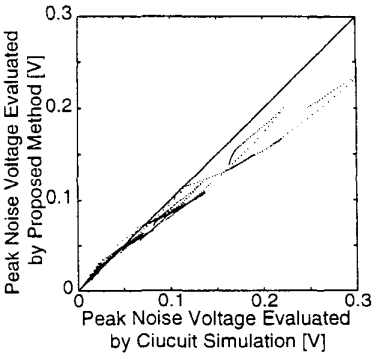

Fig. 12. Peak Noise Estimation for Interconnects Driven by CMOS Inverters.

Step 2: Transforming two partially-coupled interconnects into the model circuit of Fig 2.

Step 3: Approximations used in deriving the analytic waveform of Eq. (16).

The appropriateness of the above three steps is experimentally verified in peak noise estimation. The average errors caused by each step are evaluated from the following circuit simulation results; two partially-coupled interconnects driven by CMOS inverters, interconnects driven by resistances, and Fig 2. Table II shows the results. The average error of Step 1 is larger than the errors of Step 2 and 3, and Step 1 is a dominant error source in the proposed method.

TABLE II
AVERAGE ERROR OF EACH APPROXIMATION STEP IN PEAK NOISE ESTIMATION

	Step 1	Step 2	Step 3	Total
Error(%)	9.9	2.2	4.7	13.1

We further examine the error of Step 1. The pull-up resistance of a standard CMOS inverter is estimated such that the peak noise voltage evaluated by circuit simulation with CMOS inverter becomes equal with the noise evaluated with a resistance. Fully-coupled interconnects are assumed. Fig. 13 shows that the value of resistance varies as the total wire length changes. The vertical axis represents the resistance that keeps the error of Step 1 within $\pm 1\%$. The horizontal line labeled "Proposed Method" is the resistance estimated by the method of Sec. II-C. Fig. 13 means that the optimal resistance value for noise estimation depends on interconnect structure. The resistance value calculated by the proposed method is around the middle of the variation range. As long as the driver resistance is calculated independent of the output interconnect structure, the proposed method is apposite. If more accurate noise estimation is required, the driver resistance needs to be determined considering the output interconnect structure.

A.3 Estimation of Crosstalk Induced Delay

Next, we examine the estimation accuracy of the delay variation caused by crosstalk noise. In this experiment, we derive the transition waveform without crosstalk noise , V_{tran}, such that $V_{tran}(t) = V_{dd}\left(1 - e^{-t/\tau_v}\right)$. Fig 14 shows the estima-

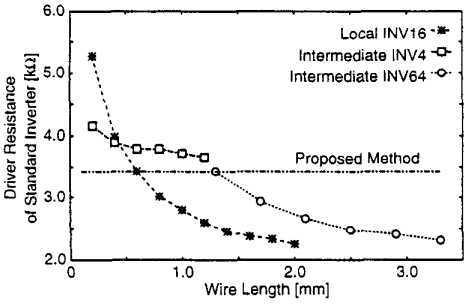

Fig. 13. Relationship between Wire Length and Driver Resistance, where the driver resistance is decided such that the peak noise can be estimated within 1% error.

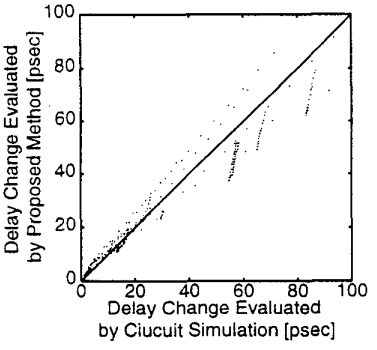

Fig. 14. Estimation of Delay Variation Caused by Crosstalk Noise.

tion results of the delay variation caused by crosstalk noise. The horizontal axis represents the value estimated by circuit simulation and the vertical axis is the value estimated by the proposed method. The delay variation caused by crosstalk noise is estimated with the error of 24% on average.

B. Generic RC Trees

In this section, we show the estimation results of crosstalk noise in generic RC trees. First, We discuss RC trees contain branches. Next, the circuits with some aggressors are discussed.

B.1 Multiple Sinks

We first evaluate the peak noise in the interconnect structure of Fig. 15. The victim net has two branches. The lengths of branches are varied from 0.3 to 3mm. The lengths of the victim and aggressive nets vary 0.3-3mm. The coupling position and the positions of the branch junctions are variously changed. The total number of the evaluated interconnect structures is about 6,500. In order to verify the effectiveness of replacing a branch with an effective capacitance C_{Beff_k}, we evaluate the peak noise in the following three circuits by circuit simulation.

- Each branch is expressed as a detail-segmented RC ladder.
- Each branch is replaced with a capacitance whose amount is the total capacitance of the branch (Ref. [8]).
- Each branch is replaced with the effective capacitance C_{Beff_k} (Proposed Method).

The results are shown in Figs. 16 and 17. In the conventional method of Fig. 16, the noise voltage is underestimated, and the

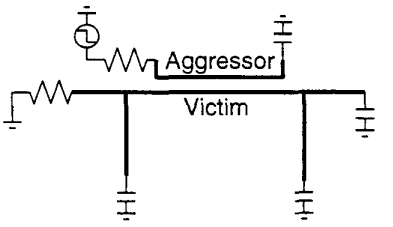

Fig. 15. Interconnect Structure with Branches used for Experiment.

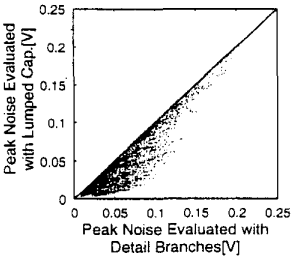

Fig. 16. Estimation Error of Replacing Branches by Conventional Method.

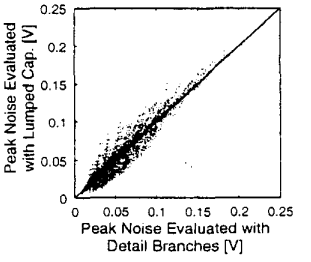

Fig. 17. Estimation Error of Replacing Branches by Proposed Method.

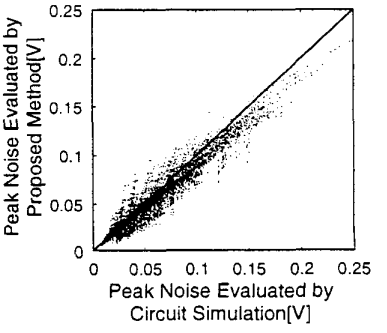

Fig. 18. Peak Noise Estimation by Proposed Method in Fig. 15.

average estimation error is 21%. On the other hand, this underestimation is improved in the proposed method. The average error is reduced to 13%. Replacing a branch with an effective capacitance improves the estimation accuracy. We next compare the peak noise evaluated by the proposed model and the circuit simulation result (Fig. 18). The average estimation error is 14%, and the amount of error is comparable with the other errors discussed in Sec. IV-A.2.

We next evaluate the peak noise in the interconnect structure of Case 2(Fig. 7), i.e. the aggressor exists inside a branch. The circuit of Fig. 19 is used for the experiment. We vary the distance x, and evaluate the peak noise by circuit simulation and the proposed method. Fig. 20 shows the estimation results. The proposed method indicates the same tendency of the saturation.

B.2 Multiple Aggressors

We estimate peak voltage of crosstalk noise caused by two aggressors. Using three partially-coupled interconnects driven by CMOS inverters, we demonstrate that a peak noise by two aggressors can be estimated superposing of every peak noise by each aggressor. We compare two peak noise values; the peak

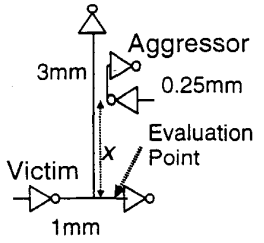

Fig. 19. Interconnect Structure used for Experiment.

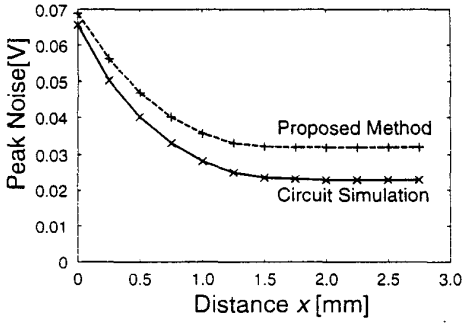

Fig. 20. Peak Noise Estimation in Circuit of Fig. 19.

noise estimated by simulating the circuit with two aggressors exactly, and the peak noise derived from the superposition of each noise evaluated by circuit simulation. We vary wire length, coupling position and transient timing of two aggressors. The total number of estimation is about 3,500. The results are shown in Fig. 21. The estimation average error is 1.5%. We can see that the peak noise can be estimated by superposition though CMOS circuits are not ideal linear systems.

Finally peak noise and crosstalk induced delay are estimated by the superposition using the proposed crosstalk noise model. The evaluated interconnect structures are the same with those in the above experiment. Fig. 22 shows the estimation results of the peak noise by two aggressors, and Fig. 23 demonstrates the estimation results of the delay change by two aggressors. The horizontal axis represents the values estimated by circuit simulation using three partially-coupled interconnects driven by CMOS inverters, and the vertical axis is the values estimated by the proposed method. The average error of peak noise estimation is 18% , and that of delay change estimation is 18%. The proposed method can estimate crosstalk noise for any types of RC network.

V. Conclusion

This paper proposes an estimation method of crosstalk noise for both peak voltage and crosstalk induced delay. We develop a 2-π noise model for accuracy improvement. The transformation method from any types of RC trees to 2-π model is devised. We verified the accuracy of the proposed method in a 0.13μm technology. The average error of estimating the peak noise of two partially-coupled interconnects is 13%. We analyze the error sources of noise estimation, and conclude that further accuracy improvement is difficult as long as the driver resistance is decided independent of the output interconnect structure. We also

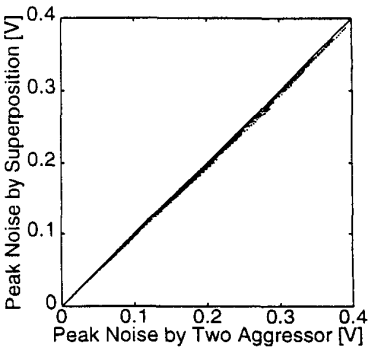

Fig. 21. Noise Estimation by Superposition in Non-Linear CMOS Circuits.

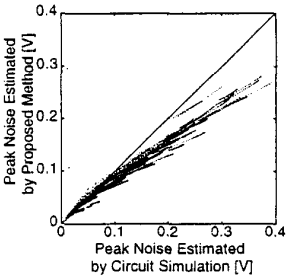

Fig. 22. Estimation of Peak Noise by Two Aggressors.

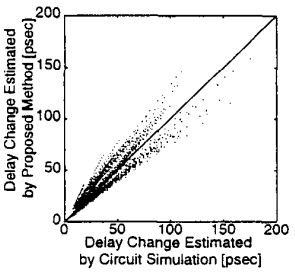

Fig. 23. Estimation of Delay Change by Two Aggressors.

verify that any types of RC trees can be transformed into the 2-π noise model with the average error of 14%. The proposed method handles interconnect resistance well, which is suitable for DSM LSI design.

References

[1] T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's," *IEEE Trans. on Electron Devices*, Vol. 40, No. 1, January 1993.

[2] H. Kawaguchi and T. Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," *Proc. ASP-DAC*, pp.35-43, 1998.

[3] A. Vittal and M. Marek-Sadowska, "Crosstalk Reduction for VLSI," *IEEE Trans. CAD*, Vol. 16, No. 3, pp.290-298, March 1997.

[4] A. Rubio, N. Itazaki, X. Zu, and K. Kinoshita, "An Approach to the Analysis and Detection of Crosstalk Faults in Digital VLSI Circuits," *IEEE Trans. CAD*, Vol. 13, No. 3, pp.387-394, March 1994.

[5] A. Devgan, "Efficient Coupled Noise Estimation for On-Chip Interconnects," *Proc. ICCAD*, pp.147-151, 1997.

[6] B. N. Sheehan, "Predicting Coupled Noise in RC Circuits By Matching 1, 2, and 3 Moments," *Proc. DAC*, pp.532-535, 2000.

[7] A. Vittal, L. Chen, M. Marek-Sadowska, K.-P. Wang, and S. Yang, "Crosstalk in VLSI Interconnections," *IEEE Trans. CAD*, Vol. 18, pp.1817-1824, 1999.

[8] J. Cong, D. Z. Pan, and P. V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization," *Proc. ASP-DAC*, pp.373-378, 2001.

[9] H. B. Bakoglu, "Circuits, Interconnections, and Packaging for VLSI," Addison-Wesley Publising Company, 1990.

[10] C. V. Kashyap, C. J. Alpert, and A. Devgan, "An Effective Capacitance Based Delay Metric for RC Interconnect," *Proc. ICCAD*, pp.229-234, 2000.

[11] E. Chiprout and M. S. Nakhla, "Asymptotic Waveform Evaluation," Kluwer Academic Publishers, 1994.

[12] C.-K. Cheng, J. Lillis, S. Lin, and N. H. Chang, "Interconnect Analysis and Synthesis," A Wiley-Interscience Publication, 2000.

[13] P.R. O'Brien and T. L. Savarino, "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation," *Proc. ICCAD*, pp.512-515, 1989.