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On-Chip Thermal Gradient Analysis Considering Interdependence between Leakage Power and Temperature**

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SUMMARY In this paper, we propose a methodology for calculating on-chip temperature gradient and leakage power distributions. It considers the interdependence between leakage power and local temperature using a general circuit simulator as a differential equation solver. The proposed methodology can be utilized in the early stages of the design cycle as well as in the final verification phase. Simulation results proved that consideration of the temperature dependence of the leakage power is critically important for achieving reliable physical designs since the conventional temperature analysis that ignores the interdependence underestimates leakage power considerably and may overlook potential thermal runaway.

key words: *thermal gradient simulation, leakage power, temperature-dependent leakage power, power calculation, leakage model*

1. Introduction

The leakage power of a large-scale integrated circuit (LSI) plays an important role in low-power circuit designs. Reduction of the leakage power is crucially important in mobile applications such as in cellular phones. As mobile systems are becoming commonplace, finer design rules are utilized to pursue lower cost and higher circuit performance. Accurate estimation and better control of the leakage power are some of the dominant factors that determine the overall systems' success.

Even in high-performance applications, such as in microprocessors or network processors, leakage power estimation is absolutely necessary [1]–[3]. In these systems, designers sometimes need to optimize the best balance between performance and leakage since the drain current of the metal-oxide-semiconductor (MOS) field-effect transistors (FETs) is inversely related with their threshold voltage. The lower the threshold voltage is, the larger the on-current becomes at the cost of larger leakage current. Since many high-end designs tend to allow higher leakage power, they need to avoid thermal runaway with a verified margin. The larger power dissipation of these chips significantly increases chip temperature, which results in an exponential increase in leakage current. In the past, thermal analysis or thermal management has been conducted for a very limited variety of products. In recent designs, more chips require thermal consideration and treatment. The number of chips that require them will be increasing as device feature size continues to be reduced. As more functions are integrated in a chip or in a package, thermal analysis considering leakage power will become increasingly important.

There are roughly two design phases where thermal analysis is required — pre layout and post layout. Post layout analysis is conducted for verification purposes so accuracy is pursued using all the physical design information readily available at that time. However, a design flow that only incorporates post layout verification will not be sufficient since temperature repair at the post layout phase is almost impossible without significantly changing the floorplan. Thus, temperature consideration in the pre layout or at least in the layout design phase is preferable. There are not so many reports on studies of temperature consideration early in the design stage. Authors in [4] propose on-chip temperature flattening at the floorplan phase. Authors in [5] consider temperature reduction as one of the objectives in force-directed placement. However, these works do not distinguish between dynamic power and leakage power. Here, dynamic power refers to charging-discharging power consumption for capacitive load and short-circuit power consumption associated with logic switching. Leakage power refers to the non switching current between power supply rail and ground which flows through off-state transistors.

In this paper, we propose an on-chip thermal gradient analysis methodology. The methodology can be utilized in all design phases with the available information at a given phase. Our contributions in this paper are summarized as follows:

- Extending the work in [4], we propose a model for thermal simulation with which we can consider the interdependence between temperature and leakage power. Using the proposed simulation model, changes in on-chip temperature gradient due to leakage power are calculated for the first time.

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- As a consequence of the proposed methodology, estimations of both on-chip temperature distribution and leakage power become more accurate than those that are calculated by treating temperature and leakage power separately. As a result, chip designs become much more reliable.

Owing to the exponential dependence of the leakage power on temperature, inaccurate estimation of the leakage power usually results in underestimations of both power consumption and temperature gradient. This not only results in performance degradation but may also end up with thermal runaway. Hence, simultaneous estimation of the chip temperature distribution and leakage power is extremely important.

2. Leakage Current Model as Function of Temperature

In our analysis, we utilize the finite-difference (FD) approach to solve the heat diffusion equation on the basis of an electrical-thermal analogy [6], [7]. The FD approach described in [4] is briefly reviewed in the next subsection. Then, it will be extended to handle the interdependence between leakage power and on-chip temperature.

2.1 On-Chip Temperature Analysis Utilizing Thermal-Electrical Analogy

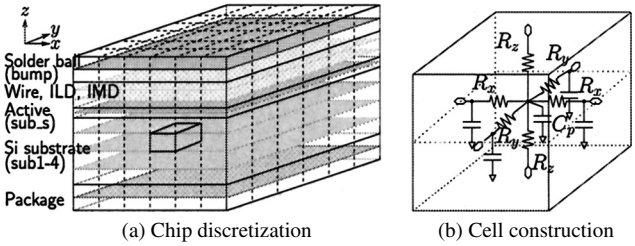
The heat diffusion equation is described by Fourier's law.

$$\boldsymbol{q} = -\kappa \nabla \boldsymbol{T} \tag{1}$$

Here, $\boldsymbol{q}$ is the heat flux vector, κ is the thermal conductivity, and $\boldsymbol{T}$ is the temperature. Similarly, electrical conduction is given by the following equation.

$$\boldsymbol{j} = -\sigma \nabla \boldsymbol{V} \tag{2}$$

Here, $\boldsymbol{j}$ is the current density vector, σ is the electric conductivity, and $\boldsymbol{V}$ is the electric potential, or voltage. Since two different phenomena are described using the identical form of differential equations, we can analyze on-chip temperature using an electrical equivalent model. Figure 1 shows the model structure for the thermal simulation. Different materials having different thermal properties are stacked in the model. The layer labeled as "solder ball (bump)" represents metal connections between the package and the printed circuit board, the layers labeled "wire, ILD, IMD" represent a composite of metal wire interconnections, interlayer dielectrics (ILDs) and inter metal dielectrics (IMDs), the layer labeled "Active" represents a surface of silicon substrate where active devices such as transistors are placed, the layers labeled "Si substrate" represent bulk silicon substrate, and the layer labeled "Package" represents epoxy or ceramic packaging material. A die contained in a package is discretized using three dimensional grids to form cells which mutually connect with adjacent cells in the x, y, and z directions. Each cell consists of thermal resistance (R_x, R_y, R_z) and capacitance (C_p) as depicted in Fig. 1(b). Composite thermal resistance models and composite capacitance models represent thermal properties for the package and silicon die (metal wire layers, device, and bulk substrate layers). A set of example values used in this paper is shown in the Appendix for reference, although the derivation of these values is described in detail in [4]. Thermal resistances located at the package–air boundaries are subjected to atmosphere temperature T_a, which is modeled using ideal voltage sources. The values of the voltage sources connected at the package top, bottom, and side can differ from each other since they generally have different boundary conditions.



(a) Chip discretization (b) Cell construction

Fig. 1 Thermal simulation model used in this analysis.

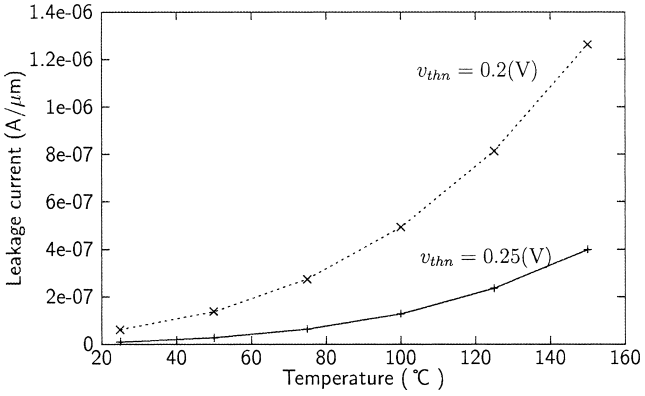
Power dissipation due to device operation at the die surface is modeled using current sources. In Fig. 1, current sources are connected at the center of the cells in the layer "sub_s." By consulting analogies of the thermal–electrical systems shown in Table 1, total power in a grid cell corresponds to the value of the current source in the cell [3], [8]. Note that current sources can be also connected to the metal wire layers in circumstances where power consumption in the wire cannot be neglected. The ideal current sources used in the previous work [4] are independent of both temperature and time. In this work, we modify current sources to represent temperature dependence.

2.2 Subthreshold Leakage Current Model for Transistor

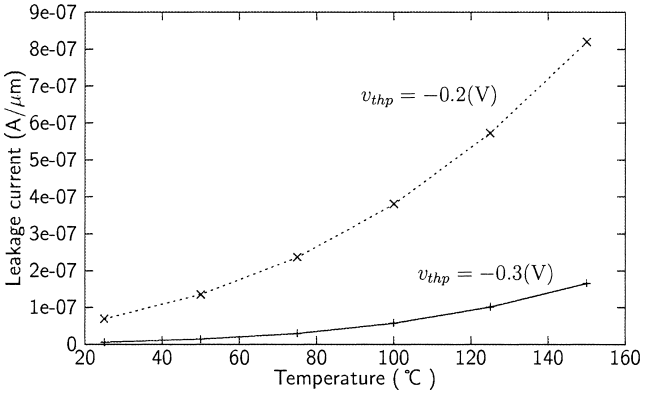
We first study the temperature dependence of the transistor leakage current using Berkeley predictive technology models (BPTM) [9], [10]. Figure 2 shows width-normalized leakage currents I_{off} calculated using 0.10-μm N-ch (a) and P-ch (b) MOS transistors. Device currents for two different threshold voltages are plotted. v_{thn} and v_{thp} stand for the threshold voltages of N-ch and P-ch MOSFETs, respectively. As seen from the figure, leakage current increases exponentially as device temperature rises. At 120°C, leakage current becomes approximately 10 times larger than that at 25°C. Since millions of transistors are integrated in a chip, the power consumption of a die changes significantly with the temperature. Hence, in temperature analysis, the illus-

Table 1 Duality between thermal and electrical quantities [3].

Thermal (Therm.)	Units	Electrical (Elec.)	Units
Power	W	Current	A
Temperature	°C	Voltage	V
Therm. resistivity	m·°C/W	Elec. resistivity	m·Ω
Therm. resistance	°C/W	Elec. resistance	Ω
Therm. capacitance	J/°C	Elec. capacitance	F



(a) N-ch MOSFET



(b) P-ch MOSFET

Fig. 2 Leakage current I_{off} of 0.1-μm transistor.

trated change in leakage power has to be correctly accounted for. Designers have to pay close attention to the interdependence between leakage power and on-chip temperature because of their positive feedback nature—a temperature rise increases leakage power and increased power raises temperature.

The leakage current I_{off} of a transistor consists of two major components: subthreshold leakage I_{sub} and gate oxide tunneling I_{gate}. Subthreshold current has a strong temperature dependence as can be seen in Fig. 2. Meanwhile, gate oxide tunneling current has a weak dependence on temperature [11]. Therefore, we model subthreshold leakage power as a function of temperature, but we model gate oxide tunneling power as temperature-independent in a manner similar to that in the dynamic power model.

On the basis of the equation used in the BSIM3 model, we represent subthreshold current as [12]

$$I_{sub} = I_{s0}\left(1 - e^{\frac{-v_{ds}}{v_t}}\right) e^{\frac{v_{gs}-|v_{th}|-v_{off}}{n \cdot v_t}}, \tag{3}$$

$$I_{s0} = \mu_0 \frac{W}{L} C_{OX} \cdot v_t^2. \tag{4}$$

Here, μ_0 is the carrier mobility at zero-bias, C_{OX} is the gate oxide capacitance per unit area, W/L is the aspect ratio of a transistor, v_{ds} is the drain-source voltage, v_{gs} is gate-source voltage, $v_t \equiv kT/q$ is the thermal voltage, v_{th} is the threshold voltage, v_{off} is a fitting parameter (which is a function of v_{th}), n is the subthreshold swing, k is Boltzmann's constant, and q is the electron charge. Off-state refers to the voltage state where v_{gs} is 0 V and v_{ds} is in between 0 V and supply voltage. Considering the temperature dependence of each parameter, Eq. (3) can be approximated to have the following form:

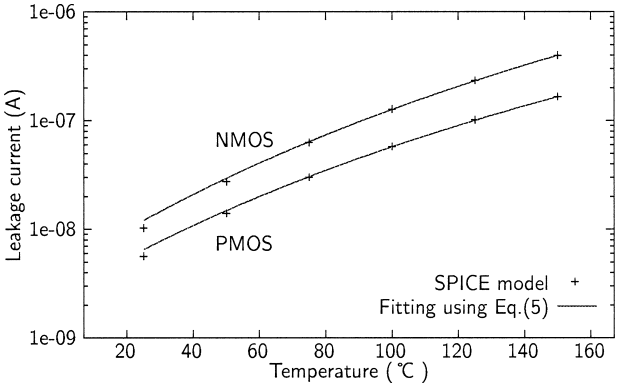


Fig. 3 Fitting of temperature dependence of subthreshold currents of MOS transistors using proposed model (Eq. (5); solid lines) with SPICE (symbols).

$$I_{sub}(T) = \alpha \cdot T^2 e^{-\frac{\beta}{T}}, \tag{5}$$

where

$$\alpha = \mu_0 \frac{W}{L} C_{OX} \left(\frac{k}{q}\right)^2 \left(1 - e^{-\frac{v_{ds}}{v_t}}\right) \tag{6}$$

$$\beta = \left(\frac{q}{k}\right) \frac{-v_{gs} + |v_{th}| - v_{off}}{n}. \tag{7}$$

The coefficients α and β can be obtained through the above equations or through a set of circuit simulations and fitting. Note that the last term in the scale coefficient α is temperature-dependent since it is a function of v_t. However, we approximate the term as constant ($1 - e^{-\frac{v_{ds}}{v_t}} \simeq 1.0$) under the typical operational conditions of the recent technologies ($T < 160$°C and $v_{ds} \simeq 1$ V). Note that v_{ds} can range from 0 to 1 V, and $v_{ds} = 1$ V is the worst case. The other parameters such as μ_0 in α [13] and v_{th} in the denominator of β are also temperature-dependent, but the effect on I_{sub} is small in the temperature range of interest.

Figure 3 shows the fitting result obtained using the proposed model equation with the MOS transistors' leakage current. Symbols in the figure are obtained through circuit simulations and lines are from Eq. (5). Proposed leakage model agrees well with SPICE simulation results, correctly representing its temperature dependence.

2.3 Leakage Current Models for Logic Cells and Circuit Blocks

In cell-based logic LSI design flows, it is more convenient to model the leakage current of the cells or circuit blocks as a whole rather than on a single transistor basis. However, there exist several off-states for a logic cell. The leakage current of the cell depends on its state. Different off-states refer

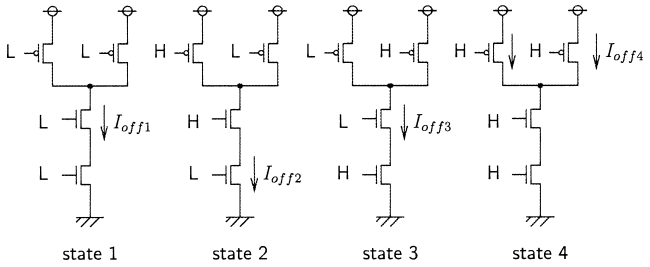


Fig. 4 Different off-state currents for NAND cell.

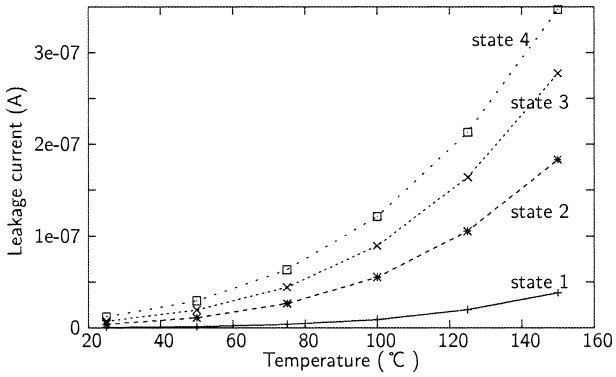


Fig. 5 Leakage current of 0.1-μm NAND cell as functions of temperature ($v_{thn}/v_{thp} = 0.25/-0.3$ V).

to different combinations of the input pins' logic states. Let us refer to some examples in Figs. 4 and 5. Figure 4 shows a schematic illustration of different off-states of a NAND cell. Figure 5 shows the temperature dependence of the leakage current of each off-state. We understand that there is a significant leakage current difference between the states. States 1 and 4, in which the leakage current becomes minimum and maximum, respectively, differ by a factor of about 10.

We also find that the proposed equation (5) holds for all the cell-leakage currents of the different states. Figure 6 shows fitting results based on Eq. (5) for an inverter cell and a NAND cell. For both logic cells, Eq. (5) fits well with the SPICE-simulated leakage currents over a wide range of temperatures. In general, the input states of the logic cells in an LSI differ from each other. When we consider a group of cells, the leakage current of the group is calculated as the sum of each cell current which should be well approximated by Eq. (5). The total leakage current of a circuit can be expressed by Eq. (5) as long as we know all the input states of all the cells. More formally, let $I_{sub,i}(T_i(t), s_i(t))$ be the leakage current of the i-th cell instance at its local temperature $T_i(t)$ and input logic state $s_i(t)$ at time t; the total leakage current of a block $I_{total\_leak}(t)$ at time t can then be obtained as follows. Note that $s_i(t)$ is determined by a logic simulation.

$$I_{total\_leak}(t) = \sum_{i \in block} I_{sub,i}(T_i(t), s_i(t)) \tag{8}$$

However, logic simulation to obtain $s_i(t)$ may take a long time or may not always be executable, especially early

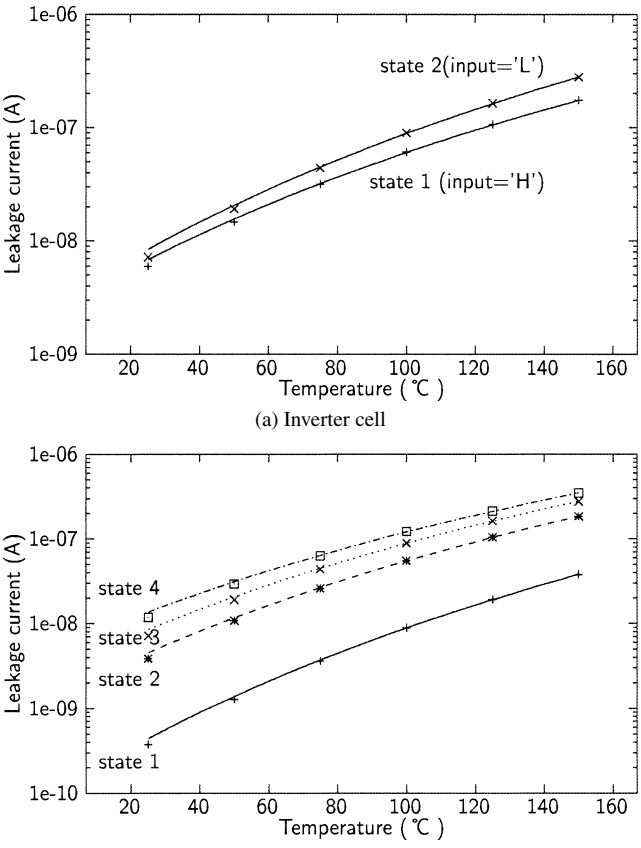


Fig. 6 Fitting of sub-threshold currents of logic cells using proposed model equation (solid line) with SPICE (symbols).

in the design stage. In addition, the input states of the cells change temporally as they are indicated to be functions of t. Considering the above factors and the fact that the time average is more important than instantaneous power consumption for steady-state temperature calculation, we propose to use the average leakage power of all possible off-states as the estimate of the leakage power of the circuit block.

$$I_{total\_leak} \simeq \sum_{i \in block} I_{sub,i}(T_i, \overline{s_i}) \tag{9}$$

Here, $I_{sub,i}(T_i, \overline{s_i})$ is defined as the average of all possible states, assuming each cell takes on various states over a long period of time in steady-state analysis. T_i represents the steady-state temperature of each cell instance.

Further simplification may be possible in the leakage calculation if the average leakage current of different cells can be well approximated using Eq. (5) and if the cells share the same exponent parameter β in $I_{sub,i}(T_i, \overline{s_i})$. From our simulation experiments, the exponent parameters β for different cells have been calculated to be almost equal. This is understandable since β is determined only by process parameters. Then, the leakage current of a block is estimated as a function of block temperature T.

$$I_{total\_leak} \simeq \alpha' \cdot T^2 e^{-\frac{\beta'}{T}} \tag{10}$$

On the basis of the total gate width W and input signal states

of each cell, we can determine a redefined scale parameter α'. The exponent parameter β' can be calculated using Eq. (7) as the average of individual logic cells' β, which can be precharacterized for each process technology.

Different levels of detailed parameters can be used depending on the design phase. In early design stages, the off-state current of the circuit block can be approximated using the sum of the average currents for each cell. In the verification phase, the actual state of each cell can be calculated through a set of logic simulations. As a short summary, the proposed leakage current model can be used for predicting the temperature dependence of a transistor, a logic cell, and circuit blocks.

3. Procedure to Consider Leak Current in on-Chip Temperature Calculation

In this section, we propose a procedure that considers leakage power in on-chip thermal analysis. The procedure is summarized by the following steps.

step 1: Calculate β' by off-state current simulation of various logic gates. First, we obtain temperature exponent β' through circuit simulation and fitting. Different coefficients can be used for different logic gates, but using the average value for each gate should work well especially in early design stages. The calculated β's are reusable for different designs with the same process, so this step has to be conducted only once for each process.

step 2: Calculate α' on the basis of block powers. Next, we calculate the scale factor α' of a circuit block at a predetermined temperature. This step can be conducted in two design phases: early stage and verification stage. In both phases, the required information is the ratio of dynamic power to leakage power at a certain temperature. In early design stages, available information about the circuit block power may be limited but the approximated instance count can be utilized, for example, through temporal logic synthesis.

step 3: Represent leakage power as an equivalent circuit model. Next, the proposed leakage power model is realized as an equivalent circuit. A conceptual drawing and the equivalent circuit model are shown in Figs. 7 and 8, respectively. Major differences from the previous work [4] are 1) the distinction between dynamic power and leakage power, and 2) the introduction of a leakage domain circuit dedicated for temperature-dependent leakage power calculation. In Fig. 8, an independent current source P_{dyn} represents dynamic power and a voltage-dependent current source P_{leak} represents leakage power. A voltage-controlled current source (VCCS) $I_{sub}(T_{(i,j)})$ represents the leakage power of a group of circuits in a grid cell at temperature $T_{(i,j)}$, which is defined by Eq. (5) or (10). A grid cell temperature $T_{(i,j)}$ is obtained by referring to the temperature-domain counterpart, which is represented as a node voltage. For each grid cell in the leakage power domain model, I_{sub} is connected with a resistor of the value V_{dd} in order to convert from leakage current into leakage power V_{ctl} which is represented as a node voltage $V_{ctl} = I_{sub}V_{dd}$. The mutual reference of the node voltages in the leakage power and local temperature using VCCS realizes interdependence.

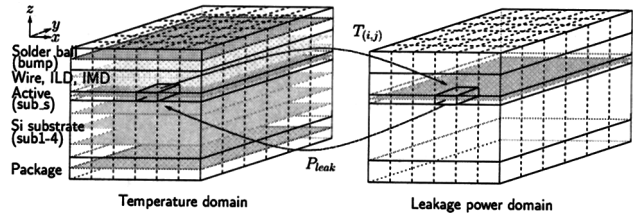


Fig. 7 Conceptual drawing of proposed equivalent models. The newly added leakage-power-domain model calculates temperature-dependent leakage power P_{leak} by consulting cell temperatures $T_{(i,j)}$ calculated in the temperature-domain model. The temperature domain model calculates the thermal distribution considering leakage power.

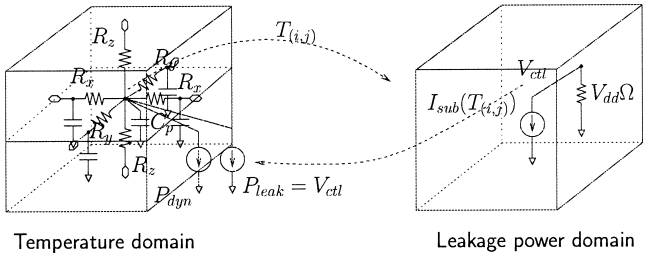


Fig. 8 Equivalent-circuit model used to consider interdependence between on-chip temperature and leakage power at grid cell coordinates (i, j).

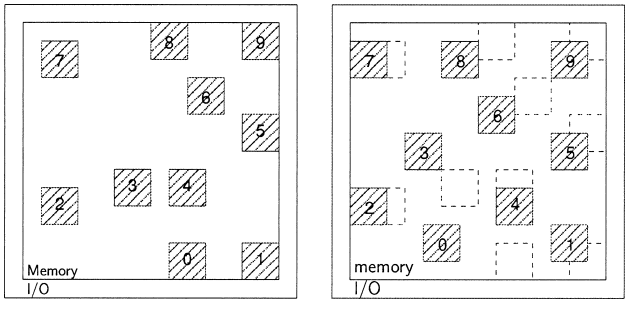
step 4: Solve the resultant equivalent model using a circuit simulator. Finally, after connecting boundary cells at atmosphere temperature using voltage sources, we solve the nonlinear circuit equation constructed in step 3 using a circuit simulator. Since Eq. (5) includes nonlinear dependence on die temperature, a nonlinear partial differential equation must be solved. This kind of problem can be efficiently solved using the steady-state or transient analysis functions of the circuit simulators.

Investigating a distribution of leakage power is sometimes useful. When there exists a high-power-density module on a chip, it may result in so-called thermal runaway owing to positive feedback between local temperature rise and leakage power increase [14]. Explicit use of the leakage power domain helps us analyze the leakage power distribution. However, for designers who require on-chip temperature gradient only, or in circumstances where memory usage limits analyzable circuit size, the leakage power domain can be eliminated by configuring the model in such a way that the current source P_{leak} in the temperature domain directly refers to its grid cell voltage (which is local temperature) to calculate the leakage power using Eq. (5).

4. Simulation Results

The on-chip temperature distribution is calculated while considering the temperature dependence of the leakage power. Figure 9 shows two floorplans: initial and optimized. In this context, the optimization has been conducted in terms of temperature flattening. Starting from the initial floorplan (Fig. 9(a)), the thermal flattening procedure proposed in [4] is conducted. In the optimized floorplan in Fig. 9(b), the initial floorplan is overlaid by dotted lines in order to show the movements of the logic blocks. Shaded squares with numbers represent logic blocks where the power density is higher than the other areas. The other areas include I/O blocks at the periphery of the chip and memory circuits that fill the remaining area. The example floorplan does not reflect a specific design, but the layout in which memory circuits are distributed over the entire chip is often adopted when a large number of power domains are used such as in [15]. This type of floorplan is considered to gain popularity in more advanced low-power designs.

In Table 2, block areas are counted on the basis of the number of the grid cells. P_{total}, P_{dyn}, and P_{leak} are the total, dynamic, and leakage powers at the maximum temperature T_{lim} which is 120°C in this analysis. We compare two temperature calculation scenarios: scenarios 1 and 2. Scenario 1 uses a conventional temperature-independent leakage power model. Both dynamic power and leakage power are calculated at T_{lim} and modeled in the same way. That is, the total power including both dynamic and leakage powers is modeled by an independent current source in each circuit type. On the other hand, scenario 2 distinguishes leakage power from dynamic power and models the leakage power using a VCCS. From its calculation, if and only if the chip temperature distribution is completely flat at T_{lim}, the total power of the two scenarios becomes equal.



(a) Initial (b) Optimized

Fig. 9 Example chip floorplan.

Table 2 Cell discretization and power distribution.

	I/O	Logic	Memory	Total
#cells	60	40	156	256
P_{total} (W)	6.7	17.4	8.1	32.3
P_{ac} (W)	4.5	15.9	2.3	22.7
P_{leak} (W)	2.3	1.5	5.9	9.6

Table 3 summarizes the result of on-chip temperature and leakage distribution. On-chip temperature is flattened even though the temperature-dependent leakage is taken into account. When comparing the maximum temperature T_{max} and the minimum temperature T_{min} on a chip, the T_{max} of scenario 2 becomes higher than that of scenario 1, and the T_{min} of scenario 2 becomes lower than that of scenario 1. As a result, the maximum on-chip temperature difference $\Delta T = T_{max} - T_{min}$ in scenario 1 is smaller than that in scenario 2 by 16.6% for the initial floorplan and 4.7% for the optimized floorplan, indicating that estimation through scenario 1 is optimistic. Here, the estimation error between the scenarios, ΔT_{err}, is calculated with scenario 2 as reference.

$$\Delta T_{err} = \frac{\Delta T_1 - \Delta T_2}{\Delta T_2} \tag{11}$$

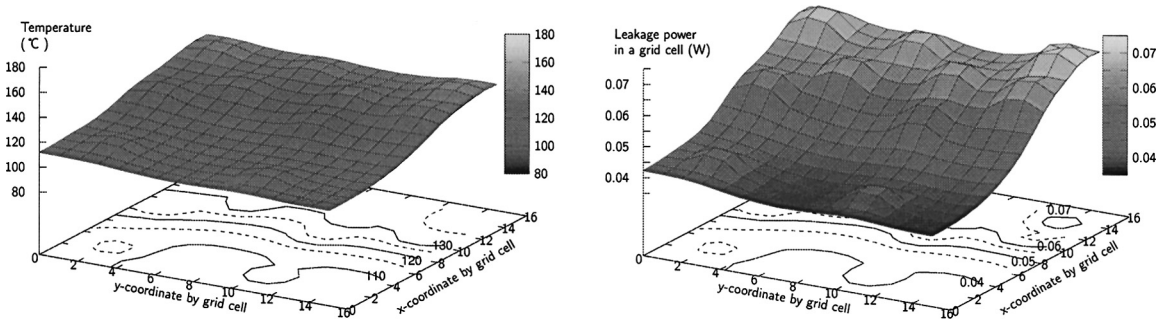
ΔT_1 and ΔT_2 are the maximum on-chip temperature differences in scenarios 1 and 2, respectively.

In scenario 2, the higher-power-density spot shows an even higher temperature, which increases local leakage power. An increase in the leakage power further increases the local temperature. Consequently, T_{max} increases when we consider temperature-dependent leakage power. In the same way, at the low-power-density spots, leakage power becomes smaller than the average value since the spot locally has a temperature lower than the average temperature originally used for leakage power calculation. Using the proposed model, these phenomena are correctly captured. Figure 10 shows temperature and leakage power distributions calculated using the proposed procedure. The leakage power distributes similarly to the on-chip temperature distribution but more steeply owing to its exponential dependence.

Scenario 1 underestimates leakage power when average temperature is different from a designer's expectation, especially when the on-chip temperature gradient is large as in the initial floorplan. The underestimation may result in thermal runaway owing to the positive feedback relationship between on-chip temperature and leakage power. This experiment also suggests that on-chip temperature flattening is important in making a chip more reliable and less leaky. The proposed model is accurate for a wide range of temperatures. Therefore, accurate transient simulation instead of steady-state simulation is also possible.

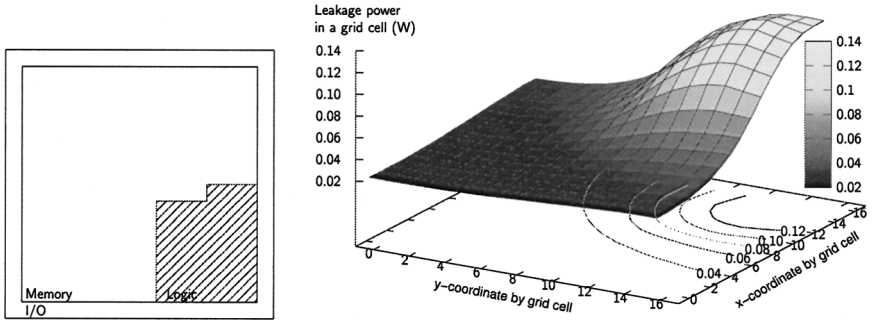
Table 3 Temperature and leakage power comparison for designs with different floorplans for the same total power.

Floorplan		Unit	Initial	Optimized
Scenario 1 (w/o leakage)	T_{max}	°C	133.9	123.4
	T_{min}	°C	107.8	115.3
	ΔT_1	°C	26.1	8.1
	P_{leak}	W	-	-
Scenario 2 (w/ leakage)	T_{max}	°C	137.4	123.6
	T_{min}	°C	106.1	115.1
	ΔT_2	°C	31.3	8.5
	P_{leak}	W	9.52	9.26
ΔT estimation error ΔT_{err}		%	−16.6	−4.7
P_{leak} estimation error P_{err}		%	0.84	3.67



(a) Temperature domain (b) Leakage power domain

Fig. 10 On-chip temperature and leakage current distribution of scenario 2.



(a) Floorplan (b) Leakage power (at leakage quota of 30%)

Fig. 11 Example floorplan and on-chip leakage current distribution.

In contrast to the temperature, total leakage power P_{leak} does not change significantly in this case compared with the initial expectation shown in Table 2. This is because the leakage power in Table 2 is calculated at T_{lim} and the average temperatures for both scenarios are almost around T_{lim}. When the estimation of the total chip power is smaller, the difference in leakage should become larger owing to the nonlinear relationship between leakage power and temperature.

Figure 11(a) shows another example. The total areas of the logic, memory, and I/O circuit blocks of this floorplan are the same as in the previous examples, but the placement of the logic circuit is different. Figure 11(b) shows a leakage power distribution using the proposed model. Due to the power concentration close to the corner of the die [4], a significant temperature gradient is observed. Figure 12 shows leakage power as a function of leakage power quota. The leakage power quota is defined as the ratio of leakage power to the total power of 32 W at T_{lim}. The conventional analysis (dashed), which does not consider temperature-leakage interdependence, calculates leakage power optimistically in comparison with the proposed analysis (solid). The larger the portion of leakage power, the larger the difference between the proposed and the conventional analysis. The leakage power cannot be compared beyond the point where the leakage power quota is 33% since thermal runaway is observed in the proposed analysis only. The use of the proposed model effectively predicts the reliability problem related to the the leakage power and on-chip temperature.

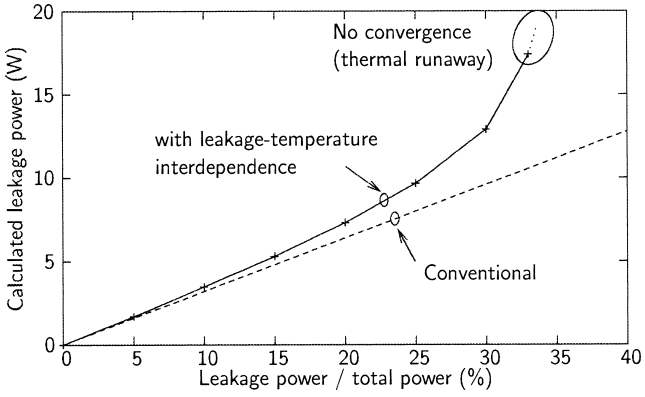


Fig. 12 Calculated leakage power for comparison with conventional analysis. A leaky circuit can result in thermal runaway owing to the interdependence between leakage power and temperature.

5. Conclusion

We proposed an on-chip temperature analysis methodology that accounts for temperature-leakage interdependence. In the proposed methodology, leakage power is expressed as a function of temperature and modeled using controlled source representation in order to realize an analysis using general circuit simulators. A model equation for temperature-dependent leakage current is proposed and its accuracy is verified with the leakage current obtained through transistor-level circuit simulations for a single tran-

sistor as well as for logic cells. A simulation example of the on-chip temperature distribution using the proposed model shows that considering temperature-dependent leakage power contributes to the accurate calculation of both the temperature distribution and the leakage power distribution. The proposed model reduces optimism existing in the conventional analysis and prevents suffering from performance degradation or thermal runaway after chip fabrication.

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Appendix: Example Thermal Resistance and Capacitance

Table A· 1 lists the thermal resistance and capacitance values used in the simulation examples.

Table A· 1 Example layer division and thermal properties used in this paper.

Layer	Thickness (μm)	R_x (K/W)	R_y (K/W)	R_z (K/W)	C_p (J/K)
package	200	2.7e4	2.7e4	2.72e3	9.81e-5
sub1–4	125	63.49	63.5	2.54	8.00e-5
sub_s	2	9.0e3	1.8e4	0.037	1.56e-6
wire1–2	3.1	7.8e3	7.8e3	0.93	5.39e-6
bump	200	5.0e4	5.0e4	1.0e3	1.69e-5

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