EQUIVALENT WAVEFORM PROPAGATION FOR STATIC TIMING ANALYSIS

Masanori Hashimoto, Yuji Yamada, Hidetoshi Onodera

Dept. Communications and Computer Engineering, Kyoto University
{hasimoto, onodera}@i.kyoto-u.ac.jp

ABSTRACT

This paper proposes a scheme that captures diverse input waveforms of CMOS gates for static timing analysis. Conventionally the latest arrival time and transition time are calculated from the timings when a transient waveform goes across pre-determined reference voltages. However, this method cannot accurately consider the impact of waveform shape on gate delay, when crosstalk-induced non-monotonic waveforms or inductance-dominant stepwise waveforms are injected. We propose a new timing analysis scheme called "equivalent waveform propagation". The proposed scheme calculates the equivalent waveform that makes the output waveform close to the actual waveform, and uses the equivalent waveform for timing calculation. The proposed scheme can cope with various waveforms affected by resistive shielding, crosstalk noise, wire inductance etc. In this paper, we devise a method to calculate equivalent waveform. The proposed calculation method is compatible with conventional methods in gate delay library and characterization, and hence our method is easy to be implemented with conventional static timing analysis tools.

1. INTRODUCTION

As circuit scale grows, static timing analysis (STA) becomes a common approach to verify timing constraints, or rather it is currently the only way to perform full-chip timing analysis. In static timing analysis, we propagate the latest arrival time and transition time throughout a circuit and derive the longest/shortest path delays. CMOS circuits consist of CMOS gates and interconnects, and currently delay times of each part, i.e. the gate propagation delay and the interconnect propagation delay, are separately calculated. As for interconnect delay, it is well known that PRIMA [1] or other similar techniques can estimate accurate transition waveforms propagating through linear device networks. On the other hand, CMOS gates are non-linear devices and the estimation of gate delay is inherently more complicated. Therefore, delay calculation based on look-up tables is widely used [2, 3]. This approach usually requires a prior characterization process to build look-up tables using a circuit simulator. Due to the limitation of circuit simulation costs, gate characterization is usually performed in two-dimensional space; output loading and transition time of input waveform (slope). The parameter of slope aims to capture the influence of waveform shape on gate delay.

Recently many factors make transition waveforms more diverse in nano-meter technologies, such as crosstalk noise, interconnect inductance and resistive shielding, and hence capturing waveform shape by using a single parameter of slope is getting harder. Nevertheless, the number of parameters to express waveform shapes does not increase because of gate characterization costs.

This paper proposes a new propagation scheme of timing information in STA called "equivalent waveform propagation". Our scheme aims to accurately capture the effects of diverse waveforms on timing. The proposed scheme does not calculate the latest arrival time and the slope from the timings when the waveform goes across reference voltages. The proposed scheme derives an equivalent input waveform with a standard shape such that the equivalent input waveform produces an output that matches with the actual output waveform. In equivalent waveform calculation, we need to know which part of the input waveform dominantly determines the output transition. We then devise a metric to point out the important waveform region, and we develop an equivalent waveform calculation method based on the least square fitting with the devised metric. The proposed method does not change other parts of delay calculation i.e. no library extension and no additional gate characterization are necessary, and hence our method is easy to work with conventional STA methods. A preliminary evaluation result that this equivalent waveform scheme is effective in crosstalk-induced waveform is reported in Ref. [4]. However resistive shielding and inductive interconnects are not discussed. In addition, practical implementation issues, such as a tradeoff between computational time and calculation accuracy, are not reported. In this paper, we demonstrate that the proposed method can calculate the equivalent waveform with the same procedure against various waveforms, such as crosstalk-induced waveform and deteriorated waveforms with overshoot and ringing due to inductance. We also evaluate the computational costs and discuss the tradeoff between accuracy and calculation costs. Throughout this paper, we assume that the distorted input waveform applied to the gate can be obtained by other methods such as Ref. [1], and focus on the problem of finding the equivalent waveform from which we can derive the latest arrival time and the slope for gate delay calculation.

The rest of this paper is organized as follows. Section 2 points out the problem of conventional methods and proposes a concept of equivalent waveform propagation. In Section 3, we describe the method for deriving the equivalent waveform. Section 4 demonstrates that the proposed method can handle various gate input waveforms that appear in nano-meter technologies. Concluding remarks are in Section 5.

2. NECESSITY OF EQUIVALENT WAVEFORM PROPAGATION

Static timing analysis is a procedure to calculate the latest arrival time (LAT) of signal transitions at each node in a circuit and propagate it to the next gate [5]. Input waveform shape is an important factor to gate delay. Static timing analysis is condensed into accurate LAT and slope propagation. Conventionally LAT is defined as the $0.5V_{\rm dd}$ (or other threshold voltage) crossing timing. Slope is also calculated as the time difference crossing between $V_{\rm th1}$ and $V_{\rm th2}$ (e.g. $0.2V_{\rm dd}$ and $0.8V_{\rm dd}$). We hereafter refer these definitions of LAT and slope as the conventional reference-voltage-base approach.

ICCAD'03, November 11-13, 2003, San Jose, California, USA.

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM

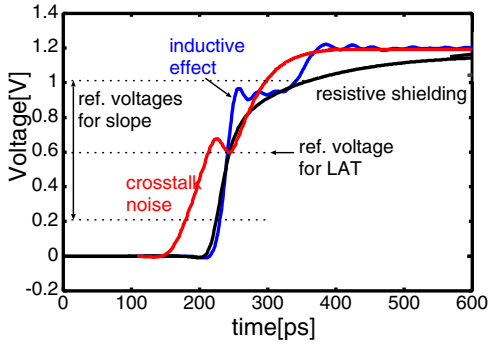

Figure 1: Diverse waveforms that have the same latest arrival time and the same slope.

2.1. Motivation

Recently there are many factors that make transition waveforms more diverse. One major factor is capacitive coupling noise, and others are on-chip inductance and resistive shielding effect. As these factors become significant, it is getting harder to capture the impact of waveform shape on gate delay using only a single parameter of slope. Even if two waveforms have the same value of slope, the waveform shapes are sometimes totally different, which results in a considerable gate delay difference. Figure 1 shows an example of waveform diversity; a crosstalk-induced non-monotonic waveform, an inductance-dominant stepwise waveform and a highly strained waveform by resistive shielding. As far as we define the latest arrival time and the slope based on the reference voltages, these three waveforms have the same latest arrival time and the same transition time and hence these waveforms are regarded as the same waveform in static timing analysis whereas the actual waveforms are much different. Needless to say, the output waveforms are much different and a considerable error of timing estimation occurs.

Gate delay calculation widely adopts table look-up models in order to consider non-linear characteristics of CMOS transistors. Typically, output load and slope of input waveform are parameters of look-up tables, and then two-dimensional tables are prepared. The tables are generated with a long process of huge amount of circuit simulation. Therefore, even if we want to increase the number of waveform parameters to express diverse waveform shape, it is prohibitively difficult to extend the table dimension due to characterization cost. Moreover, it is essentially difficult to develop a new waveform representation for such different waveforms shown in Figure 1. Considering conformity to conventional STA tools and managing characterization cost, it is highly desirable to keep the number of waveform parameter just one. This paper aims to realize accurate timing analysis while satisfying the above requirements.

From now, we demonstrate two examples that the conventional LAT and slope propagation scheme based on reference-voltage-base approach does not work well. Figure 2 shows a pair of fully-coupled interconnects. The length is 1mm. The transition waveform at the victim is affected by the transition at the aggressor. Conventional methods (e.g. Ref. [6]) evaluate the final crossing timing of $0.5V_{\rm dd}$ at Gate 2 input as LAT. The conventional methods propagate the slope of the noiseless waveform. The crosstalk-induced delay variations are evaluated by circuit simulation. We use the transistor parameters of an actual 0.13μm CMOS technology and the intermediate interconnect parameters in the 0.13μm process predicted in Ref. [7]. The wire parameters used for the experiments are coupling capacitance $C_{\rm c} = 0.058{\rm fF}/\mu{\rm m}$, capacitance to ground $C_{\rm g} = 0.096{\rm fF}/\mu{\rm m}$ and resistance $R = 0.085\Omega/\mu{\rm m}$. The supply voltage is 1.2V.

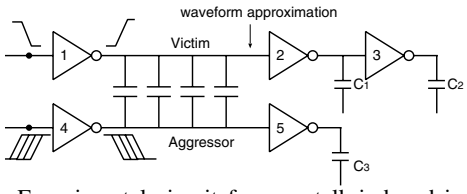

Figure 2: Experimental circuit for crosstalk-induced input waveform.

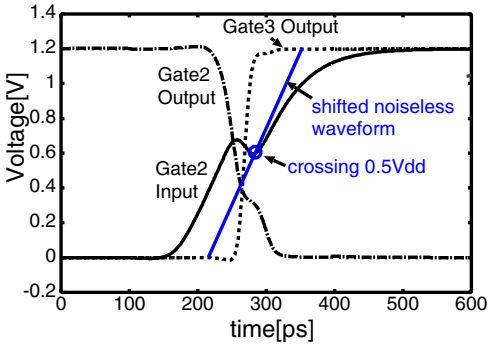

Figure 3: Crosstalk-induced waveforms that conventional method fails to handle (Gate 1, Gate 2 and Gate 3 are 4x, C1 and C2 are 1fF).

Figure 3 shows an example of transition waveforms. A noise is injected around $0.5V_{\rm dd}$. The transition waveform becomes non-monotonic and crosses $0.5V_{\rm dd}$ multiple times. On the other hand, the fall transition at Gate 2 output and the rise transition at Gate 3 output are so fast and the transition finishes before the final crossing timing of $0.5V_{\rm dd}$ at Gate 2 input, since capacitances C_1 and C_2 are not large. The conventional methods define LAT as the final crossing timing of $0.5V_{\rm dd}$. As long as we follow this definition of LAT, we never obtain the accurate output transitions at Gate 2 and Gate 3. The adjustment of the transition time (slope) does not help. In this case, output transitions of Gates 2 and 3 finish before the LAT. While clinging to the crossing timing of $0.5V_{\rm dd}$, accuracy degradation is unavoidable. This implies that we have to devise a new scheme to propagate timing information in STA.

We demonstrate another example of inductive wires. Figure 4 shows the experimental circuit. The cross section of the inductive interconnect is also shown in Fig. 4. The interconnect between Gate 1 and Gate 2 is inductive and its length is 3mm. The interconnect parameters of resistance, capacitance and inductance are $12\Omega/{\rm mm}$, $67{\rm fF}/{\rm mm}$ and $1.8{\rm nH}/{\rm mm}$. With interconnect inductance, transmission line effects appear, and the waveform becomes stepwise like in Fig. 5. This case reveals that the conventional reference-voltage-base method is incompetent. Suppose the upper reference voltage for slope evaluation is below the firstly-rising voltage like in Fig. 5. The conventional method approximates the step-wise waveform neglecting the step-wise behavior above the reference voltage. This ignorance causes the slope estimation error at Gate 2 and arrival time error at Gate 3. On the other hand, if the upper reference voltage is just above the first step voltage, the approximated waveform becomes much different. Though the output waveforms corresponding to this approximation are not described in Fig. 5 to avoid a too complicated figure, a considerable timing estimation error occurs. The approximated waveform is much sensitive to the reference voltage, and a little difference of

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM

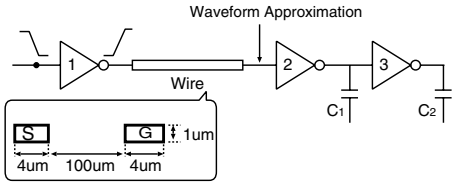

Figure 4: Experimental circuit on inductive interconnect.

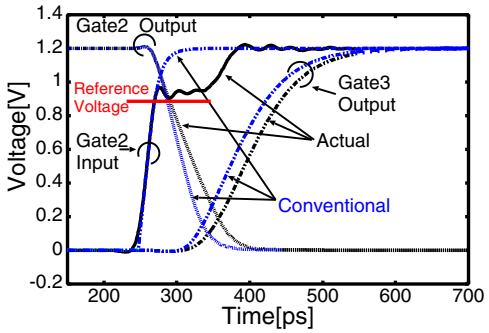

Figure 5: An example of inductive interconnect (Gate 1 is 5x, Gate 2 and Gate 3 are 4x, wire length is 3mm, and C1 and C2 are 200fF.).

reference voltage is confronted with the discontinuous waveform approximation. As long as the reference-voltage-base method is used, we cannot escape from this problem. Therefore, we have to devise a new waveform propagation scheme that is independent of reference voltage definitions.

2.2. Previous Work

Recently the problem of crosstalk noise discussed in Sec. 2.1 is raised in Ref. [8]. Reference [8] estimates the output transitions against noisy input waveforms using look-up tables. This look-up table has two additional parameters of noise width and noise height as well as load and input slope. This method requires a prior gate characterization process and it is one of the disadvantages. But the true problem is that this method can only cope with crosstalk noise and it cannot provide accurate timing analysis against other types of waveforms; such as a waveform with resistive shielding and a waveform in an inductance-dominant interconnect. In addition, it is not clear if this method can cope with multiple aggressors. One solution is increasing another parameter to express waveform shape. However, the cost of gate characterization increases exponentially according to parameter addition. Another method is proposed in Ref. [9]. It basically evaluates delay variation by circuit simulation and hence it is not suitable for large circuits. As far as we investigate, no methods provide a complete solution against the waveform diversity problem in STA discussed in Sec. 2.1, and this paper is a first attempt to tackle and solve this problem.

2.3. Equivalent Waveform Propagation and Its Goal

We propose a new scheme called "equivalent waveform propagation" so as to perform timing analysis overcoming the problems discussed so far. The proposed scheme derives the equivalent waveform such that the output waveforms of the gate match in both cases that the equivalent and actual waveforms are given to the gate input. This concept is shown in Figure 6. The big difference from the reference-voltage-base approach is that the $0.5V_{\rm dd}$ crossing timing of the equivalent waveform is not necessary the same with that of the actual waveform, whereas the conventional

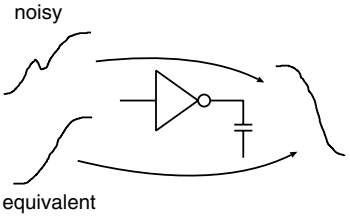

Figure 6: Proposed concept of equivalent waveform.

method clings to estimate the accurate $0.5V_{\rm dd}$ crossing timing. Without the restriction of $0.5V_{\rm dd}$, the expression freedom of the equivalent waveform expands considerably, which enables the accurate propagation of timing information. Here the issue is how to derive the equivalent waveform.

In order to keep the compatibility with conventional STA tools, we must avoid increasing table parameters. To cope with various waveforms, we should devise a generic method that is independent of injected waveform shapes. The expression of the equivalent waveform shape must be a typical waveform such that a CMOS gate drives a capacitive load, because most of gates in a circuit drive capacitive load and then gate characterization is performed assuming the typical waveforms. In the following section, we propose a waveform calculation method that can derive an equivalent waveform with small computational cost while keeping the compatibilities with conventional STA tools.

3. EQUIVALENT WAVEFORM CALCULATION

The previous section revealed that the conventional slope propagation scheme based on reference voltages does not work against diverse waveforms. We then proposed a concept of equivalent waveform propagation that is potentially able to cope with diverse waveforms. In this section, we propose a heuristic method to calculate an equivalent waveform. Practical implementation issues, such as integral calculation, are also discussed.

3.1. Least Square Method Focusing on Critical Waveform Region

The problem to derive the equivalent waveform is to find the arrival time and the slope that produce an output waveform that matches with the actual output waveform. The important thing is the equivalent waveform depends not only on the input waveform shape but also on the output behavior. Let us recall the example of Fig. 3. The significant estimation error in this situation comes from the fast output transitions at Gate 2 and Gate 3. When output load is large or when gate driving strength is weak, the output transitions become slow and the injected noise affects the output transition waveform. The aspect of error occurrence is totally different. We thus have to consider the output transitions.

One of straightforward methods to derive arrival time and slope is the least square method (LSM). However, a simple LSM just approximates the input waveform and it does not consider any information on output transitions. Figure 7 shows a typical example that the simple LSM fails. Although the output transition almost finishes before noise injection, the LSM derives the approximated waveform that is close to the entire actual waveform.

The key issue of equivalent waveform derivation is how to find a critical region that strongly affects the output waveform. As an heuristic metric to extract a critical region, we propose to use $\partial v_{\rm out}/\partial v_{\rm in}$, which is the output voltage ($v_{\rm out}$) gain subject to input voltage ($v_{\rm in}$). The left figure in Fig. 8 shows the input

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM

waveform $v_{\rm in}$ and the output waveform $v_{\rm out}$ in time domain. The right figure represents the relation between $v_{\rm in}$ and $v_{\rm out}$. The metric $\partial v_{\rm out}/\partial v_{\rm in}$ means the slope of the curve in the right figure. When the metric is small, $v_{\rm in}$ scarcely varies the output voltage. Conversely, when the metric is large, slight change of $v_{\rm in}$ affects $v_{\rm out}$ considerably. With this metric, we can effectively extract the critical waveform region.

The metric $\partial v_{\rm out}/\partial v_{\rm in}$ is transformed as follows:

$$\frac{\partial v_{\rm out}}{\partial v_{\rm in}} = \frac{\partial v_{\rm out}}{\partial t} \cdot \frac{\partial t}{\partial v_{\rm in}} = \frac{\partial v_{\rm out}}{\partial t} \cdot \frac{1}{\partial v_{\rm in}/\partial t}. \qquad (1)$$

We can calculate the value of $\partial v_{\rm out}/\partial v_{\rm in}$ from $v_{\rm in}(t)$ and $v_{\rm out}(t)$. Here the gain curve obtained by DC analysis is different with Eq. (1), because DC analysis cannot consider the conditions of output loading and driving strength. Static timing analysis methods usually have the waveforms of $v_{\rm in}(t)$ and $v_{\rm out}(t)$ irrespective of gate delay models, e.g. k-factor (non-linear) model [2] or Thevenin equivalent circuit model [3]. Rigidly speaking, $v_{\rm out}(t)$ can be built from the information on propagation delay and output slope when k-factor (non-linear) model is used. Therefore, no additional information is necessary to calculate the metric.

We then devise an improved objective function of the least square method using the metric of $\partial v_{\rm out}/\partial v_{\rm in}$ as

$$\int_{t_1}^{t_2} \left| \frac{\partial v_{\rm out}}{\partial v_{\rm in}}\Big|_{v_{\rm in}=g(t)} \right| \{f(t) - g(t)\}^2 dt, \qquad (2)$$

where $g(t)$ is the actual waveform of gate input and $f(t)$ is the equivalent waveform. Times t_1 and t_2 are decided such that the time region between t_1 and t_2 includes the input signal transition completely. We search the equivalent waveform that minimizes Eq. (2) with two variables of arrival time and slope of $f(t)$. Please note that the expression of $f(t)$ should be the same with the waveform used in gate characterization, but the proposed method does not limit the expression itself. We can use ramp, exponential or their mixed expressions as far as a single parameter expresses waveform shape.

The procedure of our method is summarized as follows.

1. Calculate the approximated input waveform by the conventional reference-voltage-base approach. In this step, noiseless transition waveform is used.
2. Calculate the output waveform corresponding the approximated input waveform using look-up tables. The metric of $\partial v_{\rm out}/\partial v_{\rm in}$ is calculated using the input and output waveforms derived in Step 1 and Step 2.
3. Set the input waveform calculated in Step 1 as the initial approximated waveform, and minimize Eq. (2).

The proposed method does not need any additional information, and uses the only information that every STA tool already has. Our method requires no library extension and no additional gate characterization. Therefore, our method is easy to be implemented into existing static timing analysis tools.

3.2. Integration Issues

In Step 3, we execute integration in the time range from t_1 to t_2. When the functional expression both of $f(t)$ and of $g(t)$ are known and we use a series expansion technique, we can calculate Eq. (2) without numerical integration. We think this situation is common. Because when we calculate the actual waveforms by using PRIMA

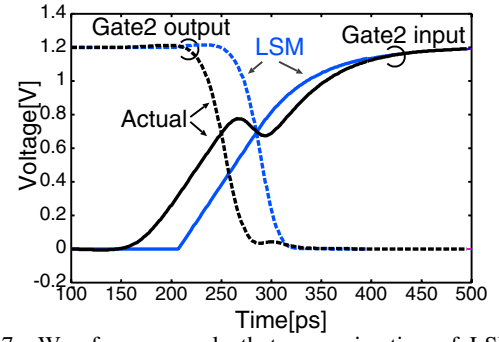

Figure 7: Waveform example that approximation of LSM fails. (Gate 1 is 4x, Gate 2 and Gate 3 are 3x, C and C2 are 1fF).

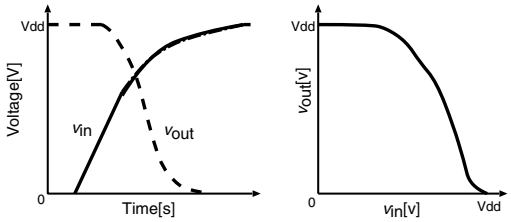

Figure 8: Input and output waveforms in time domain (left figure), and relationship between gate input and output voltages (right figure).

[1], or other similar techniques, the typical waveform expression consists of several exponential and linear terms, which are easy to be integrated. On the other hand, when $f(t)$ cannot be defined as an expression, or when the series expansion of $f(t)$ is difficult, we should perform numerical integration.

When we cannot avoid performing numerical integration, tighter integral range without accuracy degradation is desirable from the point of computational cost. As for t_1, it is reasonable to set t_1 to the timing when the input transition starts. The problem here is how to decide t_2. Now we want to compute the equivalent waveform to the actual input waveform, and hence we do not have to pay much attention to the time region after the input transition finishes. From another point of view, we want to match the output waveforms corresponding to the actual and the equivalent input waveforms. Therefore, the input waveform in the time region after the output transition finishes is also unimportant. Getting two points of view together, we should choose the earlier timing from (1) the input transition finishes and (2) the output transition finishes. When crosstalk noise is induced, we add the noise width to t_2, because the crosstalk-induced delay increase is at most the noise width. The definition of noise width is found in Ref. [10]. We experimentally verify that this policy is reasonable and helpful to reduce computation cost on numerical integration in the next section. We also discuss the number of split segments in numerical integration.

4. EXPERIMENTAL RESULTS

We experimentally verify the proposed method on three conditions; crosstalk noise is induced, resistive shielding is prominent, and wire inductance is dominant.

We first explain the expression of equivalent waveform used in the experiments. We use a waveform expression composed of a linear function(0–60%) and an exponential function (60%–) with a single parameter of T_{12} [11]. The parameter of T_{12} is originally defined as the crossing time difference between $0.4V_{\rm dd}$ and

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM

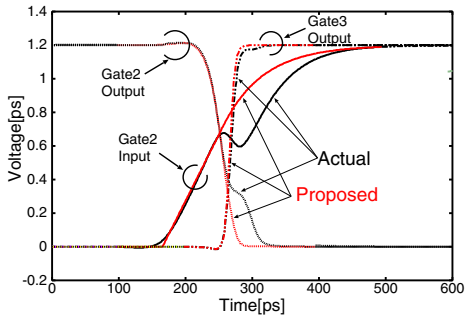

Figure 9: Crosstalk-induced waveforms (in the same condition with Fig. 3).

$0.6V_{\rm dd}$. The rise waveform $f_{\rm rise}$ is expressed as

$$f_{\rm rise} = \begin{cases} 0 & 0 \le t \le t_{\rm s}, \\ V_{\rm dd}\frac{0.2(t-t_{\rm s})}{T_{12}} & t_{\rm s} < t \le t_{\rm s} + 3T_{12}, \\ V_{\rm dd}(1-0.4e^{-\frac{t-3T_{12}-t_{\rm s}}{2T_{12}}}) & t_{\rm s}+3T_{12} < t, \end{cases} \quad (3)$$

where $V_{\rm dd}$ is the power supply voltage and $t_{\rm s}$ is the offset time when the voltage begins to rise. We experimentally verify that this expression is close to actual transition waveforms as far as a single parameter is used, and hence we adopt this expression as the shape of the equivalent waveform. Please note that the proposed scheme of equivalent waveform propagation is independent of the waveform definition as explained in Sec. 3.1. Other waveform expressions also can be used as the equivalent waveform expression.

4.1. Capacitive Coupling

We first evaluate the accuracy of the proposed method against crosstalk-induced noisy waveforms. Figure 2 shows the experimental circuit. We assume that the accurate noise waveforms are given by some existent methods. We suppose that the conventional method propagates the final timing of crossing $0.5V_{\rm dd}$ and the slope of the noiseless waveform in STA. We evaluate both the proposed method and the conventional method. Figure 9 shows the result in the same condition of Fig. 3. The derived equivalent waveform and the actual waveform do not cross each other at the final timing when the actual waveform crosses $0.5V_{\rm dd}$, as we expected. The proposed method focuses on the important region before the fall transition at Gate 2 finishes. Thus, the proposed method overcomes the drawback of the simple least-square fitting shown in Fig. 7.

We next evaluate the crosstalk-induced variation of the propagation delay from Gate 2 input to Gate 3 output, and we verify the estimation accuracy of delay variation. The transition timing of the aggressor(Gate 4) input is varied with 10ps time step. This means that the timing of noise injection is changed with 10ps time step. The transition time of the aggressor input is 100ps. We change the timing of inducing noise waveform, driver strength of each gate and the values of C_1, C_2 and C_3.

Figure 10 shows one of experimental results. The horizontal axis is the timing of noise injection, and the vertical axis is the variation of delay time caused by crosstalk noise. The curve evaluated by the conventional method changes drastically although the actual curve changes smoothly. This drastic change comes from the conventional definition of the latest arrival time. The latest arrival time varies discontinuously even though the crosstalk-induced waveforms are almost the same. The conventional method thus has a serious problem. On the other hand, the proposed method estimates the delay variation curve as we expected. The maximum estimation error of delay variation is reduced from 32ps to 3ps. Similar results are obtained under other configurations of experiments. We can see that the proposed method can estimate the impact of noisy input waveform on timing.

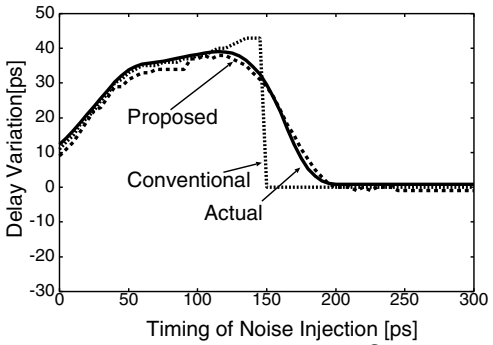

Figure 10: Crosstalk-induced delay variation (Gate 1 is 4x, Gate 2 is 4x, C1 and C2 are 100fF).

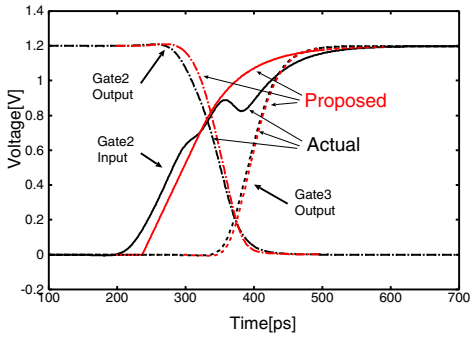

Figure 11: Equivalent waveform derivation when two aggressors exist.

We also verify the effectiveness of the proposed method against the interconnect with two aggressors. Figure 11 shows the result. As you see, the proposed method works well in the same procedure even when there are multiple aggressors.

4.2. Resistive Shielding

We examine the effectiveness of the proposed method in resistive shielding. The experimental circuit is shown in Fig. 12. We assume intermediate interconnects in the 0.10μm process predicted by ITRS [7]. The interconnect parameters of resistance and capacitance are $0.74\Omega/\mu$m and 0.20fF$/\mu$m. The interconnect length between Gate 1 and Gate 2 is 100μm. The length of the branch part, i.e. the interconnect between Gate 1 and Gate 4, is varied and the variations are $100, 500, 1000, 2000$ and 3000μm. This branch interconnect strains the input waveform of Gate 2. Gate 1 is 4x or 8x inverter. Gate 2 and Gate 3 are 1x or 4x inverters, and the load capacitances C_1 and C_2 are 1, 10, 50 or 100fF. The total number of evaluation is 80. The maximum error of the proposed method is 15ps, whereas that of the conventional method is 31ps. The proposed method reduces the amount of error by more than 50%. Figure 13 shows an example that the conventional method does not work well. As you see, the output waveform of Gate 3 using the proposed method is very close to the actual waveform. However, the conventional reference-voltage-base method causes 16ps error. When resistive shielding is significant, the proposed equivalent-waveform scheme provides more accurate timing analysis than the conventional method.

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM

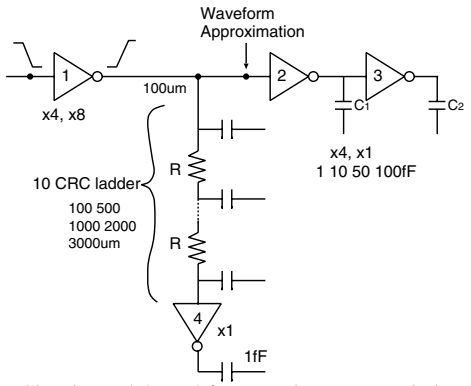

Figure 12: Circuit model used for experiment on resistive shielding.

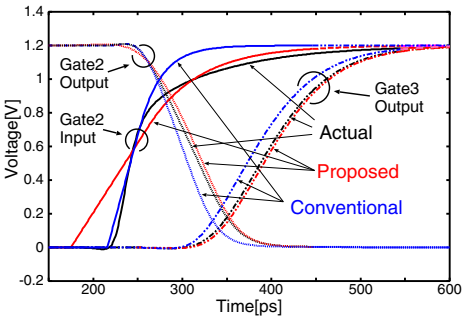

Figure 13: Waveform example that proposed method well captures input waveform (Gate 1 is 8x, Gate 2 and Gate 3 are 1x, C1 and C2 are 50fF, branch length is 1mm).

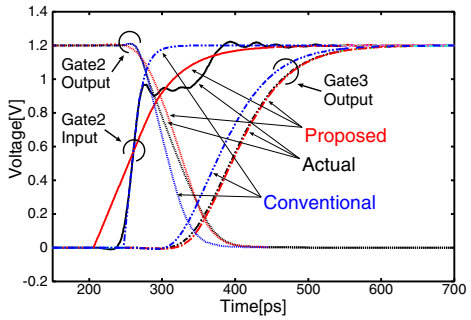

Figure 14: Equivalent waveform calculation against inductive interconnect (Gate 1 is 5x, Gate 2 and Gate 3 are 4x, wire length is 3mm, C1 and C2 are 200fF.).

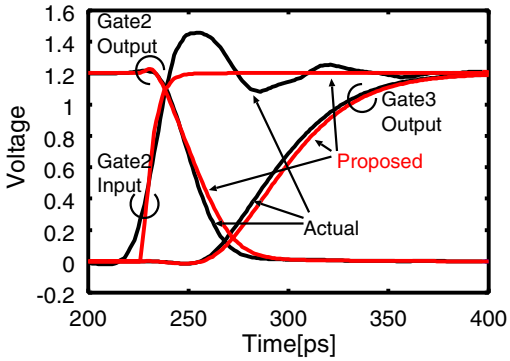

Figure 15: A ringing case (Gate 1 is 16x, Gate 2 and Gate 3 are 4x, wire length is 3mm, C1 and C2 are 100fF.).

4.3. Inductive Interconnects

Gate input waveforms become more complicated when interconnect inductance is dominant. We experimentally verify the effectiveness against inductive interconnects. The experimental condition is the same with Sec. 2.1. The proposed method and the conventional reference-voltage-base method are evaluated.

We show the result in Fig. 14. The gate input waveform is bent after passing the reference voltage of $0.6V_{\rm dd}$, so the reference-voltage-base method cannot capture the stepwise waveform well. On the other hand, thanks to the metric of $\partial v_{\rm out}/\partial v_{\rm in}$, the propose method can capture the change of input waveform. The timing estimation error is reduced from 20ps to 2ps by the proposed method.

We vary the driving strength of Gate 1 and evaluate the accuracy under several conditions. We confirm that the proposed method provides accurate output waveforms. However, we find a case that the accuracy of our method may be degraded slightly. Figure 15 shows a typical case. There is an overshoot at Gate 2 input. The proposed method sets t_2 in Eq. (2) as the first crossing timing of $V_{\rm dd}$ and calculates the equivalent waveform. Since the gate voltage becomes over $V_{\rm dd}$ after t_2, the fall output transition of Gate 2 is accelerated, which results in a small error of timing estimation at Gate 3 output.

4.4. Accuracy vs. #Segments in Integration

The calculation of Eq. (2) in equivalent waveform derivation can be done analytically if waveform expressions are easy to be integrated and/or we use a series expansion technique. However, in a more generalized case, numerical integration is performed. In this case, the integral region of Eq. (2), the number of segments used in numerical integration and the accuracy are tightly related. We here examine this relationship. The relation between #segments and computation costs is discussed in the next section.

Section 3 discusses the integral region of Eq. (2) and explains how to decide t_2. We verify that this decision method is proper. The proposed method determines $t_2 = \min(t_{\rm in}, t_{\rm out})$ to integrate Eq. (2) in necessary and sufficient region, where parameter $t_{\rm in}$ ($t_{\rm out}$) is the timing when the input (output) voltage swings by $0.9V_{\rm dd}$. We evaluate the accuracy varying #segments used for integration. We also evaluate another candidate of $t_2 = \max(t_{\rm in}, t_{\rm out})$ for comparison. We here assume a waveform strained by resistive shielding. When #segments is three, the error is reduced from 10ps to 3ps by choosing the earlier timing. When the given error limit is below 3ps, six segments are necessary if we do not select the earlier timing. The proposed decision method of t_2 thus helps to improve accuracy and to reduce calculation costs.

We next evaluate the number of required segments. We assume two types of waveforms; output load is purely capacitive and resistive shielding is significant. Table 1 shows the relationship between the accuracy and #segments. The column "Conventional" represents the error when the conventional reference-voltage-base method is used. When resistive shielding is negligible, the required number of segments is only three. This is consistent with the fact that the conventional reference-voltage-base approach worked well so far. However the effect of resistive shielding becomes strong, the conventional method fails and the error is over 10%. On the other hand, the proposed method with eight-segment-integration achieves small error of 1%.

The above discussion supposes that crosstalk noise is not in-

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM

Table 1: Error[%] vs. #segments for waveforms w/ and w/o resistive shielding.

	Proposed(#segments)					Conventional
	3	5	8	10	40	
w/o res. shielding	1.6	1.6	0.0	0.0	0.0	1.9
w/ res. shielding	11.3	7.3	1.0	0.3	0.3	10.9

Table 2: Calculation costs of proposed method. Each value is normalized by cost of conventional STA.

#segments	3	5	10	20	40
calculation costs	1.12	1.17	1.27	1.48	1.71

duced. In order to capture the effect of crosstalk noise, we need some evaluation points while noise is injected. We then decide #segments according to the noise width. In our experiment, four to five evaluation points are adequate. We have two requirements of time step Δt in numerical integration; the time step decided by the transition waveform without crosstalk noise Δt_{tran}, and the time step determined by the crosstalk noise width Δt_{noise}. We then choose $\Delta t = \min(\Delta t_{tran}, \Delta t_{noise})$.

4.5. Computation Costs vs. #Segments in Integration

We implement the proposed method into a STA tool and evaluate the calculation costs. Followings are the delay calculation procedure of the implemented STA tool. Gate delay calculation is executed using Thevenin equivalent circuit model [3]. Interconnect RC trees are once reduced into a π circuit [12], and it is used to calculate effective capacitance [13] and gate output waveform. The output waveforms of interconnects are calculated from gate output waveform and quadratic transfer function. The transfer function is calculated by Ref. [14]. In minimizing Eq.(2), three to five iterations are needed.

We evaluate the computational costs of the proposed method. Please note that in this evaluation we execute numerical integration of Eq. (2) as the worst case. When we can calculate Eq. (2) analytically, the calculation cost increase is much less. The circuit used for the experiment is a simple circuit of inverter chain. Table 2 shows the experimental results. The calculation cost is normalized by that of the conventional reference-voltage-base implementation. We here evaluate the calculation time purely required for timing propagation excluding the time of reading and writing files and RC reduction. When resistive shielding is not significant and crosstalk noise is not injected, the required number of segments is three and it corresponds to 12% increase of computation costs. When resistive shielding is significant, the increase is about 25%. As far as we investigate, the required number of segments for crosstalk-induced waveform is around ten to fifteen. We then conclude that the proposed method can provides accurate timing analysis with CPU time increase of 15 to 30% at most.

5. CONCLUSION

In this paper, we propose a new scheme called "equivalent waveform propagation" to capture diverse gate input waveforms in accurate gate delay calculation. In order to realize the proposed scheme, we develop an equivalent waveform calculation method based on the least square method. With the metric developed to extract critical region of a waveform shape, the proposed calculation method can derive the equivalent waveform successfully. The proposed method requires no library extension and no additional characterization, which means the high conformity of our method to conventional STA tools. We experimentally verify that the proposed method is more accurate in delay calculation than conventional reference-voltage-base approach under various conditions; resistive shielding is significant, crosstalk noise is injected, and interconnects are inductive. The proposed scheme of "equivalent waveform propagation" is promising in nano-meter technologies.

6. ACKNOWLEDGEMENT

This work is supported in part by the 21st Century COE Program (Grand No. 14213201).

7. REFERENCES

[1] A. Odabasioglu, M. Celik and L. T. Pileggi, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," *Proc. ICCAD*, pp.58–65, 1997.

[2] N. H. E. Weste, K. Eshraghian, "Principles of CMOS VLSI Design, 2nd edition," *Addison-Wesley Publishing Company*, 1992.

[3] F. Dartu, N. M. Menezes and L. T. Pileggi, "Performance computation for precharacterized CMOS gates with RC-loads," *IEEE Trans. CAD*, pp.544–553, 1996.

[4] M. Hashimoto, Y. Yamada and H. Onodera, "Capturing Crosstalk-Induced Waveform for Accurate Static Timing Analysis," *Proc. ISPD*, pp.18-23, 2003.

[5] R. B. Hitchcock, G. L. Smith and D. D. Cheng, "Timing Analysis of Computer Hardware," *IBM Journal of Research and Development*, Vol. 26, No. 1, pp.100-105, January 1982.

[6] K. Agarwal, Y. Cao, T. Sato, D. Sylvester and C. Hu, "Efficient Generation of Delay Change Curves for Noise-Aware Static Timing Analysis," *Proc. ASP-DAC*, pp.77-84, 2002.

[7] Semiconductor Industry Association, International Technology Roadmap for Semiconductors, 2001.

[8] S. Sirichotiyakul, D. Blaauw, C. Oh, R. Levy, V. Zolotov and J. Zuo, "Driver Modeling and Alignment for Worst-Case Delay Noise," *Proc. DAC*, pp.720-725, 2001.

[9] Y. Sasaki and G. D. Micheli, "Crosstalk Delay Analysis using Relative Window Method," *Proc. ASIC/SOC Conference*, pp.9-13, 1999.

[10] J. Cong, D. Z. Pan, and P. V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization," *Proc. ASP-DAC*, pp.373-378, 2001.

[11] F. Chang, C. Chen and Prasad Subramaniam, "An Accurate and Efficient Gate Level Delay Calculator for MOS Circuits," *Proc. DAC*, pp.282–287, 1988.

[12] P. R. O'Brien and T. L. Savarino, "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation," *Proc. ICCAD*, pp.19–25, 1992.

[13] C. Cheng, J. Lillis, S. Lin and N. H. Chang, "Interconnect Analysis and Synthesis," *A Wiley Interscience Publication*, 2000.

[14] X. Yang, C. -K. Cheng, W. H. Ku and R. J. Carragher, "Hurwitz Stable Reduced Order Modeling for RLC Interconnect Trees," *Proc. ICCAD*, pp.222–228, 2000.

Proceedings of the International Conference on Computer Aided Design (ICCAD'03)
1092-3152/03 $ 17.00 © 2003 ACM