Representative Frequency for Interconnect R(f)L(f)C Extraction

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Abstract— This paper discusses the frequency to extract RLC values from interconnects. The frequency used for RLC extraction affects the accuracy of interconnect characterization, and hence careful determination of extraction frequency is crucial. We propose a representative frequency for RLC extraction based on the interconnect length. We show that the proposed method enables accurate analysis of the waveform at the far-end of interconnects. We verify that the extraction at the proposed frequency provides the most accurate transition waveform against various input signals and interconnect structures in digital circuits.

I. Introduction

As increasing operating frequency, frequency-dependence of interconnect characteristics is becoming significant. Interconnect characteristics, especially resistance and inductance depend on frequency because of skin-effect and proximity effect. In frequency-dependent interconnects, the behavior of interconnects depends on frequency e.g. attenuation and phase velocity dispersion. In digital circuits, common input waveform of interconnects are trapezoidal pulses. A trapezoidal pulse contains frequency components from DC to ∞. Moreover, the input pulse pattern is not entirely periodic. The frequency spectrum varies depending on the width of pulse and the period. The minimum pulse width and period are determined by system clock. But on signal line, the pulse pattern depends on the circuit behavior.

To treat frequency-dependent interconnects, several circuit models are proposed [1–3]. The frequency-dependent models improve simulation accuracy [2, 4], but in circuit design, frequency-dependent models are not used so commonly. Because most of conventional design methods are based on the frequency-independent model.

If interconnect characteristics can be modeled well by a single frequency, we can use the design techniques proposed so far, e.g. circuit reduction, buffer insertion and timing analysis [5, 6]. Furthermore, frequency-independent RLC values can intuitively predict fundamental interconnect characteristics such as characteristic impedance. We can also save the cost to extract RLC value from DC to high frequency. However, determination of a single extraction frequency is difficult.

In Ref. [7], the impact of a frequency-dependent model is discussed. A frequency-dependent model is compared with an equivalent circuit extracted at DC from the viewpoint of signal delay, crosstalk noise and so on. Ref. [7] reports that a frequency dependent model is necessary for crosstalk noise estimation. However the authors examine only a DC extracted model and frequency dependent model. Therefore it is not clear whether crosstalk can be estimated using a frequency-independent model extracted at a certain representative frequency.

In this paper, the extraction frequency based on the interconnect length is proposed. It is commonly adopted to determine the representative frequency from the shape of an input signal waveform, especially from the rise time, focusing on the spectrum of the input signal. This is natural and reasonable when we analyze the incident waveform to the near-end of the interconnects. On the other hand, our main interest is the analysis of the waveform at the far-end. As signals are propagating through an interconnect, high-frequency components are easy to attenuate. The dominant frequency components that determine the far-end waveform are different from those for the near-end waveform. We observe that accurate estimation of attenuation behavior is crucial to obtain accurate far-end waveforms. Open-ended transmission-lines can be treated as resonator and transmission-line resonators are used in microwave circuits. An on-chip transmission-line with CMOS receiver can be regarded as a resonator. From the theory of a resonator, the frequency where attenuation becomes minimum is decided by the interconnect length. We reveal that this resonance frequency is the dominant frequency to characterize far-end waveforms, and then propose to adopt it as the representative frequency used for interconnect RLC extraction. We experimentally verify that the most accurate waveform is obtained when the proposed frequency is used for extraction. We show that the maximum errors in our experiments are below 8% in the voltage amplitude, signal delay and the amplitude of crosstalk noise. Therefore the proposed frequency enables accurate transient analysis using frequency-independent interconnect model.

In Section II, interconnect modeling and its problems are described. We next discuss the extraction frequency in digital circuits. We then show the experimental results in Section IV. Section V concludes the discussion.

II. Problem Description

This section describes the problem discussed in this paper. We first show frequency-dependence of interconnect characteristics and demonstrate its impact on transient analysis.

A. Frequency-Dependence of Interconnect Characteristics

Frequency-dependence of interconnect characteristics is mainly caused by skin-effect and proximity effect. So the characteristics variation is strongly related with the interconnect structure as well as the frequency. Skin effect and proximity effect are remarkable on wide and thick interconnects. Because, skin depth becomes comparable to the interconnect size in relatively lower frequency.

Figure 1 shows an example of resistance and inductance characteristics. The resistance and inductance values are calculated by a field-solver [8]. The assumed interconnect structure is co-planar, and the width of the signal line is 10μm, the width of the ground line is 20μm and their spacing is 2μm. In this case, the resistance increases by 10% from DC to 1.2GHz, and the inductance decreases by 10% from DC to 1.9GHz. The resistance and the inductance start changing from relatively low frequency of 1 to 2GHz, and thus frequency-dependence is not negligible to model interconnects in current high-performance circuits any longer.

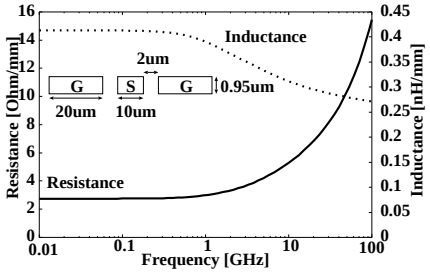

Fig. 1. Frequency-dependence of resistance and inductance. (co-planar structure, signal line width 10μm, ground line width 20μm, spacing 2μm)

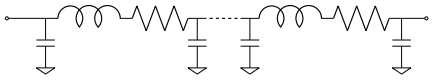

Fig. 2. RLC ladder circuit model.

B. Interconnect Models and their Impact on Waveform

Generally, interconnects in VLSIs are expressed by lumped RLC for circuit design. To model long interconnects that have transmission line characteristics, an RLC ladder circuit as Figure 2 is used. This ladder model cannot consider the frequency-dependence of interconnect characteristics. A number of frequency-dependent models are proposed [1–3]. In this paper, we use the model of Ref. [3] as a golden frequency-dependent model. It is implemented in HSPICE [9] as w-element model. In interconnect design, characteristic parameters such as characteristic impedance and attenuation constant are essential factors for designers. Although frequency-dependent models such as Ref. [3] can provide accurate waveforms, circuit designers can not know such parameters that should be used for circuit design, because such parameters are also freqency dependent. We therefore have to determine a single frequency to specify the characteristic impedance, attenuation constant and so on. As mentioned in Section I, the frequency spectrum of propagating signal depends on circuit behavior, so it is difficult to specify the most representative frequency from the frequency spectrum. This paper proposes a method to determine the representative frequency.

Figure 3 shows the impact of frequency-dependence on transient analysis. The simulated circuit is shown in Figure 3. The interconnect shown in Figure 1 is driven by a voltage source and a resistor $R_{\rm d}$ that correspond to a CMOS driver. Interconnect characteristic impedance Z_0 is 55Ω and the output impedance of the driver $R_{\rm d}$ is 10Ω. The solid line labeled "FD" shows the voltage waveform at the far-end by the frequency-dependent model. In this paper, we use "FD" as the abbreviation of "Frequency-Dependent model". The dashed lines labeled "DC" and "$f_{\rm sig}$" are the results of frequency-independent models. "DC" means the RLC ladder model extracted at DC, and "$f_{\rm sig}$" corresponds to RLC extraction at the significant frequency [6]. The number of ladder is 51. Significant frequency is one of a representative frequency defined from the frequency components of a trapezoidal pulse, and it is explained in the next section. As you see, both waveforms of the conventional frequency-independent models ("DC" and "$f_{\rm sig}$") are far from that of frequency-dependent model ("FD"). When R and L are extracted at DC, the extracted resistance is too low, and, the resistance extracted at significant frequency is too high. From the above observations, we can expect that a frequency between DC and significant frequency provides the waveform that is close to the waveform of the frequency-dependent model. If

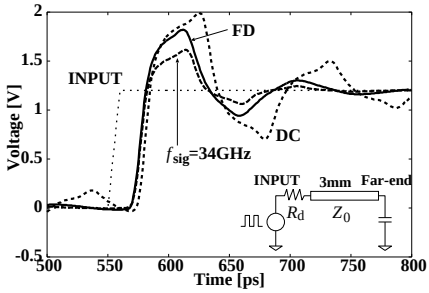

Fig. 3. The impact of frequency-dependence. (interconnect structure is shown in Figure 1, $Z_0 = 55\Omega$, $R_{\rm d} = 10\Omega$)

the representative frequency can be determined systematically, we can model interconnects by a single frequency. In the following section, we discuss the way to determine the representative frequency to model interconnects at a single frequency.

III. Representative Frequency for Extraction

In this section, we discuss the representative frequency to extract interconnect RLC. Conventionally, frequency determined from input pulse is used for interconnect extraction. We first explain some representative frequencies conventionally used for extraction, and we then propose the representative frequency calculated from interconnect length.

A. Conventional Methods

In digital circuits, a trapezoidal pulse that contains multiple frequency components is a common waveform. In order to derive frequency-independent model of Figure 2, we have to choose a single extraction frequency.

There are several representative frequencies of periodic pulse waveform. One of them is significant frequency [6]. Significant frequency is expressed by signal transition time $t_{\rm r}$. The significant frequency $f_{\rm sig}$ is defined such that the signal energy from DC to $f_{\rm sig}$ becomes 75% of all signal energy. In the range $7 \leq T_{\rm w}/t_{\rm r} \leq 13$, $f_{\rm sig}$ is given by $0.34/t_{\rm r}$ [6]. On the other hand, DC is often used for extraction. Ref. [7] concludes that the extraction at DC is accurate enough to estimate signal delay and overshoot/undershoot. DC extraction is enough when frequency-dependence is weak, e.g. narrow interconnects or low frequency. But as shown in Figure 3, RLC ladder extracted at DC or the significant frequency causes considerable amount of errors in transient analysis.

B. Proposed Method

Conventional methods based on input pulse shape focus on the frequency components at the near-end of interconnects. However the far-end waveform is more important for circuit designer because the waveform directly affects signaling delay. The far-end waveform becomes totally different because of attenuation and reflection. We propose an extraction frequency that aims to express accurate far-end waveforms. Figure 4 shows step responses obtained with a FD model and a ladder extracted at significant frequency $f_{\rm sig}$. The experimental setup is the same as Figure 3. As shown in Figure 4, the ladder extracted at $f_{\rm sig}$ models the incident wave of interconnects well, but a remarkable error occurs at the far-end. This error is mainly caused by overestimation of attenuation. On transmission-lines, characteristic impedance and attenuation constant are important factors which decide the waveform at

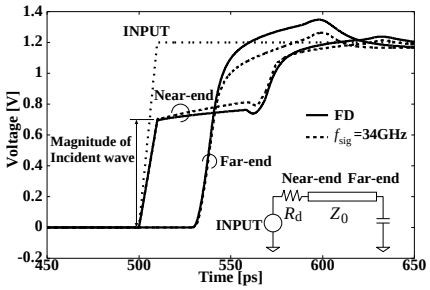

Fig. 4. Waveform at near-end and far-end. (interconnect structure is shown in Figure 1, $Z_0 = 55\Omega$, $R_{\rm d} = 10\Omega$)

the far-end. Approximately, characteristic impedance is expressed as $Z_0 = \sqrt{L/C}$ and is proportional to square root of inductance $\sqrt{L}$. The attenuation constant α is expressed as $\alpha = R/2Z_0$. The attenuation constant is roughly proportional to resistance R and square root of inductance $\sqrt{L}$. From the above observation, variation of resistance strongly affects waveform propagation. Moreover, as shown in Figure 1, the variation of resistance is larger than that of inductance. At 34GHz of Figure 1, inductance decreases by about 30% from DC and resistance increases by about 230% from DC. The inductance decreases because of proximity effect and the internal-inductance decreasing. Therefore the inductance value saturates at high frequency. On the other hand, resistance increases exponentially as frequency become higher. Therefore the estimation of resistance is crucial to analyze far-end waveform. The attenuation strongly depends on interconnect structure such as interconnect length. From above discussion, we have to consider interconnect structure when determining an extraction frequency.

To determine an extraction frequency from the viewpoint of the waveform at the far-end, we have to specify the dominant frequency component at the far-end. From the theory of open-ended transmission-line resonators, when the quarter wavelength $\lambda/4$ is equal to interconnect length l, transmission-lines are equivalent to a series resonator shown in Figure 5. When quarter wavelength $\lambda/4$ is equal to interconnect length l, the frequency $f_{\rm res}$ is expressed by

$$f_{\rm res} = c/\lambda = c/4l, \tag{1}$$

where c is the velocity of electromagnetic wave. When the frequency is $f_{\rm res}$, the impedance of series resonator become minimum and the attenuation of frequency component $f_{\rm res}$ is minimum. Figure 6 shows a transfer characteristic of a transmission-line. The interconnect structure is the same as Figure 1 and interconnect length is 5mm. The relative permittivity of SiO_2 is 4.0, so the velocity of electromagnetic wave is 1.5×10^8 m/s. In this case, resonance frequency $f_{\rm res}$ is 7.5GHz. The voltage gain becomes maximum at the resonance frequency $f_{\rm res}$. Therefore the frequency component $f_{\rm res}$ strongly affects the waveform at the far-end. The frequency spectrum at the far-end is as shown in Figure 7 when a transmission-line is driven by a voltage source and a resistor. The frequency $f_{\rm res}$ is the first peak of frequency components regardless of various transition times. We hence consider the frequency $f_{\rm res} = c/4l$ as a representative frequency. In LSIs, the phase velocity of electromagnetic wave c is constant because it is determined by the permittivity and permiability of insulator. Frequency $f_{\rm res}$ is determined only by interconnect

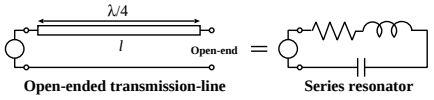

Fig. 5. Open-ended transmission-line and equivalent series resonator.

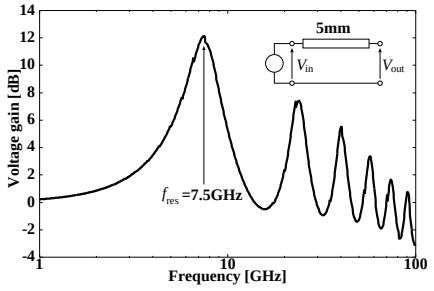

Fig. 6. Transfer characteristics of a transmission-line shown in Figure 1, interconnect length is 5mm.

length. We propose this $f_{\rm res}$ as an extraction frequency and rewrite $f_{\rm res}$ to $f_{\rm proposed}$ in following sections.

C. Limitations of the Proposed Method

We here examine the limitation of the proposed method. The proposed method assumes that the inductance effect of interconnects is significant and interconnects behave as transmission-lines. This assumption at first seems to make a limitation. However when the inductance effects are negligible, RC lump model is enough to model interconnects.

The second assumption is that the resonance frequency is uniquely decidable. For example, the resonance frequency cannot be determined on branched interconnect because of multiple-reflection. But in high-performance interconnects, impedance matching is applied at the branch to avoid multiple-reflection. Additionally on almost global interconnects, repeaters are inserted and the fan-out of driver is 1.

The proposed method is based on open-ended transmission-line resonator. In most CMOS circuits, transmission-lines are terminated by input capacitance of receivers, which is small enough to assume open-ended. However on transmission-lines terminated by resistance or so, the resonance frequency $f_{\rm res}$ is not equal to $c/4l$. In such case, we have to decide resonance frequency by other way.

Therefore these assumptions does not reduce the application area of the proposed method so much. The proposed method is valid for the most of high-performance interconnects.

IV. Experimental Results

This section shows some experimental results. We verify the modeling accuracy of each representative frequency by circuit

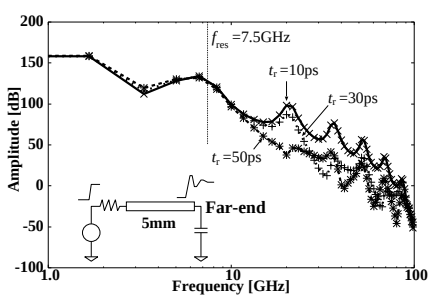

Fig. 7. Frequency spectrum of waveform at the far-end.

TABLE I
RANGE OF PARAMETERS AND REPRESENTATIVE FREQUENCIES.

Parameter range	Corresponding freq. range
10ps $\leq t_{\rm r} \leq$ 100ps	3.4GHz $\leq f_{\rm sig} \leq$ 34GHz
0.5mm $\leq l \leq$ 10mm	3.75GHz $\leq f_{\rm proposed} \leq$ 75GHz

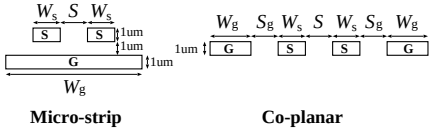

Fig. 8. Cross-sections of interconnects.

simulation. We first explain experimental conditions and some metrics of accuracy. We then verify the accuracy under various experimental conditions.

A. Experimental Conditions and the Metrics of Accuracy

In this section, we explain experimental conditions and metrics of accuracy.

To verify the accuracy of the proposed method comprehensively, we examine under various frequency-dependence and various waveforms. Frequency-dependence of interconnects is determined by the interconnect structures. Waveform variation is expressed by pulse transition time. We therefore vary the following parameters and evaluate the proposed and the conventional representative frequencies.

- pulse transition time ($f_{\rm sig}$ changes).
- interconnect length ($f_{\rm proposed}$ changes).
- interconnect structure and driver strength.

First, the effect of pulse transition time is examined. Transition time decides significant frequency, so $f_{\rm sig}$ varies and $f_{\rm proposed}$ is fixed in this experiment. We then verify the cases that interconnect length changes. Frequency $f_{\rm proposed}$ varies as changing interconnect length, and $f_{\rm proposed}$ is fixed. The ranges of each parameter and the range of corresponding representative frequencies are listed in Table I.

We experiment the above conditions in various interconnect structures and driver output impedance. As the interconnect structure, two popular interconnect structures; micro-strip and co-planar are used. To evaluate crosstalk noise, we locate two signal interconnects. The cross-sections of two interconnect structures are shown in Figure 8. $W_{\rm s}$ is the width of signal interconnect, $W_{\rm g}$ is the width of ground line, S is the spacing between signal interconnects and $S_{\rm g}$ is the spacing between the signal interconnect and the ground line. The frequency-dependence of interconnect characteristics is significant on the thick, wide and long interconnects such as clock lines, bus and global interconnects. For such interconnects, wide interconnects are used to reduce interconnect loss, and the spacing between interconnects are adjusted considering the inductance and capacitive coupling. Therefore we verify interconnect structures in $1\mu{\rm m} \leq W_{\rm s} \leq 8\mu{\rm m}$, $8\mu{\rm m} \leq W_{\rm g} \leq 40\mu{\rm m}$, $2\mu{\rm m} \leq S \leq 8\mu{\rm m}$ and $2\mu{\rm m} \leq S_{\rm g} \leq 8\mu{\rm m}$.

In transient analysis, we evaluate the voltage waveform of the experimental circuit as shown in Figure 9. One of two lines is stimulated by the input pulse, and the other is kept quiet. We call the stimulated line as "Aggressor", and the quiet line as "Victim". The near-end of each line are held by a resistance,

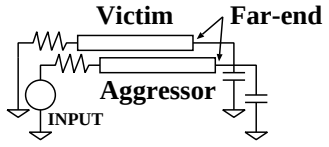

Fig. 9. Experimental circuit for transient analysis.

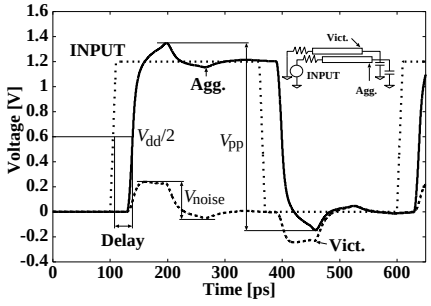

Fig. 10. Definition of delay time, peak-to-peak voltage and crosstalk.

which represents the output impedance of the driver. The characteristic impedance of verified interconnects are within 20Ω–100Ω. The driver output impedance is varied from 10Ω to 100Ω. The far-end of each line is connected to the capacitor load that corresponds to the input capacitance of a receiver. The value of capacitor loads is fixed to 50fF.

To verify modeling accuracies, evaluation metrics are necessary. We use $V_{\rm dd}/2$ propagation delay time (Delay), amplitude of overshoot/undershoot ($V_{\rm pp}$) and amplitude of far-end crosstalk noise ($V_{\rm noise}$) as evaluation metrics. Figure 10 shows the definition of delay time, peak-to-peak voltage and crosstalk. We evaluate these metrics of the ladder extracted at each representative frequencies and frequency-dependent model. We consider the result of the frequency-dependent model as reference data. This means that the evaluation results that are close to those of frequency dependent model are accurate.

B. Transition time vs. Accuracy

We here show the results when transition time is changed. Significant frequency $f_{\rm sig}$ is decided by transition time. When transition time $t_{\rm r}$ is 10ps, $f_{\rm sig}$ is 34GHz and when $t_{\rm r}$ 100ps, $f_{\rm sig}$ becomes 3.4GHz. Figure 11 and Figure 12 show the simulated peak-to-peak voltage and delay time. We use a co-planar interconnect structure with 8μm signal wire width, 20μm ground wire width, 4μm spacing between each interconnects and 5mm length. The output impedance of the drivers is 50Ω. The simulated crosstalk noise voltage is also shown in Figure 13. Table II shows the maximum errors when the transition time varied. From Figure 11, extraction at DC causes about 9% error constantly in the peak-to-peak voltage. The extraction at $f_{\rm sig}$ causes over 10% error when the transition time is small. Significant frequency $f_{\rm sig}$ becomes extremely high when transition time is small. Therefore attenuation on interconnect is overestimated. From Figure 12, the ladder extracted at DC causes about 9% error in the delay time. DC extraction overestimates the inductance value, so the velocity of signal is underestimated. Therefore delay time is overestimated especially when transition time is small. The extraction at $f_{\rm proposed}$ achieves less than 3% errors in the peak-to-peak voltage and the delay time. From Figure 13, there is the same trend as the peak-to-peak voltage in the amplitude of crosstalk noise. DC extrac-

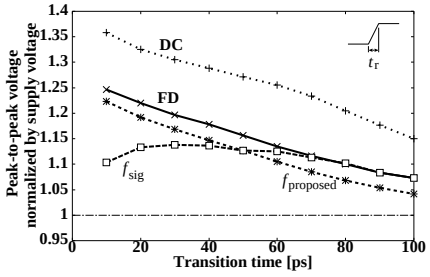

Fig. 11. Voltage peak-to-peak when the transition time is changed.

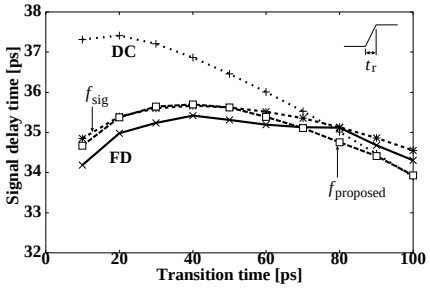

Fig. 12. Delay time when the transition time is changed.

tion causes error constantly and f_{sig} causes remarkable error when the transition time is small. As seen in Table II, DC extraction causes about 10% overestimation in V_{pp}, delay and V_{noise}. Resistance and inductance extraction at f_{sig} causes over 10% underestimation in V_{pp} and V_{noise}. The ladder extracted at $f_{proposed}$ steadily provides the most accurate estimation among the three, and the maximum error is about 8%.

We here show one example of typical waveforms. Figure 14 shows the waveforms at the far-end of the aggressor and the victim interconnects. From Figure 14, the overshoot and crosstalk are overestimated on the ladder extracted at DC, and are underestimated on the ladder extracted at f_{sig}. From viewpoint of the signal delay, we can see that DC overestimates the delay time. From the observation of waveforms, the equivalent circuit extracted at $f_{proposed}$ is the most accurate.

C. Interconnect length vs. Accuracy

Next, the accuracy versus the interconnect length is discussed. Frequency $f_{proposed}$ depends on the interconnect length and the wave velocity. The wave velocity is determined by relative permittivity. Therefore we can assume that the velocity is constant in the same technology. Figure 15 shows the peak-to-peak voltage, and Figure 16 shows the delay time normalized by the delay time of FD model. Figure 17 shows the amplitude of the crosstalk noise. The simulation condition is the same as Section B. As seen in Figure 15, the ladder extracted at

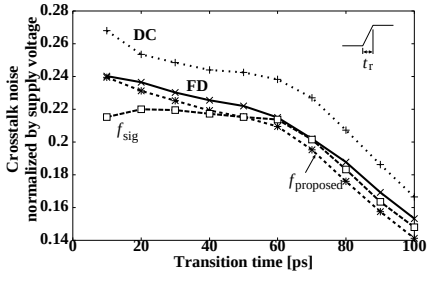

Fig. 13. Crosstalk noise peak-to-peak when the transition time changed.

TABLE II
MAXIMUM ERRORS WHEN THE TRANSITION TIME CHANGED.

Extraction Freq.	DC	$f_{proposed}$	f_{sig}
Error in V_{pp}	$+9.0\%$	-3.0%	-11.5%
Error in Delay	$+9.2\%$	$+1.9\%$	-1.2%
Error in V_{noise}	$+11.8\%$	-7.9%	-10.4%

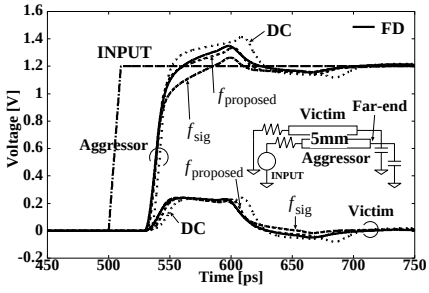

Fig. 14. The waveforms at the far-end of the aggressor and victim.

$f_{proposed}$ achieves the minimum error in peak-to-peak voltage. DC extraction always overestimates the V_{pp}, and f_{sig} extraction causes underestimation when the interconnect length becomes long. As shown in Figure 16, DC extraction causes about 10% error when the interconnect length becomes long. The errors of $f_{proposed}$ and f_{sig} extraction are almost same and below 4%. From Figure 17, crosstalk noise becomes larger as the interconnect length becomes long in the region where the interconnect length is small. The noise amplitude is almost constant when the length is more than 2mm. Figure 17 shows that DC extraction causes overestimation and f_{sig} causes underestimation of the crosstalk noise.

The maximum errors are listed in Table III. As you see, DC and f_{sig} may cause over 10% errors but the maximum error of $f_{proposed}$ is about 3%. These results indicates the ladder extracted at $f_{proposed}$ is robust against the change of the interconnect length.

D. Results of Overall Experiments

In the above sections, we show that the frequency calculated from interconnect length $f_{proposed}$ achieves the most accurate analysis. Table IV shows the maximum errors in all of the results we evaluate. We carefully choose the experimental conditions so that we can cover most part of the realistic cases. The total number of experiments is about 14,000. The ladder extracted DC or f_{sig} causes errors beyond 20%. When a wide micro-strip interconnect is driven by a strong driver, DC and f_{sig} tend to cause large error. The proposed frequency $f_{proposed}$ achieves the error below 8%. The above discussions prove that

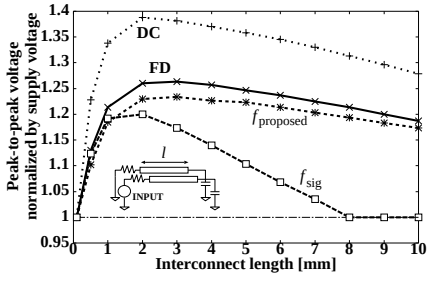

Fig. 15. Voltage peak-to-peak when the interconnect length changed.

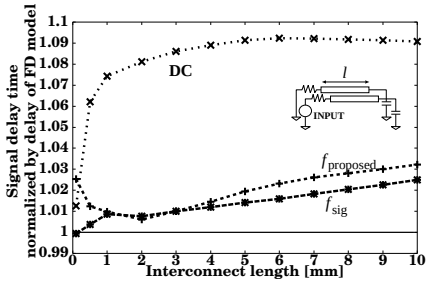

Fig. 16. Normalized delay time when the interconnect length changed.

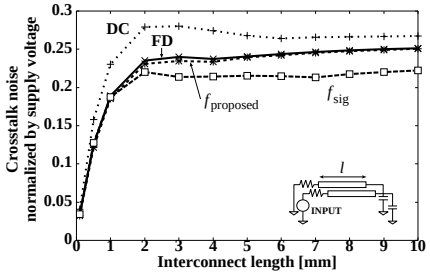

Fig. 17. Crosstalk noise peak-to-peak when the interconnect length changed.

the ladder extracted at the proposed frequency f_{proposed} provides the most accurate modeling of frequency-dependent interconnects among the three frequencies.

E. Tolerance to Extraction Frequency Variation

We here discuss the effect of f_{proposed} estimation error on modeling accuracy. As mentioned in Section C, the proposed method is based on open-ended transmission-line theory. However in real chips, interconnects are terminated by input capacitor of the receiver and, rigidly speaking, the sink is not ideal open-end. The resonance frequency is not equal to f_{proposed} exactly, but the difference is usually quite small because input capacitor of CMOS receiver is small.

Figure 18 shows the extraction frequency versus errors. X-axis is the extraction frequency and Y-axis is the error from frequency-dependent model. The experimental setup is the same as that of Figure 14, 5mm wire length and 10ps transition time. The proposed frequency f_{proposed} is 7.5GHz. As shown in Figure 18, the errors in V_{pp} and in V_{noise} become minimum at the proposed frequency. The error in delay becomes minimum at about 20GHz, but the error is almost constant above 10GHz. From Figure 18, the errors are below 2% in the region of $f_{\text{proposed}} \pm 30\%$. This result indicates that the proposed method is accurate enough even if the proposed frequency has a certain error in comparison with the exact resonance frequency. We can also see that extraction at DC and significant frequency $f_{\text{sig}} = 34$GHz is far from the frequency with the minimum error around f_{proposed}. The errors at DC and significant frequency are above 10% whereas that of the proposed method is below 2%.

TABLE III
MAXIMUM ERRORS WHEN THE INTERCONNECT LENGTH CHANGED.

Extraction Freq.	DC	f_{proposed}	f_{sig}
Error in V_{pp}	$+10.2\%$	-2.4%	-15.7%
Error in Delay	$+9.1\%$	$+3.2\%$	$+2.5\%$
Error in V_{noise}	$+18.7\%$	-1.8%	-11.3%

TABLE IV
MAXIMUM ERRORS IN OVERALL EXPERIMENT.

Extraction Freq.	DC	f_{proposed}	f_{sig}
Error in V_{pp}	$+22.5\%$	-4.6%	-28.0%
Error in Delay	$+27.0\%$	$+4.8\%$	$+23.0\%$
Error in V_{noise}	$+37.4\%$	$+7.9\%$	-18.2%

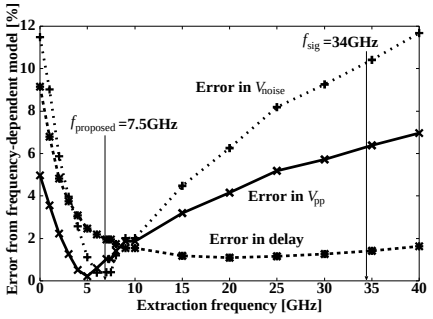

Fig. 18. Extraction frequency vs. errors.

V. CONCLUSION

The frequency that should be used to extract RLC values is discussed. When we use frequency-independent equivalent circuits for circuit design, the extraction frequency must be carefully determined to maximize the fidelity in interconnect characteristics. We propose an RLC extraction scheme that uses the frequency determined by interconnect length. We experimentally verify that the proposed frequency achieves the most accurate estimation in delay time and amplitude of overshoot or undershoot. The maximum error is within 5% in peak-to-peak voltage and delay, and the maximum error in crosstalk is within 8% in our experiments. With the proposed representative frequency, RLC extraction at a single frequency becomes accurate enough to model interconnect characteristics, and hence we can exploit many effective design and analysis techniques developed ignoring frequency-dependence.

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