Design and Optimization of CMOS Current Mode Logic Dividers

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Abstract— We designed and measured a high-speed CML divider in a 0.18μm CMOS process. The fabricated chip operates at up to 10GHz with power consumption of 8.6mW. From a small-signal equivalent circuit model, we derive an analytical performance model that gives the relationship among maximum operation frequency, gate width and load resistance. We also discuss the design optimization based on the derived performance model.

I. Introduction

Recently, over 10Gbps/channel high-speed communication systems with all CMOS transceivers have been reported [1]. In such high-speed circuits, current mode logic (CML) circuits are often used instead of CMOS static logic due to its higher speed and wider noise margin. A CML divider is especially used in various circuits such as PLL, CDR, MUX and DEMUX, and hence its design and optimization method is indispensable for high-performance circuit design.

We design and fabricate a high-speed CML divider in a 0.18μm process. Measurement results show that it operates at 10 GHz. We also discuss design optimization of a CML divider. We observe that unity gain frequency in a small-signal analysis is strongly correlated with the maximum operation frequency, and we reveal that a design optimization for maximizing unity gain frequency improves the maximum operating frequency.

II. CML Divider Architecture

Figure 1 shows a configuration of a CML divider. It consists of two CML D-latches. The circuit topology of a popular CML D-latch is shown Fig.2. A CML D-latch has two blocks: a sense part that transfers input signal to output transparently, and a latch part that outputs the stored logic value. We sometimes use poly as a load resistance because of smaller parasitic capacitance. On the other hand, in this work, we use active resistance by PMOS to realize variable resistance.

When the input clock signal is high, the left D-latch is in sense mode, and the right one is in latch mode (Fig. 1). The inverted output of the right D-latch goes back to the left D-latch input. The input of the left D-latch is transfered to its output. When the input clock signal becomes low, the left one stores the logic state, and the right latch moves in sense mode. The right D-latch outputs the logic value stored in the left D-latch. Thus, the output of D-latch changes by a single clock edge, and hence Fig. 1 works as a 1/2 divider.

III. Design and Measurement Results

We designed and measured a CML divider in a 0.18 μm digital CMOS process. The parameters of the designed CML divider are shown in Fig.2. Figure 3 is the layout of the CML divider. The output buffer, which consists of a differential amplifier and a NMOS common source amplifier, is connected to the output of the CML divider.

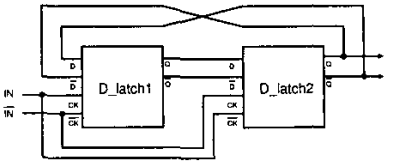

Fig. 1. Configuration of CML Divider

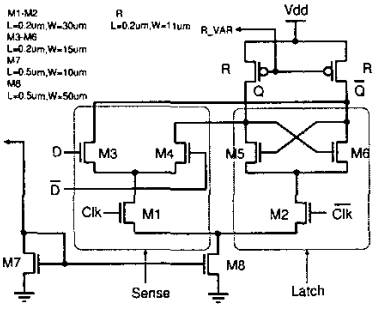

Fig. 2. Circuit Topology of CML D-latch

Fig. 3. Layout of CML Divider (40μm $\times$ 50μm).

The measured output waveform is shown in Fig.4. We give 10 GHz differential sin signals whose single-ended amplitude is 500mV$_{pp}$ as an input clock signal. The tail current, I_{SS}, is set to 1.7mA. Fig.4 (a) shows the output waveform measured by a digital sampling oscilloscope, and (b) is the output spectrum measured by a spectrum analyzer. We confirm that the designed CML divider operates at up to 10 GHz. The measured performance of a CML divider is summarized in TABLE I. The power consumption at 10GHz operation is 8.6mW.

IV. Analytical Performance Optimization

This section discusses a theoretical performance analysis of a CML divider, and describes design optimization using the performance analysis.

We use a small-signal equivalent circuit model to analyze the divider performance. Although the actual clock input is not a small signal and the operating point changes at every

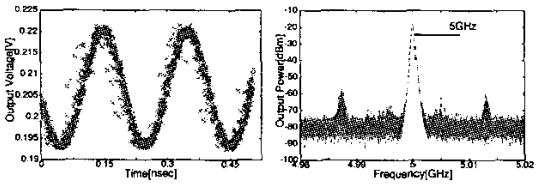

Fig. 4. Output Waveform and Spectrum.

TABLE I
MEASURED PERFORMANCE OF CML DIVIDER AT 10GHZ.

	Performance
Technology	0.18 μm digital CMOS, 1.8V
Max Operation Frequency	10 GHz
Power Dissipation	8.6mW
Core Chip Area	40μm x 50μm

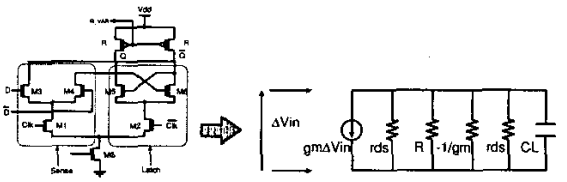

Fig. 5. Small-signal equivalent circuit model.

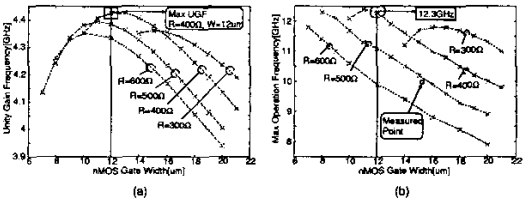

Fig. 6. Unity Gain Frequency and Max Operation Frequency

clock phase, Reference [2] reports that the essence of the divider performance can be captured by a small-signal model. We hence assume in this paper that the input clock amplitude is very small, and all differential NMOSs, M3-M6, are biased by the same current $I_{SS}/4$. In this case, the small-signal equivalent circuit is represented as Fig.5. We can derive the maximum frequency f_{out_max} when the voltage gain becomes unity.

$$f_{out\_max} \leq \frac{\sqrt{{g_m}^2 - \left(\frac{1}{R} + \frac{2}{r_{ds}} - g_m\right)^2}}{2\pi C_L}, \qquad (1)$$

where g_m is the transconductance of M3-M6 biased by $I_{SS}/4$, R is a load resistance, and C_L is the total parasitic capacitance at the output node. In Eq. (1), g_m is a function of NMOS gate width W, and tail current I_{SS}. The load capacitance C_L is also a function of W. Therefore, at each tail current, a CML divider has optimal parameters W, R that make the operation frequency maximum.

Suppose the tail current I_{SS} is 1.7mA. Figure 6 (a) shows the unity gain frequency at various W and R values. Figure 6 (a) indicates that the optimal parameters, $W = 12\mu$m and $R = 400\Omega$, provide the maximum unity gain frequency of 4.43 GHz. We also perform a large-signal analysis by circuit simulation. Figure 6 (b) shows a relationship among the maximum operation frequency, W and R. Similar with unity gain frequency in a small-signal analysis, the maximum operation frequency of a CML divider has an optimal point. The CML divider with $W = 12\mu$m and $R = 400\Omega$, which are the optimal parameters by the small-signal analysis, operates at almost the maximum frequency. Comparing Figs. 6 (a) and (b), we conclude that the unity gain frequency is tightly correlated with the actual maximum operation frequency, although the operation frequency of the CML divider is not completely in agreement with $2 \times f_{out\_max}$. We can obtain the optimal parameters for the maximum operating frequency by maximizing the unity gain frequency.

We show the measured point of the fabricated CML divider in Fig.6 (b). The parameters of the designed CML divider are $W = 15\mu$m, $R = 330\Omega$, and it operates at 10 GHz at most when I_{ss} is 1.7mA. With the analysis of this paper, we can improve the speed of the fabricated CML divider by over 2GHz.

V. CONCLUSION

We design a high-speed CML divider in a 0.18μm process, and discuss design optimization. The fabricated circuit operated at up to 10 GHz. We show that there is a strong correlation between the actual maximum operation frequency and the unity gain frequency in a small-signal equivalent circuit model. With the performance analysis in a small-signal analysis, a CML divider can be optimized by tuning load resistance and gate width under the given tail current.

ACKNOWLEDGEMENT

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