Performance Limitation of On-chip Global Interconnects for High-speed Signaling

Akira Tsuchiya*, Yuuya Gotoh*, Masanori Hashimoto*† and Hidetoshi Onodera*
*Kyoto University, Kyoto 606-8501, JAPAN, †PRESTO, JST.
{tsuchiya, gotoh, hasimoto, onodera}@vlsi.kuee.kyoto-u.ac.jp

Abstract— **This paper discusses performance limitation of on-chip interconnects. On-chip global interconnects are considered to be a bottleneck of high-performance LSIs. To overcome this issue, high-speed signaling and large throughput interconnection using electrical wires are studied. However the limitation of on-chip interconnects has not been studied sufficiently. This paper reveals the maximum performance of on-chip global interconnects based on derived analytic expressions and detailed circuit simulation. We derive trade-off curves among bit rate, interconnect length, and eye opening both for single-end and for differential signaling. The results show that differential signaling improves signaling performance several times compared with conventional single-end signaling, and demonstrate that 80 Gbps differential signaling on 10mm interconnects is promising.**

I. Introduction

According to advances in LSI fabrication technology, operating frequency is increasing. The clock frequency will be over 15GHz at 2010 [1]. A big challenge in this era is high-speed and large capacity signal transmission. Recently to attack this problem, high-speed signaling and throughput driven interconnection are becoming a hot research topic both in design and EDA communities [2]. Optical communication instead of metal wire signaling is also studied [3].

The current signaling scheme is roughly classified into single-end and differential signaling. Differential signaling is used for on-chip high-speed and long-distance interconnection as well as off-chip signaling, for example clock distribution [4]. On the other hand, single-end signaling is very common in chip design. Each scheme has both advantages and disadvantages, and hence circuit designer should be aware of the maximum performance of both signaling schemes, and know in what situation differential signaling is preferable, or rather a sole solution.

The limitation of electric interconnects is discussed in Ref. [5] and it is considered to top out at most 20Gbps. Reference [5] focuses on terminated single-end transmission-lines at various levels such as on-chip, on-board and cables. The conventional on-chip single-end signaling, however, has an open-end termination because of a small input capacitor of a receiver. The discussion on on-chip signaling needs open-ended single-end signaling and differential signaling in addition. Another issue is that the analytic discussion in Ref. [5] is not supported substantially by a detailed analysis considering dispersion and crosstalk.

In this paper, the performance limit of on-chip interconnects is discussed. There are several factors that degrade signal integrity, i.e. attenuation, crosstalk and dispersion. Experimental results show that the main factor that inhibits high-speed signaling is attenuation in crosstalk-controlled interconnect structures. From the viewpoint of attenuation, we analytically derive the maximum eye opening voltage for open-ended single-end signaling, terminated single-end signaling and differential signaling. Experimental results by circuit simulation verify that the analytical performance estimation is valid even when crosstalk noise and frequency-dependence of interconnects are considered. The analytic estimation provides trade-off curves among bit rate, length, eye opening. They indicate the performance difference between single-end and differential signaling and reveal in which region differential signaling has a significant advantage over single-end signaling. We observe that the performance limitation depends on the sensitivity of receiver. The improvement of the receiver sensitivity makes differential signaling achieve tens Gbps signaling on centimeter order length interconnect.

In Section II, we derive expressions for analytical performance estimation. Section III shows some experimental results and discuss performance trade-off curves of signaling. Section IV concludes this paper.

II. Analytical Estimation of Interconnect Performance

This section derives analytic expressions that estimate the performance of on-chip global interconnects. We here focus on attenuation as the most dominant factor that prevents global signaling, and perform an analytical performance estimation based on simplified interconnect and waveform models. The detailed estimation with crosstalk noise, dispersion is demonstrated in the next section.

A. Figure of merit for signaling performance estimation

Eye-diagram is commonly used to evaluate the feasibility and quality, which include bit error rate, of signaling systems [6]. Figure 1 shows an example of eye-diagram. Large eye opening area means that signaling has timing/noise margin. To evaluate the area of eye opening, rectangle/hexagon eye mask is used commonly. However, for simplify in this paper, we use the maximum eye opening in voltage shown in Figure 1 as a figure of merit. In the case of on-chip signaling, attenuation is the most important factor that limits high-speed long-distance signaling. In this condition, the eye opening in time is strongly correlated with that in voltage, and hence we discuss the performance limitation by evaluating the maximum eye opening in voltage.

0-7803-8495-4/04/$20.00 ©2004 IEEE.

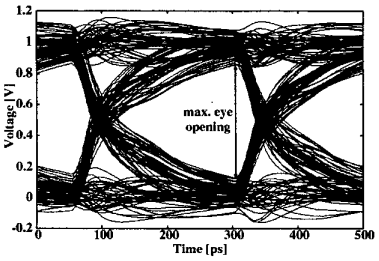

Fig. 1. An example of eye-diagram and the figure of merit.

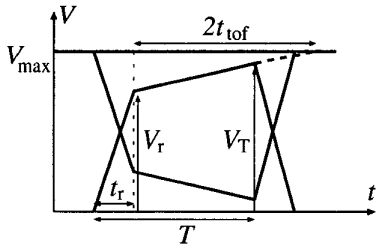

Fig. 2. Piecewise linear waveform model.

B. Analytical performance estimation

We here describe analytical performance expressions that estimate the maximum performance of interconnects.

1) Assumptions on derivation: We here explain three assumptions used for the derivation of the analytic expressions.

The first assumption is that crosstalk noise and frequency-dependence are not significant, since the main cause of eye closing in on-chip signaling is the attenuation. Crosstalk noise affects eye-diagram, however crosstalk noise can be suppressed in a well-designed interconnect structure by shielding and spacing. Interconnect characteristics is frequency dependent because of skin- and proximity-effect and return-current distribution, which causes waveform dispersion. However the effect of waveform dispersion is small compared to that of the attenuation. In the analytical estimation, crosstalk and dispersion are not considered. However, we experimentally verify the adequacy of the analytical estimation by circuit simulations considering crosstalk and dispersion.

The second assumption is impedance-matched driver and termination. For conventional single-end signaling, the near-end is driven by a matched driver and the far-end is open-ended, because the far-end is terminated by a small input capacitor of the receiver. To examine the effect of the termination, the single-end signaling with impedance-matched termination is also evaluated. For differential signaling, the near-end is the same as the single-end signaling. The far-end of the differential pair is terminated by a bridge termination. The bridge termination is commonly used in Low-Voltage-Differential-Signaling (LVDS).

The third assumption is that the waveform at the far-end is expressed as a piecewise linear expression as shown in Figure 2. T is the minimum period of input pulse. t_r is the signal transition time of waveform at far-end, and we assume that t_r is equal to the transition time of input pulse. This assumption is valid when distortion due to frequency-dependence of transmission-line characteristics is weak. V_{max} is the voltage amplitude when the input value is continuously "1". In the case of open-ended transmission-lines, V_{max} is equal to the supply voltage. As for terminated transmission-lines, V_{max} is determined by the resistance of the termination of each end and the DC resistance of the interconnect. At the near-end, the half amplitude of input pulse is injected by the impedance-matched driver. As the injected voltage wave travels on the interconnect, the amplitude decreases by the attenuation. The voltage V_r means the rise voltage at the far-end of the interconnect. On open-ended transmission-lines, V_r is the twice of the amplitude of the arrival voltage wave because of perfect reflection. V_r is determined by the attenuation of the interconnect. On lossy transmission-lines, the voltage continuously rises from V_r [7]. V_T is defined as the voltage after the time T passed since the signal transition started. From a closed-form expression of waveform on lossy transmission-lines, Ref. [8] shows that the voltage at the far-end reaches V_{max} after the time $2t_{tof}$ passed when the interconnect is driven by a matched driver. The time t_{tof} is the signal time of flight and $t_{tof} = l/v$, where l is the interconnect length and v is the velocity of the propagating wave. Therefore V_T is determined from V_r, V_{max} and t_{tof}, which provides simple yet efficient expressions of eye opening shown in the next section.

2) Single-end signaling (Open-ended): We here derive an equation that represents the maximum eye opening. From Figure 2 and the discussion in the previous section, the maximum eye opening voltage V_{eye} is expressed by

$$V_{eye} = \begin{cases} V_{max} - 2(V_{max} - V_T) = 2V_T - V_{max} & (T < 2t_{tof}) \\ V_{max} & (T > 2t_{tof}) \end{cases}. \quad (1)$$

On open-ended transmission-lines, V_{max} is equal to the supply voltage. We set, in this paper, that the supply voltage is 1, without losing generality, because the target circuit is linear. Using the piecewise linear approximation, the first equation of Eq. (1) is rewritable to

$$V_{eye} = 2\left\{\frac{1 - V_r}{2t_{tof}}(T - t_r) + V_r\right\} - 1. \quad (2)$$

We here define the attenuation n as $n = e^{-\alpha l}$ where α is the attenuation constant. By using n, $V_r = n/2 \times 2 = n$, where $n/2$ is the arrival voltage at the far-end and the latter term of 2 corresponds to perfect reflection. The eye opening V_{eye} is expressed by

$$V_{eye} = \begin{cases} \frac{1-n}{l/v}(T - t_r) + 2n - 1 & (T < 2t_{tof}) \\ V_{max} = 1 & (T > 2t_{tof}) \end{cases}. \quad (3)$$

The derived expression indicates that the maximum eye opening V_{eye} is determined by the minimum period T, the rise time t_r, interconnect length l and the attenuation n. The velocity v is determined by the dielectric constant of metal insulator.

3) Single-end signaling (Terminated): The differences between the open-ended case and the terminated case are V_r and V_{max}. V_r is expressed by $n/2$ because there is no reflection at the far-end. On the terminated transmission-lines, V_{max} is

expressed by

$$V_{\max} = \frac{Z_0}{Z_0 + R_{\text{line}} + Z_0}, \tag{4}$$

where Z_0 is the characteristic impedance, which is equal to the driver and termination resistances, and R_{line} is the whole resistance of the interconnect. Here the attenuation n is approximately expressed [7] by

$$n = \exp(-\alpha l) \simeq \exp\left(-\frac{R_{\text{line}}}{2Z_0}\right). \tag{5}$$

Eq. (4) can be rewritten as follows.

$$V_{\max} = \frac{Z_0}{2Z_0 - 2\log n} = \frac{1}{2\,(1 - \log n)}. \tag{6}$$

From the difference of V_{r} and $V_{\max}$, the maximum eye opening is expressed by

$$V_{\text{eye}} = \begin{cases} \frac{\frac{1}{2(1-\log n)} - \frac{n}{2}}{l/v}\,(T - t_{\text{r}}) + n - \frac{1}{2(1-\log n)} & (T < 2t_{\text{tof}}) \\ \frac{1}{2(1-\log n)} & (T > 2t_{\text{tof}}) \end{cases}. \tag{7}$$

4) Differential signaling: In the case of differential signaling, the eye opening V_{eye} is simply the twice of Eq. (7). point of attenuation.

$$V_{\text{eye}} = \begin{cases} \frac{\frac{1}{1-\log n} - n}{l/v}\,(T - t_{\text{r}}) + 2n - \frac{1}{(1-\log n)} & (T < 2t_{\text{tof}}) \\ \frac{1}{1-\log n} & (T > 2t_{\text{tof}}) \end{cases}. \tag{8}$$

III. Experimental results

In this section, we show some experimental results and demonstrate: 1) the validity of the analytic discussion in the previous section, and 2) the performance tradeoffs among signaling scheme, bit rate, interconnect length and attenuation by detailed circuit simulation with crosstalk and dispersion.

A. Simulation setup

We evaluate the eye opening by circuit simulation. First, interconnect R(f)L(f)C are extracted by 2D field-solver, because inductance of a long interconnect such as 10mm is proportional to the length. The shunt conductance is negligible in LSIs because the electric loss of insulator is small. Figure 3 shows the interconnect structure. We assume the 45nm process in Roadmap [1]. In Figure 3, M10 means the tenth metal layer and we assume M11 and M12 are the special thick layer for long distance interconnect or power/ground wire. In M12, there are seven signal line ("S" in Figure 3) and ten ground wires("G" in Figure 3). There are twenty ground wires in M10. The interconnect characteristics is modeled by frequency dependent coupled transmission-line model [9] implemented on circuit simulator [10].

Figure 4 shows the experimental circuit. Each signal wire is excited by an ideal resistance and an ideal voltage source. The input pulses of signal wires are random non-return-zero patterns that are independent of each other. The pulse shape is trapezoidal pulse with pulse period T and transition time $T/10$. In following section, we define "bit rate" by $1/T$. For simplicity, the supply voltage is 1V, because of the linearity of the circuit model. We evaluate the eye opening of each signaling scheme with various pulse period T, interconnect length l, and so on.

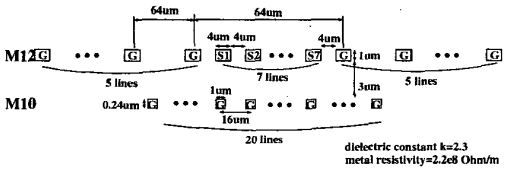

Fig. 3. Cross section of the interconnect.

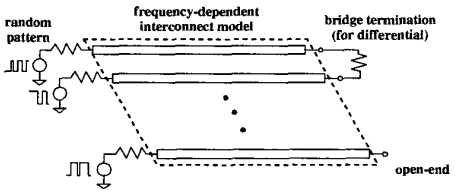

Fig. 4. Experimental circuit.

B. Bit rate vs. eye opening

We here show the bit rate versus the maximum eye opening. Figure 5 shows the analytical estimation and the simulation results. The interconnect structure is Figure 3. To evaluate differential signaling, two signal wires are driven by differential signal and other 5 signal wires are driven by random pattern. These 5 signal wires are noise source. In the case of single-end signaling, S2, S4 and S6 wires are replaced to ground wires, which means that each signal wire has shield wires on both side. In this case, the interconnect resource used by single-end signaling and that used by differential signaling become the same. The far-end of interconnects are open-ended. From Section II, the eye opening of terminated single-end transmission-lines are the half of differential signaling. So we here compare the open-ended single-end signaling and differential signaling. The interconnect length is 10mm and the attenuation of single-end signaling is $n = 0.42$, that of differential is $n = 0.36$. In Figure 3, analytical estimation (labeled "formula") are valid because it is close to the experimental results (labeled "circuit simulation"). Figure 3 shows that in low bit rate region up to 20Gbps, the eye opening of single-end signaling is larger than that of differential signaling. This is because $V_{\max}$ of single-end signaling is large. However as the bit rate becomes higher, the eye opening of single-end decreases very rapidly and becomes almost 0 over 40Gbps. This is because $V_{\max} - V_{\text{r}}$ of single-end becomes larger by attenuation.

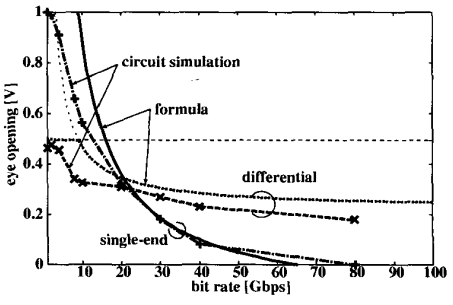

Fig. 5. Bit rate vs. eye opening.

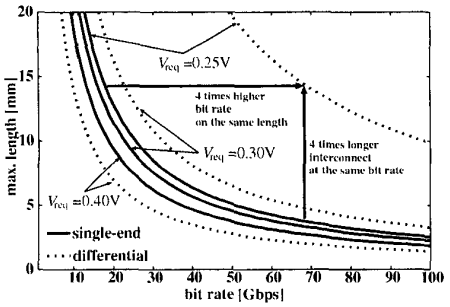

Fig. 6. Bit rate vs. maximum interconnect length with various receiver sensitivity (V_{req}).

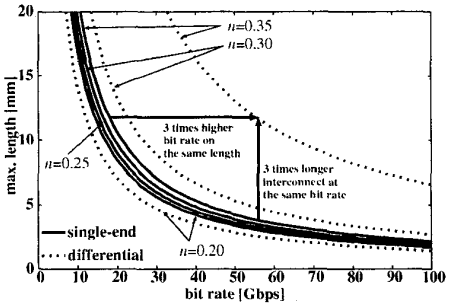

Fig. 7. Bit rate vs. maximum interconnect length with various attenuation. (high n means low attenuation.)

C. Bit rate vs. maximum interconnect length

From the equations derived in Section II, we can obtain the trade-off curve between bit rate and interconnect length. Figure 6 shows the curves of single-end signaling and differential signaling. The condition is the same as that of Section III-B. In Figure 6, V_{req} means the required eye opening V_{eye} for signal comparison. V_{req} depends on the sensitivity and noise margin of the receiver. The trade-off curve of single-end signaling does not change so drastically by V_{req}. On the other hand, the trade-off curve strongly depends on V_{req}. However as V_{req} becomes lower, the advantage of differential signaling become larger. Generally speaking, the comparison ability of differential receiver is higher, and differential signaling does not suffer from the integrity of the reference voltage given to the receiver [6]. If V_{req} is $0.25V_{dd}$, differential signaling can achieve 100Gbps communications on 10mm length interconnect. On the other hand, single-end signaling can perform 25Gbps signaling on 10mm length interconnects and if the bit rate is 100Gbps, interconnect length has to be within 2.5mm.

Figure 7 shows the trade-off curves between length and bit rate with various attenuation n. V_{req} is equal to $0.25V_{dd}$. From Figure 7, the performance of differential signaling depends on the attenuation, and it gets close to single-end signaling as the attenuation becomes large, because V_{max} decreases.

From the above discussion, differential signaling is much superior to single-end signaling when V_{req} is small and n is not too small. Exploiting the better comparison characteristics of the differential receiver, we can receive the benefit of differential signaling.

We here show an example of eye diagram. Figure 8 shows the eye diagram of 80Gbps signaling on 10mm differential

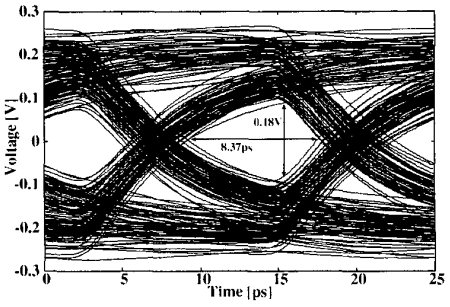

Fig. 8. Eye diagram of 80Gbps signaling on 10mm differential interconnect.

transmission-line. The simulation conditions are the same as those explained in Section III-A. The eye opening is roughly consistent with the analytical estimation and this result shows the validity of the analytical performance estimation.

IV. Conclusion

The performance limitation of on-chip interconnect is discussed. It is important to know the maximum performance and performance trade-off to choose a proper signaling scheme. We first derive analytical expressions for performance estimation. By some assumptions, the maximum eye opening voltage is expressed by attenuation n, interconnect length l and pulse shape. We then verify the analytical estimation by circuit simulation. The analytical estimation is valid even though the estimation does not consider crosstalk and dispersion. The analytical estimation gives trade-off curves of interconnect performance. In a practical situation in interconnect structure and receiver ability, differential signaling can perform 80Gbps communication on 10mm length interconnect. The advantage of differential signaling is significant when the attenuation is not so severe.

Acknowledgement

This work is supported in part by the 21st Century COE Program (Grand No. 14213201).

References

[1] Semiconductor Industry Association, "International Technology Roadmap for Semiconductors", 2003 ed., 2003.
[2] T. Lin and L. T. Pileggi, "Throughput-Driven IC Communication Fabric Synthesis," *Proc. ICCAD*, pp.274–279, 2002.
[3] R. H. Havemann and J. A. Hutchby, "High-Performance Interconnects: An Integration Overview," *Proceedings of the IEEE*, vol.89, no.5, pp.586–601, May 2001.
[4] Ferd E. Anderson, Steve Wells, and Eugene Z. Berta, "The Core Clock System on the Next Generation Itanium Microprocessor," *ISSCC*, pp.146–147, 2002.
[5] D. A. B. Miller and M. H. Özaktas, "Limit to the bit-rate capacity of electrical interconnects from the aspect ratio of the system architecture," *Journal of Parallel Distributed Computing*, vol.41, no.1, pp.42–52, 1997.
[6] William J. Dally and John W. Poulton, "Digital Systems Engineering," Cambridge University Press, 1998.
[7] C.-K. Cheng, J. Lillis, S. Lin, and N. H. Chang, "Interconnect Analysis and Synthesis," A Wiley-Interscience Publication., 2000.
[8] Akira Tsuchiya, Masanori Hashimoto, and Hidetoshi Onodera, "Driver Sizing for High-Performance Interconnects Considering Transmission-Line Effects," *Proc. of SASIMI2001*, pp.377–381, Oct 2001.
[9] Dmitri Borisovich Kuznetsov and José E. Schutt-Ainé, "Optimal Transient Simulation of Transmission Lines," *IEEE Trans. Circuits and Systems*, vol.43, no.2, pp.110–121, Feb 1996.
[10] Avant! Corporation and Avant! subsidiary, "Star-Hspice Manual", 2003.