PAPER *Special Section on VLSI Design and CAD Algorithms*

Si-Substrate Modeling toward Substrate-Aware Interconnect Resistance and Inductance Extraction in SoC Design

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SUMMARY This paper proposes a simple yet sufficient Si-substrate modeling for interconnect resistance and inductance extraction. The proposed modeling expresses Si-substrate as four filaments in a filament-based extractor. Although the number of filaments is small, extracted loop inductances and resistances show accurate frequency dependence resulting from the proximity effect. We experimentally prove the accuracy using FEM (Finite Element Method) based simulations of electromagnetic fields. We also show a method to determine optimal size of the four filaments. The proposed model realizes substrate-aware extraction in SoC design flow.
key words: *substrate, interconnect, resistance, inductance, SoC*

1. Introduction

With advances in LSI fabrication technology, circuit operating frequency is predicted to increase continuously, and local clock frequency will be 15 GHz at 45 nm technology node [1]. Furthermore, even with the current generations of wafer process, recent trends of embedding radio-frequency/mixed-signal blocks in SoC [2] require local oscillator frequencies of over 10 GHz. In such high speed LSIs, on-chip interconnect inductance gives impact on circuit design including timing [3]. At the same time, frequency dependence of interconnect inductance and resistance resulting from the substrate proximity effect should be taken into account [4], [5]. It is because the substrate is usually close to signal wires. The distance is several microns at most even when signal wires are on the topmost layer. When designing a co-planar line for a high-frequency signal, the width and spacing to ground wires are several microns, which is comparable to the distance to the substrate. Thus, the substrate has a distinct impact on resistance and inductance when the frequency is high, though the substrate resistivity is high.

Figure 1 shows circuit simulation examples with and without frequency dependence of interconnect resistance due to the proximity effect on substrate loss. The simulated device under test (DUT) is the micro-strip line discussed in the next section, which is driven by inverters having 260(P-ch) and 130(N-ch) of W/L ratios. Resistivity of the substrate is set to 10 mΩcm. The actual measured RLC values, shown in the next section, are set in the W-element table [6]. The input slew rate t_r is 20 psec./V_{dd}, whose significant frequency $f_s = 0.35/t_r$ [7] is 18 GHz. In this case, the 50% rising time at the far-end of DUT varies by around 30% due to the frequency dependence of the resistance value.

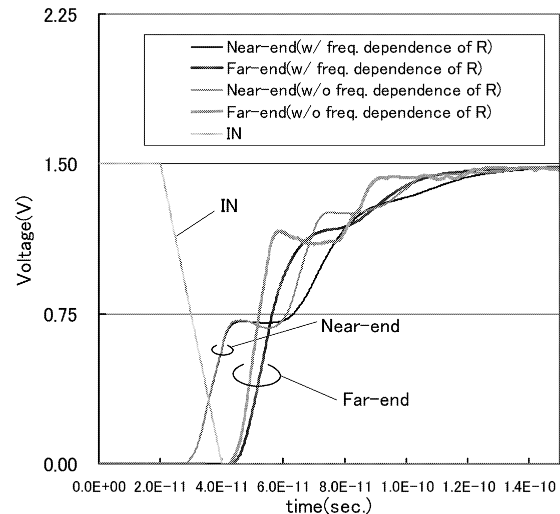

Fig. 1 Influence of substrate loss.

In the SoC design, RF (Radio Frequency) interface IP blocks are often embedded. Designers and/or placement and routing tools have to route interconnects for high-frequency signals. After routing, signal integrity must be verified because unexpected characteristic impedance, attenuation and impedance mismatch may degrade the signal integrity and circuit performance. To evaluate signal integrity, interconnect RLC parameter extraction is necessary. For on-chip interconnects, filament-based extractors [8]–[12] are commonly used because structure modeling can be easily performed with an ascii description, which is suitable for automatic extraction.

However, it is not easy to extract such inductance and resistance. An obstacle is that an efficient substrate modeling for a filament-based extractor is not developed. Extractors [11], [12] provide a multiple filament option, but it is optimized for the skin effect. With the multiple filament option, Si-substrate requires a large number of filaments to

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take the proximity effect into consideration, which prevents filament-based extractors from extracting interconnect inductances and resistances efficiently in computational cost.

To solve this issue, it is necessary to establish a multiple filament modeling which reproduces the proximity effect to the Si-substrate with a small number of filaments. We observe the current concentration in the substrate due to the proximity effect, and propose a Si-substrate modeling with four filaments. The proposed modeling enables substrate-aware interconnect resistance and inductance extraction with a small computational cost using a filament-based extractor.

On the actual LSIs, there are buses running in parallel and densely-routed wires exist. They cause a potential need to extract mutual inductance and simulate the inductive coupling effect as a part of signal integrity verification. However, as a first step, this paper focuses on loop self inductance and resistance extraction.

In this paper, we first survey the actually measured frequency dependence of interconnect resistance and inductance with different substrate resistivities of 100 Ωcm and 10 mΩcm in order to see the proximity effect of substrate. Then, we introduce a new Si-substrate model for filament-based extractors and a method to determine optimal dimension of the filaments. We experimentally prove accuracy of the proposed model, adopting the FEM-based electromagnetic simulation as the reference.

In the SoC interconnect design, designers extract parasitic resistance and inductance of each objective interconnect segment by using a filament-based extraction tool with the proposed substrate model. Guided with the extracted inductance and resistance values, designers proceed circuit design.

2. Measured Frequency-Dependence of Interconnect Resistance and Inductance

In order to observe interconnect characteristics resulting from the properties of Si-substrate, we have designed test element groups (TEG), which have been built in a 130 nm CMOS technology. After specifying the characteristic by measurement, we discuss an effective simulation model for substrate-aware extraction.

Figure 2 shows cross-sectional view of the TEG we studied, where a part of DUT is a micro-strip line (MSL). There are ground (GND) lines for DC return, whose DC resistances are negligibly small. Thus, in all TEGs, the loop DC resistance is almost determined by the resistance of a signal line. The GND lines for DC return are connected to the substrate by via arrays. There is no M1 ground plane even in the MSL configuration. Figure 3 shows each DUT layout pattern, consist of MSL and co-planer lines (CPL). Figures 4–7 show the frequency dependence of the interconnect resistance and inductance, converted from measured S-parameters. The frequency range is up to 20 GHz. Regardless of the substrate resistivities, the micro-strip line has the same characteristic as the co-planer line with a far GND re-

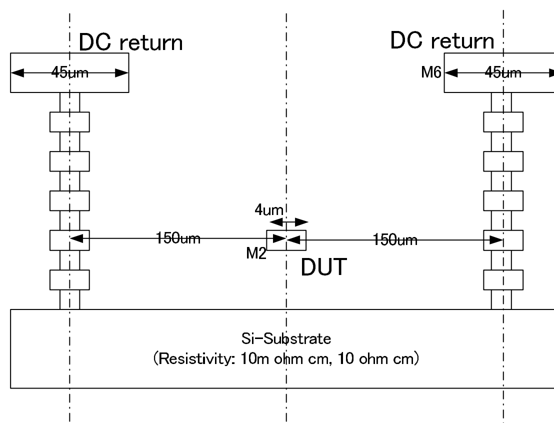


Fig. 2 Cross-sectional view of TEG.

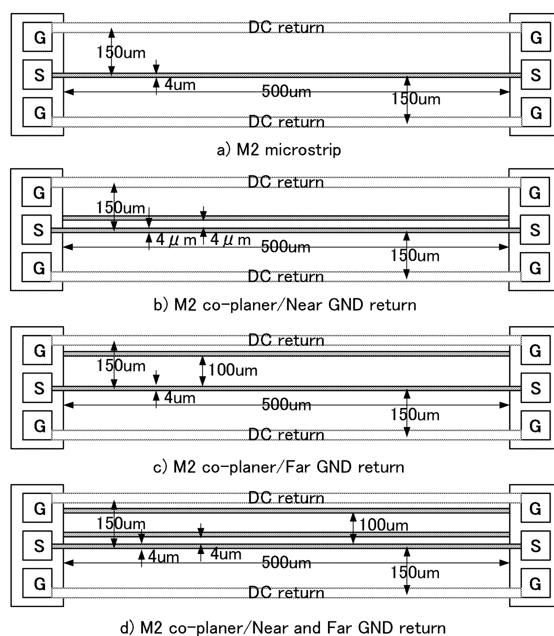


Fig. 3 Layout pattern of DUT.

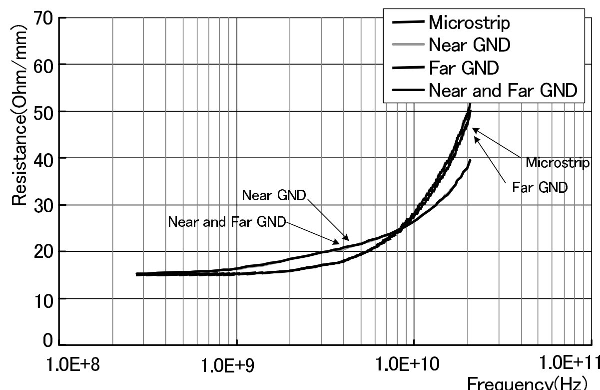


Fig. 4 Measured resistances (10 mΩcm substrate).

turn. Similarly, the co-planer with a near GND return has the same tendency as the co-planer with near and far returns.

The largest difference between the two substrate resistivities is found in the ohmic loss above 5 GHz (Figs. 4 and 6). That is, on the low resistivity substrate of 10 mΩcm, the micro-strip and the co-planer with a far GND return involve large ohmic loss above 5 GHz. It is considered to originate in the proximity effect of the substrate.

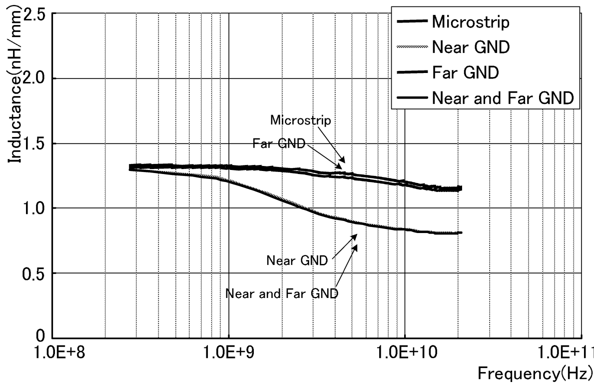


Fig. 5 Measured inductances (10 mΩcm substrate).

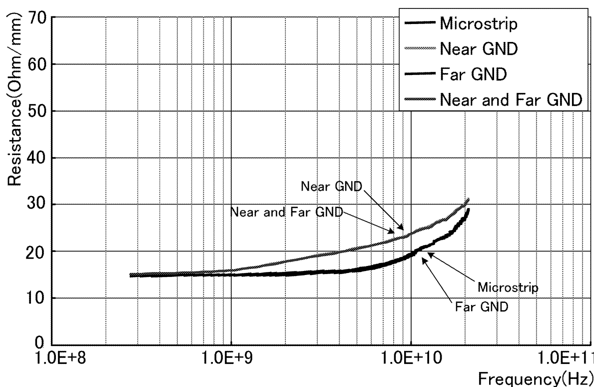


Fig. 6 Measured resistances (10 Ωcm substrate).

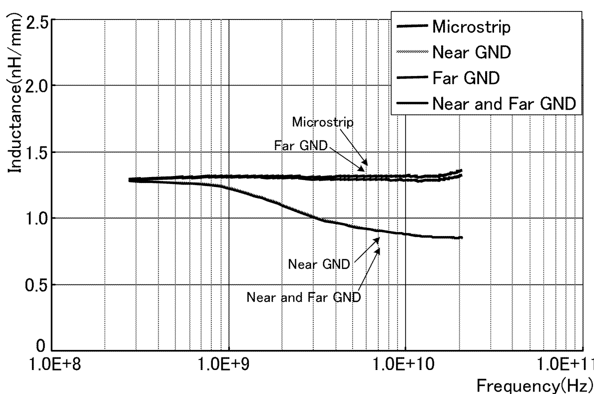


Fig. 7 Measured inductances (10 Ωcm substrate).

3. Si-Substrate Modeling Approach

In this section, we discuss an effective substrate modeling for the partial element equivalent circuit (PEEC) and the loop inductance and resistance extraction [13], [14], which can consider the proximity effect observed in the measurement.

3.1 Problems of the Conventional Modeling

In the PEEC model, a Si-substrate is discretized into filaments [15]. The frequency dependence due to the skin and the proximity effects can be taken into account by forming multiple return paths.

Figure 8 depicts the current flow in the substrate that is modeled as several filaments. The current in metal power/ground wires is omitted to clearly demonstrate current flow in the substrate though the return current flows in metal power/ground wires as well as in the substrate. The current flows to minimize the total impedance. At higher frequency, it crowds through the conductors that are closest together and here the resistance increases but the inductance decreases. At low frequency, it spreads out to minimize the resistance.

If the substrate is not discretized into multiple filaments, the major frequency dependence does not occur. Figure 9 shows that single filament substrate model does not

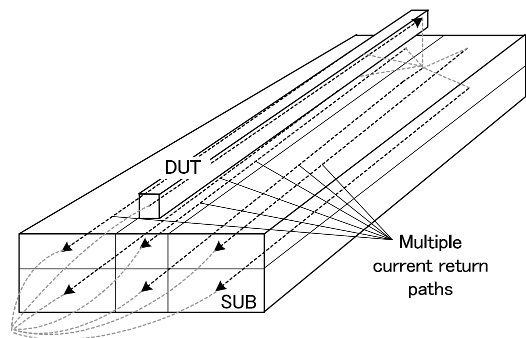


Fig. 8 Current flow in the substrate modeled as multiple filaments.

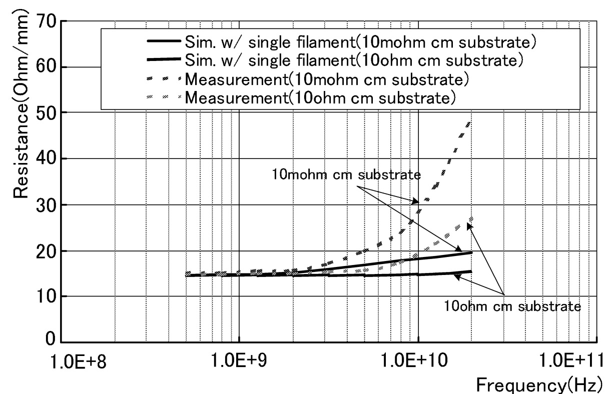


Fig. 9 Resistance of MSL (PEEC w/single filament substrates).

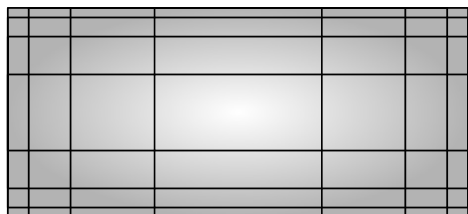


Fig. 10 Multiple filaments optimized to the skin effect.

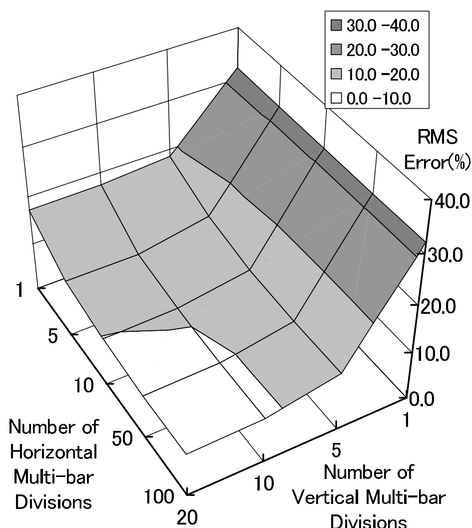


Fig. 11 RMS error of resistance of MSL, extracted using multi-bar function built in Raphael RI3 (10 mΩcm substrate).

reproduce the frequency dependence very well. At 10 GHz, there appears 36% discrepancy from measured resistance as for 10 mΩcm substrate. The resistance increase observed in the simulation results at higher frequency comes from the skin and proximity effect of the signal line, not the substrate. It means that the major factor to the frequency dependences is the proximity effect of the substrate.

A general approach to model the substrate using PEEC is dividing the substrate into many filaments, since the substrate has large volume [10]. A commonly-used discretization method into multiple filaments, which is implemented in the extractors [11], [12] allocates many filaments near the edges as shown in Fig. 10, because it aims to consider skin effect. However, when the discretization method is applied to Si-substrate, it requires many filaments to well reproduce the proximity effect. Figures 11 and 12 show the filament number dependence of resistance and inductance extraction errors concerning MSL put on the 10 mΩcm substrate, using a discretization method called multi-bar implemented in Raphael [11] RI3-mode. More than 10×10 substrate filaments have to be allocated in order to suppress the resistance extraction error within 10%.

Figure 13 shows that several hundreds of filaments take longer CPU time than the several filaments case by over two orders of magnitude. Comparable processing time to the referenced FEM solver means that there is no merit in computational cost to make use of the filament-based extractor. Both filament-based method and FEM solver are prohibitively expensive in computational cost. To efficiently extract interconnect resistance and inductance of a SoC, which includes complicated interconnect structures, processing time needed for filament-based extraction must be minimized by reducing the number of filaments while keeping accuracy.

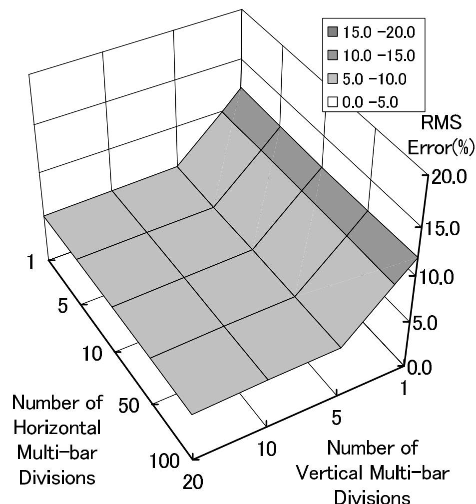


Fig. 12 RMS error of inductance of MSL, extracted using multi-bar function built in Raphael RI3 (10 mΩcm substrate).

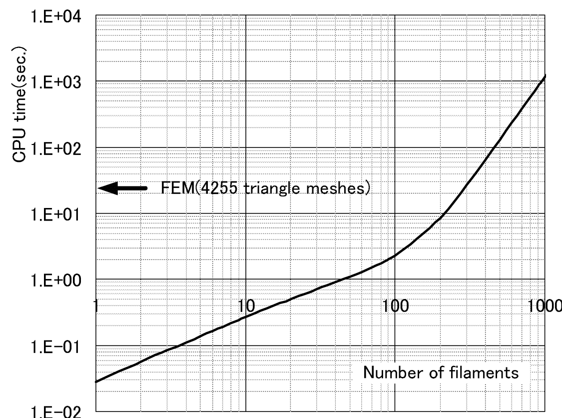
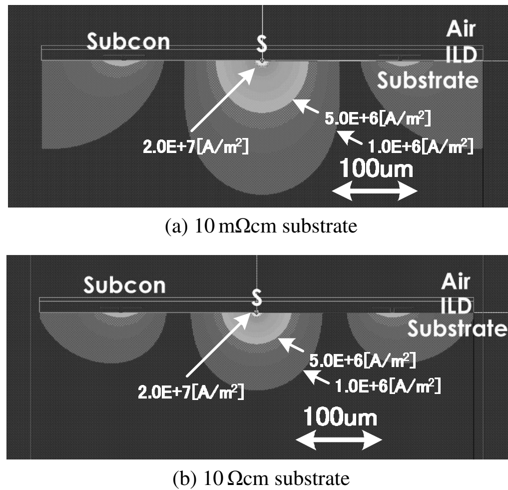


Fig. 13 Relationship between the number of filaments and the processing time.

3.2 Proposed Modeling

In order to derive a multiple-filament model suitable for the proximity effect to the Si-substrate, we observe the current distribution in the substrate. Current flow in the substrate, simulated by FEM, is highly concentrating near the signal at frequencies where resistance and inductance are changing due to the proximity effect (Fig. 14). We can hence expect that much fewer filaments reproduce the frequency dependence of resistance and inductance. We examined several number of substrate filaments as for the most remarkable



(a) 10 mΩcm substrate

(b) 10 Ωcm substrate

Fig. 14 Current distribution in substrate of MSL at 10 GHz, simulated by FEM.

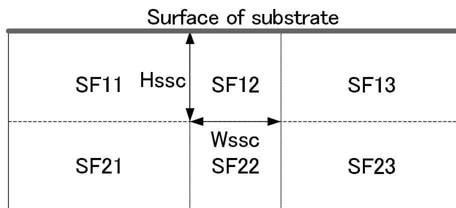


Fig. 15 Cross-section of six filaments substrate.

case, that is the micro-strip line on the 10 mΩcm substrate. We will show the relationship between the number of filaments and the corresponding extraction accuracy in the next section. Each set of substrate filaments is optimized along with the following steps. To simplify the explanations, let us assume six substrate filaments shown in Fig. 15 here.

Step1 Set the size of the top middle filament, consist of $Hssc$ and $Wssc$ of $SF12$ in Fig. 15. The total height of the substrate (e.g. 400 μm) is determined by the fabrication. Here, the total width is set to the distance between the DC return lines, widely enough to match the DC resistance.

Step2 Calculate root-mean-square (RMS) error between resistances and inductances computed by the filament-based extraction and a reference field solver, over the target range of frequencies.

Step3 Change the size of the top middle filament. Calculate RMS as same as Step2.

Step4 Repeat Step3, and adopt a size of the top middle filament, which provides the minimum RMS error.

When there are more than six filaments, the procedure is the same though the number of variables increases.

3.3 Application to SoC Interconnects

On the actual wafers, there are many shapes of interconnects, including bends, branches, and orthogonal interconnects. A general method to treat these interconnects by PEEC is, once extracting interconnect resistance and inductance of each straight transmission-line segment, then connecting them in series (Fig. 5.12 in [3]). Concerning orthogonal interconnects, influences of eddy currents flowing in the crossing lines are not significant [3], even for 4 μm interconnects, which are almost the limits of the width for the current generations of copper interconnect processes [16]. As for the bends and branches, since it may thought that an edge effect is not negligible, we evaluated the edge effect by comparing 3D full-wave FEM simulation [17] results applied to folded lines as shown in Fig. 16. We evaluated MSL and CPL structures. The maximum differences in resistance and inductance between the extracted values from the folded lines and straight transmission lines are 4.2% and 2.7% due to the edge effect, respectively even at 50 GHz. We conclude that the edge effect is not significant. Here, FEM results only for the folded wires are shown. Similar results are obtained for branches with 90-degree bends and orthogonal wires, though they are omitted.

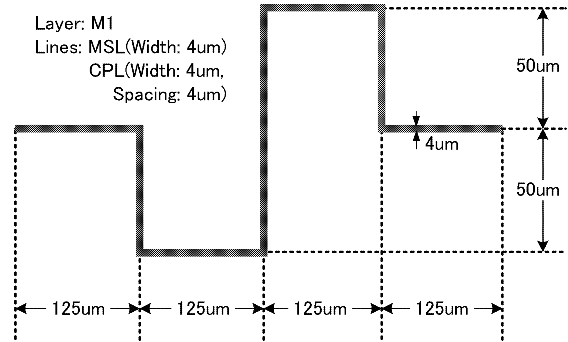


Fig. 16 Folded lines simulated by 3D full-wave FEM.

In the next section, we discuss the detailed experimental results and validness of this flow.

4. Experimental Results

To discuss the correctness of the proposed method with referring to current distribution in the substrate, we use a FEM filed solver, Maxwell [18] as the reference. The conditions for the FEM are, allocating 4255 of triangle meshes for whole conductors and setting the stopping criterion within 1% error. The resistances and inductances simulated by FEM have been correlated with the measured values within RMS errors of 8.3% and 12.9% in the measured frequency range of 50 MHz–20 GHz, respectively. On the other hand, we use Raphael as a filament-based extractor. Partial inductances and resistances are converted to the loop inductances and resistances inside Raphael. Effective resistivity of 10 Ωcm substrate, used for this experiment, is decreased to 200 Ωcm by the amount of P-well ion implantation. When performing the simulation using Maxwell (FEM) and Raphael (PEEC), we consistently use 200 Ωcm as resistivity instead of 10 Ωcm. As shown in Figs. 22–29, which will be discussed later in detail, the characteristics of

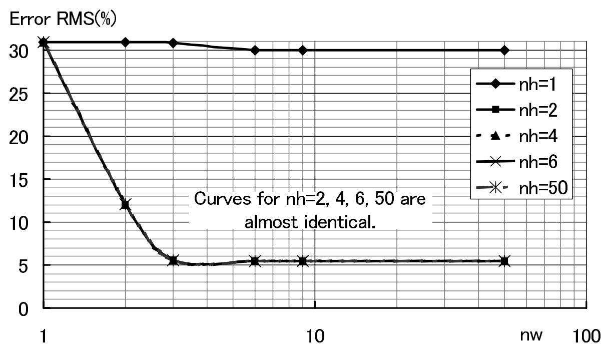


Fig. 17 RMS error of resistance between FEM and PEEC (10 mΩcm substrate).

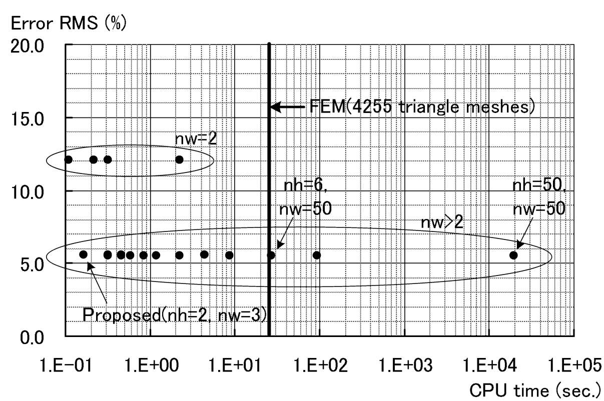


Fig. 18 Relationship between computing time and the RMS error (10 mΩcm substrate).

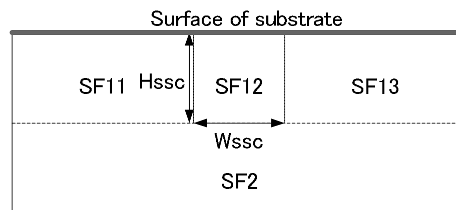


Fig. 19 Cross-section of proposed four-filaments substrate.

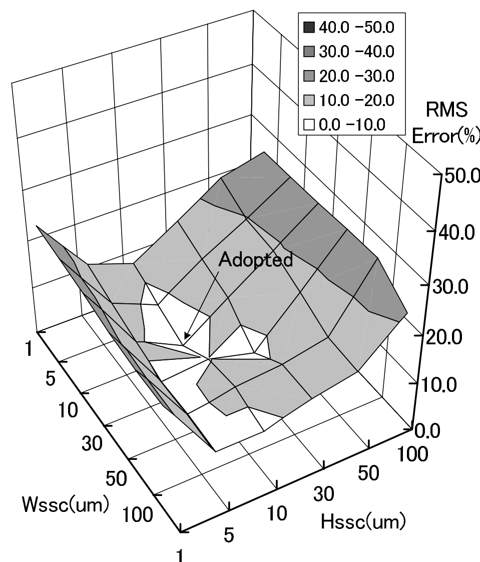


Fig. 20 RMS error of resistance of MSL, extracted using the proposed four-filaments substrate configuration (10 mΩcm substrate).

resistance and inductance simulated by PEEC agree with the corresponding characteristics simulated by FEM. Since the result of CPL with a far GND is very close to that of MSL, we show only the result of MSL in the figures. Similarly, the result of CPL with far and near GND returns is not distinguishable from that of CPL with a near return. We describe only the result of CPL with a near return, as well.

In order to clarify the number of filaments required to consider the substrate effect, we examined several number of substrate filaments for the most remarkable case, that is the micro-strip line on the 10 mΩcm substrate. Figure 17 shows the RMS error of resistance extracted by Raphael with different number of filaments. Sizes of the filaments are optimized by the method discussed in the previous section. *nh* and *nw* in the figure captions stand for the vertical and the horizontal number of the substrate filaments, respectively. Except for the cases of $nh = 1$, the plots approximately trace the same RMS error curve.

Figure 18 shows the relationship between computing time on Enterprise [TM] 450 Server-300 and the corresponding RMS error. In the cases of $nw = 2$, the RMS error becomes 12%, and it is double compared with the other cases that *nw* is larger than 2. In other words, although it is generally thought that the large extraction resources are needed to consider the substrate effects, $nw = 3$, which consuming only less than 1 second of CPU time, reproduces the characteristic. The reason why $nw = 2$ cases do not reproduce the characteristics is that the horizontal distribution of the substrate current can not be expressed by the two horizontal filaments, because the vertical boundary of two filaments corresponds to the center of the signal line.

Taking into account these results, we propose to adopt 3×2 filaments as a general model. Furthermore, we can reduce three downward segments to one segment, without increasing the errors. The reduced filaments are shown in Fig. 19. The three bottom filaments are merged into a single filament. Figures 20 and 21 show $Hssc$ and $Wssc$ dependence of the errors on the 10 mΩcm substrate. Here, MSL shows the most remarkable characteristic of frequency dependence and the largest RMS errors. Therefore, RMS errors of MSL are shown in Figs. 20 and 21 as a representative. We confirmed that the sizes of the four filaments, optimized to the micro-strip DUT, also reproduce the characteristics of the co-planer DUT. The results are shown in Figs. 22–29. The frequency range is set from 50 MHz up to 50 GHz. The values of $Hssc$ and $Wssc$ in Fig. 15 are set to 10 μm and 50 μm for 10 Ωcm substrate, and set to 10 μm and 10 μm for 10 mΩcm substrate, respectively. The remained RMS errors are below 8.5% under all sets of patterns and parameters.

Then, we confirmed robustness of the obtained filament size, changing height and width of the signal line on

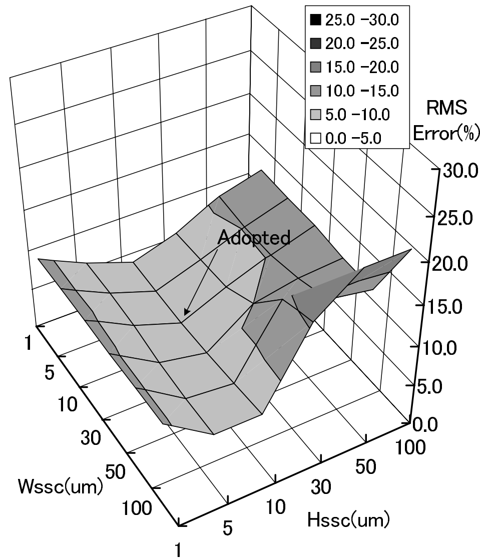


Fig. 21 RMS error of inductance of MSL, extracted using the proposed four-filaments substrate configuration (10 mΩcm substrate).

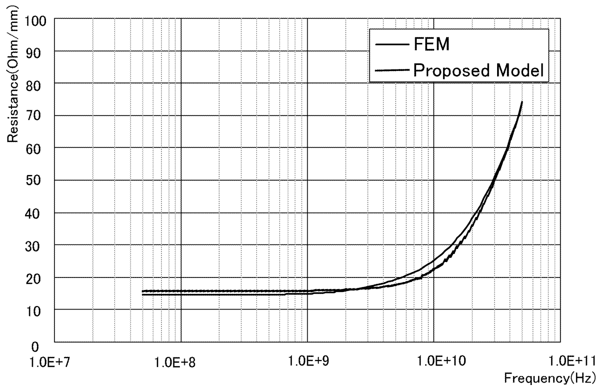


Fig. 22 Resistance of MSL (10 mΩcm substrate, four filaments).

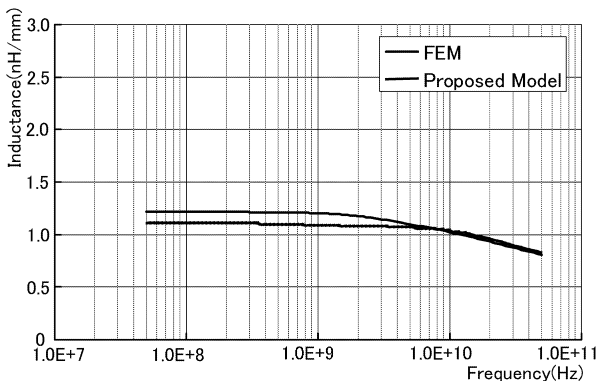


Fig. 23 Inductance of MSL (10 mΩcm substrate, four filaments).

the 10 mΩcm substrate. The sizes of the substrate filaments have been kept throughout this experiment. The results are shown in Table 1. The errors are below 10% if width of the signal line is less than 10 μm, that is the size of $Wssc$ in Fig. 19. In SoC design, the variation and the maximum

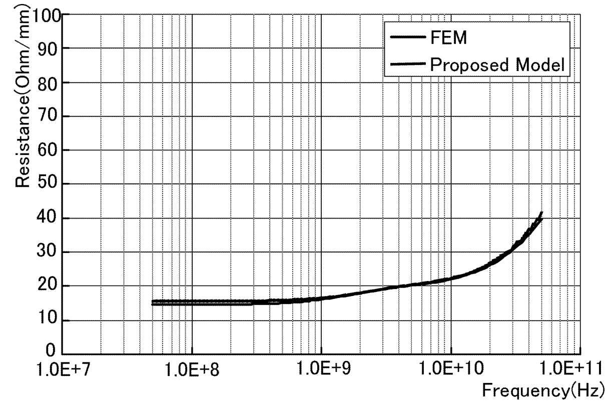


Fig. 24 Resistance of CPL with a near GND return (10 mΩcm substrate, four filaments).

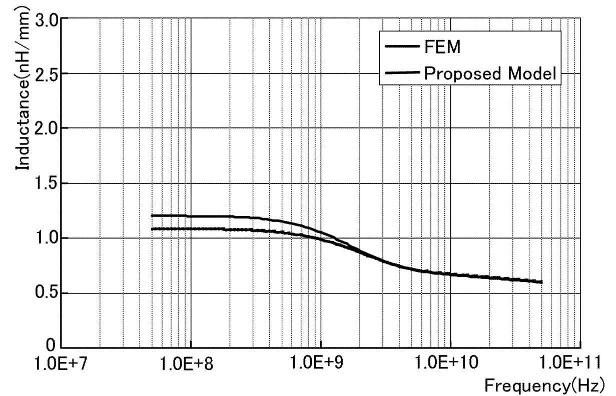


Fig. 25 Inductance of CPL with a near GND return (10 mΩcm substrate, four filaments).

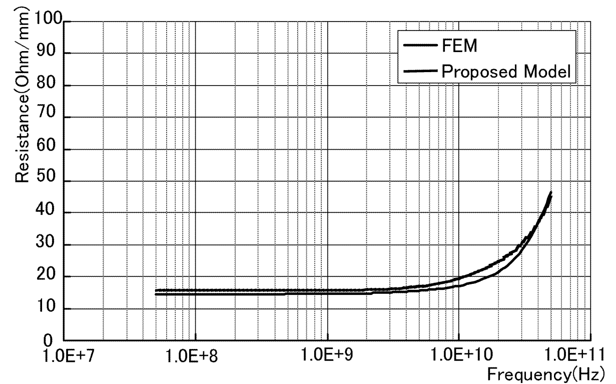


Fig. 26 Resistance of MSL (10 Ωcm substrate, four filaments).

value of interconnect width are limited, and hence the substrate model derived by the proposed procedure is expected to be applicable to most of interconnects.

Further, to see the robustness concerning the locations of DC returns, we checked the errors for varied distance of the DC return lines with keeping the sizes of the substrate filaments. The resulting values are still kept within 9% (Table 2). The derived substrate model is not sensitive to DC return configurations.

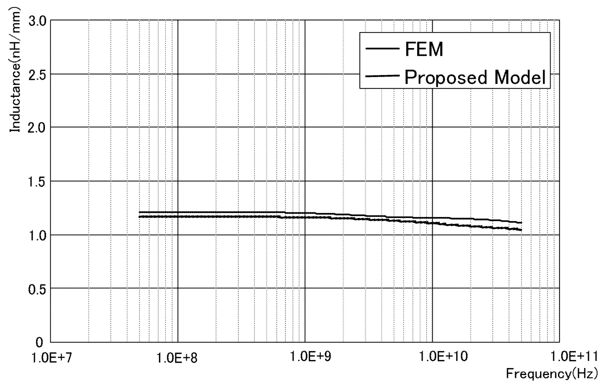


Fig. 27 Inductance of MSL (10 Ωcm substrate, four filaments).

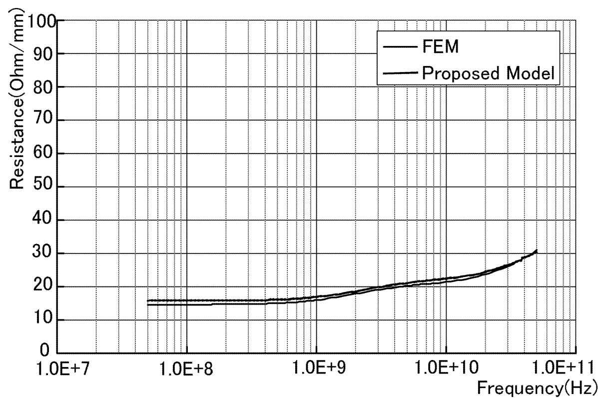


Fig. 28 Resistance of CPL with a near GND return (10 Ωcm substrate, four filaments).

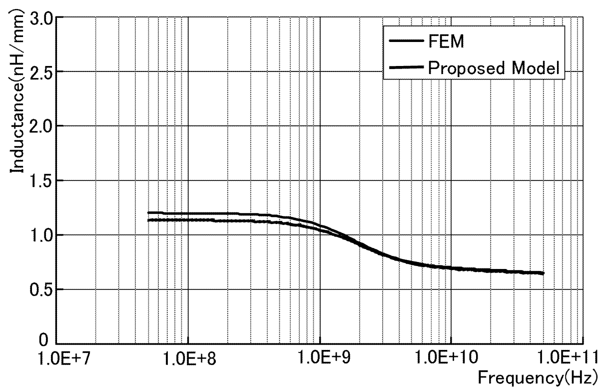


Fig. 29 Inductance of CPL with a near GND return (10 Ωcm substrate, four filaments).

Table 1 Robustness of the proposed model against size and height variations of the signal line.

RMS error (%)		Resistance				Inductance			
		W (μm)				W (μm)			
		2	4	8	16	2	4	8	16
Metal	4	4.7	5.7	8.1	11.4	5.2	5.7	6.4	7.2
Layer	2	4.7	6.1	8.5	11.8	5.4	7.0	6.0	7.2

Table 2 Robustness of the proposed model against spacing variation between the signal and the DC-return lines.

RMS error (%)	Signal to DC-return spacing (μm)			
	50	100	150	200
Resistance	4.8	6.5	6.1	7.3
Inductance	2.8	6.4	7.0	8.9

5. Conclusion

In this paper, we experimentally proved that a small set of PEEC filaments can reproduce the frequency dependence of interconnect resistance and inductance caused by the substrate proximity effect. We also introduced a method to optimize the filaments. One promising application of the proposed modeling is interconnect process characterization for SoC chip-level RLC extraction tools (e.g. [19]), that use filament-based extractors during the characterization. While this paper shows the Si-substrate can be modeled as four or more filaments, the proposed modeling procedure still needs to run the FEM field solver in order to derive the filament size. Establishing a more efficient procedure to determine filament size is one of our future works.

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