TIMING ANALYSIS CONSIDERING SPATIAL POWER/GROUND LEVEL VARIATION

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ABSTRACT

Spatial power/ground level variation causes power/ground level mismatch between driver and receiver, and the mismatch affects gate propagation delay. This paper proposes a timing analysis method based on a concept called "PG level equalization" which is compatible with conventional STA frameworks. We equalize the power/ground levels of driver and receiver. The charging/discharging current variation due to equalization is compensated by replacing output load. We present an implementation method of the proposed concept, and demonstrate that the proposed method works well for multiple-input gates and RC load model.

1. INTRODUCTION

As power/ground noise has been aggravated, power/ground-noise-aware timing analysis is eagerly demanded. This problem can be classified into two issues; how to find the worst-case noise pattern [1], and how to compute propagation delay [2–6]. Conventionally, power-noise-aware timing analysis assumes that ground levels of a driver and its receiver is the same. This is true when the driver and the receiver are placed in the neighborhood. However, if they are placed away, ground level as well as power level becomes different because power/ground noise varies spatially.

Some recent works on propagation delay computation focus on the mismatch problem of power/ground level between driver and receiver [3–6]. One of the difficulties to solve the mismatch problem is large number of parameters that affect propagation delay. The power and ground levels of the driver and the receiver as well as output capacitance and input transition time are parameters. Moreover voltage levels of other stable inputs change propagation delay, and they are also parameters. In the case of a 3-input gate, the number of parameters becomes seven, and it is difficult to construct a gate delay model using look-up tables due to huge characterization cost. References [3–5] propose gate delay models that are derived by first-order expansion using the sensitivity. However, References [3, 4, 6] focus on inverter and buffer, and they do not consider multiple-input gates explicitly. Reference [5] mentions multiple-input gates, but implementation issues are not explained clearly. Also in VDSM technologies, RC load, such as CRC π load model, must be handled to consider interconnect resistance. Reference [3] discusses RC load, but it is not clear whether References [4–6] can cope with RC load in gate-level static timing analysis.

This paper discusses timing analysis that considers temporal and spatial power/ground noise when noise waveforms are given. We experimentally examine the temporal noise on timing. We then propose a concept to solve the mismatch problem due to spatial PG noise. The proposed concept equalizes PG levels of driver and receiver. The charging/discharging current variation caused by the equalization is compensated by adjusting the output load. An implementation method is also presented. Thanks to the proposed concept, we can perform timing analysis with a compact gate delay model. We experimentally verify that the proposed concept works well for various gates, loads and paths.

This paper is organized as follows. We explain the motivation and the target problem of this paper in Section 2. We then propose a concept of "PG level equalization" to capture PG level variation with a compact gate delay model. An implementation method is also described in Section 3. Section 4 demonstrates experimental results of path delay calculation. Section 5 concludes the discussion.

2. MOTIVATION AND TARGET PROBLEM

This section describes the motivation of this work, and clarifies the target problem of this paper.

2.1. Problem of Temporal and Spatial Power/Ground Noise on Timing

There are two obstacles to perform power/ground noise aware timing analysis when noise waveforms are given; temporal variation and spatial variation of PG noise. We here demonstrate both problems, and we explain our goal of this paper.

We first discuss temporal variation of PG noise. PG noise has various amplitude, shape and time constant. When time constant of noise shape is much larger than the transition time of a logic gate, the power/ground level can be regarded as constant. On the other hand, when the noise

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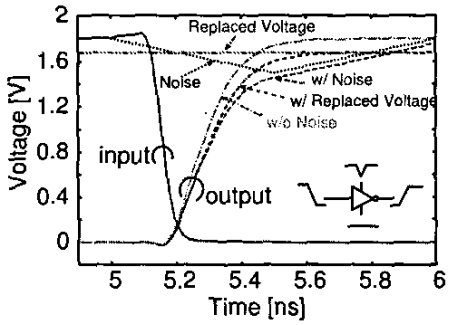

Figure 1: Delay variation by power noise.

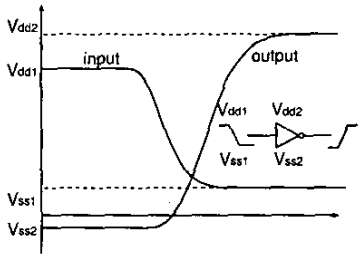

Figure 2: Input and output waveforms with spatial PG level variation.

time constant is comparable with gate transition speed, gate delay calculation becomes complicated and rigid analysis for numerous noise shapes is difficult due to computational cost. Figure 1 shows an example. In this paper, we assume a 0.18μm CMOS process in the experiments. The time constant of power noise is comparable with the gate transition time. The output waveform that is affected by the power noise is much different from the noiseless output waveform. The delay time is increased by 15%.

One possible solution of this problem is replacing temporally-variant noise waveform with a constant voltage level. Our extensive experiments reveal that this replacement works in various conditions. The replaced voltage is calculated as the integral average voltage during the output transition or the output voltage when the output transition starts. Figure 1 also shows the waveform that is calculated by the replaced voltage, and it is close to the actual output waveform. We will not discuss it further since it is not the main topic of this paper, but we think that temporally-variant noise waveform can be replaced with a constant supply voltage.

The second problem is spatial PG variation, and it is the main topic of this paper. Gates in a path are not necessarily placed in the neighborhood, for example, repeaters are necessarily placed with a certain distance. Therefore in a general condition, the PG level of each gate is different. Figure 2 shows an example of input and output waveforms. The maximum and minimum voltage levels of input waveform ($V_{\rm dd1}$, $V_{\rm ss1}$) are the PG levels of the driver gate, and they are different from the PG levels of the receiver gate ($V_{\rm dd2}$, $V_{\rm ss2}$). The charging/discharging current strongly depends on the input voltage level, which results in gate delay variation. Also except inverter and buffer, there are multiple inputs. In this situation, gate delay $t_{\rm d}$ and output transition time $t_{\rm ro}$ are expressed as follows.

$$t_{\rm d} = f_1(t_{\rm ri}, C_{\rm o}, V_{\rm dd1}, V_{\rm ss1}, V_{\rm dd2}, V_{\rm ss2}, V_{\rm in1}, .., V_{\rm in(n-1)}),$$

$$t_{\rm ro} = g_1(t_{\rm ri}, C_{\rm o}, V_{\rm dd1}, V_{\rm ss1}, V_{\rm dd2}, V_{\rm ss2}, V_{\rm in1}, .., V_{\rm in(n-1)}),$$

where $t_{\rm ri}$ is the input transition time, n is the number of inputs, and V_{ink} is the k-th stable input. We can fix one of the voltage levels without losing generality. When we set $V_{\rm ss2}$ to zero, the equations are rewritten as follows.

$$t_{\rm d} = f_2(t_{\rm ri}, C_{\rm o}, V_{\rm dd1}, V_{\rm ss1}, V_{\rm dd2}, V_{\rm in1}, .., V_{\rm in(n-1)}), \quad (1)$$

$$t_{\rm ro} = g_2(t_{\rm ri}, C_{\rm o}, V_{\rm dd1}, V_{\rm ss1}, V_{\rm dd2}, V_{\rm in1}, .., V_{\rm in(n-1)}). \quad (2)$$

When the functions of f_2 and g_2 of a 3-input gate are expressed by a lookup table model, we have to generate seven dimensional tables and the characterization cost by circuit simulation is prohibitively large.

2.2. Target Problem

This paper focuses on spatial PG level variation. We propose a gate delay calculation method using a compact gate delay model that has just three parameters: output loading, input transition time and supply voltage. Our approach is compatible with the conventional static timing analysis, and the characterization cost does not increase drastically. We assume that the PG voltage levels of each gate are given throughout this paper.

3. GATE DELAY CALCULATION CONSIDERING SPATIAL P/G LEVEL VARIATION

This section presents a concept to cope with spatial PG level variation. We then show an implementation method of the proposed concept.

3.1. Proposed Concept of "PG Level Equalization"

The PG level variation changes charging/discharging current, which results in gate delay variation. Basically, gate delay is the time required to charge/discharge output load. Therefore, even if the current increases/decreases by PG level variation, we can keep the gate delay unchanged by increasing/decreasing the output load in the same ratio.

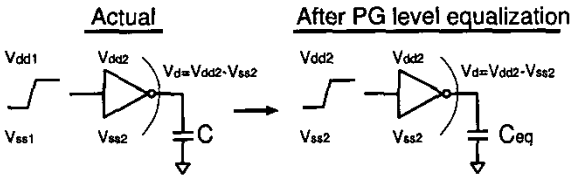

Figure 3: Proposed concept called "PG level equalization".

Figure 3 shows the proposed concept. We set the PG levels of the input waveform to V_{dd2} and V_{ss2}. The equalization of the PG levels is compensated by the adjustment of the output load C. We calculate the equivalent output load C_{eq}, and replace $C_{\rm actual}$ with C_{eq}. The gate delay becomes unchanged when the following relation is satisfied.

$$I_{\rm actual} : I_{\rm eq} = C_{\rm actual} : C_{\rm eq}, \tag{3}$$

where $I_{\rm actual}$ is the actual charging/discharging current, and $I_{\rm eq}$ is the charging/discharging current after PG level equalization. Then $C_{\rm eq}$ is expressed by

$$C_{\rm eq} = \frac{I_{\rm eq}}{I_{\rm actual}} \cdot C_{\rm actual}. \tag{4}$$

Thanks to PG level equalization, the gate delay and transition time calculation is simplified as follows.

$$t_{\rm d} = f_3(t_{\rm ri}, C_{\rm o}, V_{\rm d}), \tag{5}$$

$$t_{\rm ro} = g_3(t_{\rm ri}, C_{\rm o}, V_{\rm d}). \tag{6}$$

where $V_{\rm d}(= V_{\rm dd2} - V_{\rm ss2})$ is the receiver supply voltage.

There are several proposals for gate delay calculation in Eqs. (5) (6). For example, Ref. [2] proposes an interpolation method in voltage using usual two dimensional tables. A vendor proposes a scalable polynomial delay model that includes supply voltage and temperature as well as output load and input transition time as variables. We here think that the formulation of gate delay in Eqs. (5) (6) is acceptable in LSI design.

The proposed concept of "PG level equalization" is quite simple and the necessity is the calculation of Eq. (4) only. The other part of timing analysis is basically the same with the conventional method, and thus the proposed method is compatible with the conventional STA framework. If we have STA tools that can handle Eqs. (5) (6), we can perform static timing analysis considering spatial PG level equalization just with the pre-processing of Eq. (4). We think that the gate delay model of Eqs. (5) (6) is or will be popular, and the proposed concept can co-work with current and future STA tools.

Figure 4 shows input and output waveforms with and without PG level equalization. The PG levels of the actual input waveform are different, and we equalize the PG levels of the input waveform to those of the receiver. PG level

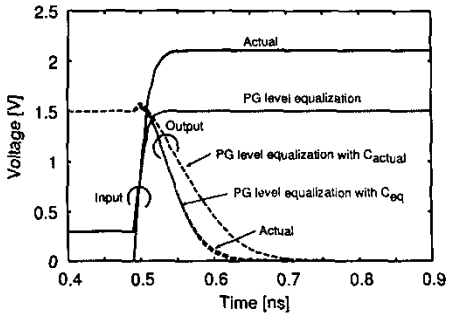

Figure 4: Input and output waveforms with PG level equalization.

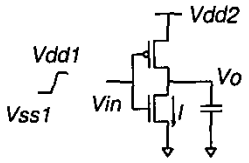

Figure 5: Current flow.

equalization without replacing output load $C_{\rm actual}$ gives the waveform that is far from the actual waveform, because the discharging current becomes different by PG level equalization. We then replace $C_{\rm actual}$ with $C_{\rm eq}$. $I_{\rm actual}$ is calculated by DC analysis in the case that $V_{\rm in} = V_{\rm dd1}$ and $V_{\rm o} = V_{\rm dd2}$ in Figure 5. $I_{\rm eq}$ is calculated in the case that $V_{\rm in} = V_{\rm o} = V_{\rm dd2}$. Thanks to the replacement of output loading, the output waveform with PG level equalization gets close to the actual output waveform. We can see that the basic idea of PG level equalization works well. Hereafter we explain practical implementation issues of the proposed concept.

3.2. Delay and Transition Time Definition

We here explain the definitions of delay and transition times. The definitions are important to calculate path delay, because inconsistent definitions degrade accuracy or rather disable timing propagation. Figure 6 explains the definitions in this paper. Delay $t_{\rm d}$ is the time interval between the input crossing timing of $(V_{\rm dd1} + V_{\rm ss1})/2$ and the output crossing timing of $(V_{\rm dd2} + V_{\rm ss2})/2$. This definition is efficient, because the arrival time when the input goes across $(V_{\rm dd1} + V_{\rm ss1})/2$ is calculated before.

In this paper, we use a waveform expression composed of a linear (0-60%) and an exponential functions (60%-) with a single parameter of T_{12} [9], because ramp waveforms are not suitable for accurate analysis [11]. The parameter of T_{12} is originally defined as the crossing time difference be-

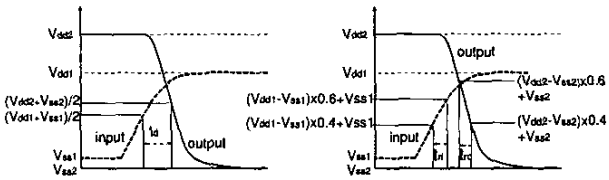

Figure 6: Definitions of delay and transition time.

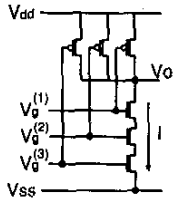

Figure 7: 3-input NAND gate.

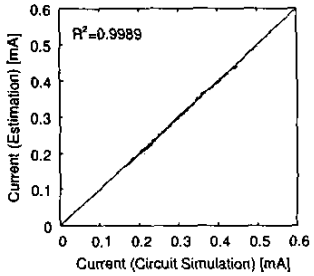

Figure 8: Current estimation accuracy (3-input NAND).

tween $0.4V_{\rm dd}$ and $0.6V_{\rm dd}$. The transition times $t_{\rm ri}$ and $t_{\rm ro}$ are calculated at the crossing timings of 40% and 60% of each voltage swing as shown in the right figure (Fig. 6). Please note that the proposed concept is independent of the definitions described here, although some modifications in implementation may be necessary.

3.3. Current Calculation

The key of the proposed concept is the calculation of Eq. (4), and there are two problems; (1) how we should efficiently calculate current $I_{\rm actual}$ and $I_{\rm eq}$ even for multiple-input gates, and (2) of what timing we should calculate current $I_{\rm actual}$ and $I_{\rm eq}$ in the case that the input transition is slower than the output transition. Solutions of these two problems enable us to perform timing analysis considering spatial PG level variation. This section discusses the first problem, and the second one will be discussed in the next section.

The simplest way to calculate the current in Eq. (4) is to use analytic expressions proposed so far, for example, alpha-power model [7] and equivalent inverter transformation [8]. Alpha-power model [7] is very effective for inverter, but it does not cope with other gates directly, eg. NAND and NOR. Reference [8] proposes a method to replace series-connected MOSFETs with an equivalent MOSFET. This method assumes that the transition swing is between $V_{\rm DD}$ and $V_{\rm SS}$, and other stable inputs are $V_{\rm DD}$ or $V_{\rm SS}$. However in order to capture spatial PG level fluctuation, we need a current model that has all input voltage levels and its supply voltage levels as variables. The extension of Reference [8] is not straightforward, and we hence adopt response surface method [10] as an alternative. We can use other methods if their accuracy is sufficient.

Figure 7 shows the structure of a 3-input NAND gate. Let us examine a fall transition case that the series-connected NMOSFETs discharge the output load as an example. The current I that flows through the series-connected NMOSFETs depends on four parameters, $V_g^{(1)}, V_g^{(2)}, V_g^{(3)}$ and V_o, when we fix the voltage of $V_{\rm SS}$ as a reference level. The response surface method is performed as follows. We first execute DC analysis varying $V_g^{(1)}, V_g^{(2)}, V_g^{(3)}$ and V_o. We next construct a response surface function, where the order of the polynomial function is decided such that necessary and sufficient accuracy can be obtained.

Figure 8 shows the accuracy of the current estimation by the derived response surface function. In this case, we vary V_o from 1.5 to 2.1 V and $V_g^{(1-3)}$ from 1.2 to 2.0 V. The order of the polynomial response surface function is three. The current I is accurately estimated with $R^2 = 0.9989$. The response surface method is a generic method, and we can apply it to various logic gates. The accuracy can be controlled by the order of polynomials.

Figure 9 shows the error when we perform PG level equalization without the replacement of the output load. We vary $V_{\rm dd}$ and $V_g^{(2-3)}$ from 1.6 to 2.0V. We use rise input waveforms whose minimum level is -0.2 to 0.2 V and whose maximum level is 1.6 to 2.0 V. The actual output load is varied from 10 to 100fF, and the input transition time is 30ps. The maximum error is 78 ps. On the other hand, Figure 10 with the replacement of Eq. (4) indicates more accurate estimation results. The maximum error is reduced to 14ps. The delay variation due to PG level fluctuation is well captured by the proposed concept. We confirm that other transition direction and other type of gates, such as INV, NOR, AOI and OAI, can be treated similarly, and we verify the accuracy.

3.4. Slope Consideration

We will explain the second problem using an example of an inverter. In the experimental results shown in the previous section, the transition time of the input waveform is small compared with the output transition time, and the condition for calculating $I_{\rm actual}$ and $I_{\rm eq}$ is easily decided, that is, we just consider the behavior after the input transition finishes.

Let us examine another case that the transition time of the input waveform is larger than the output transition time. Figure 11 shows an example. We give a rise transition to an

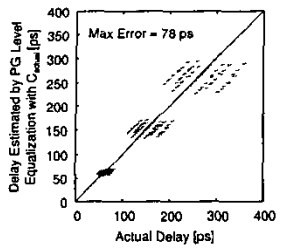

Figure 9: Delay estimation accuracy of PG level equalization without Eq. (4). (3-input NAND, fall transition).

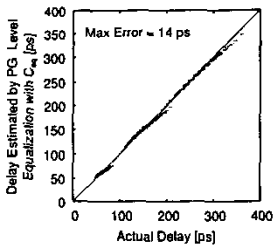

Figure 10: Delay estimation accuracy of PG level equalization with Eq. (4). (3-input NAND, fall transition).

inverter.

We equalize the input and output voltage levels, and generate the input waveform labeled "PG level equalization". In this process, we keep the following relation: $(V_{dd1} - V_{ss1})/T_{12actual} = (V_{dd2} - V_{ss2})/T_{12eq}$. This means that the slope is the same. We align the actual and the equalized waveform in time axis such that the linear parts of both the waveforms match as shown in Figure 11. Figure 11 shows three output waveforms; the actual waveform and the waveforms calculated by PG level equalization with and without the replacement of the output loading. In this figure, the replacement assumes that the input transition is very fast, i.e. the current calculation in Eq. (4) uses V_{dd1} and V_{dd2} as the input voltage levels. We can see that the replacement of the output loading fails. This is because the output transition almost finishes before the input voltage gets close to V_{dd1} (V_{dd2}). The input voltage level that dominantly determines the output transition behavior is not V_{dd1} (V_{dd2}).

We intuitively think that the input voltage while the output is changing, especially before the output becomes $(V_{dd2} + V_{ss2})/2$, has a strong impact on the output behavior. We then choose a timing when the output crosses a voltage level V_{ref}, and use the currents at that timing as I_{actual} and I_{eq} in Eq. (4). In order to determine V_{ref}, we execute numerous experiments varying V_{ref} from $(V_{dd2} - V_{ss2}) \times 0.1 + V_{ss2}$ to $(V_{dd2} - V_{ss2}) \times 0.9 + V_{ss2}$ as well as the voltage level conditions and output load. We observe that the maximum error becomes the smallest when we set $V_{ref} = (V_{dd2} + V_{ss2})/2$. Another issue is how to calculate the output waveform to decide the crossing timing of V_{ref}. From experimental results, we decide to use the output waveform estimated by PG level equalization with C_{actual}, because we experimentally observe that even if the accurate output waveform would be obtained, the accuracy is almost the same. Figure 12 shows the output waveform calculated by the proposed concept with $V_{ref} = (V_{dd2} + V_{ss2})/2$. We

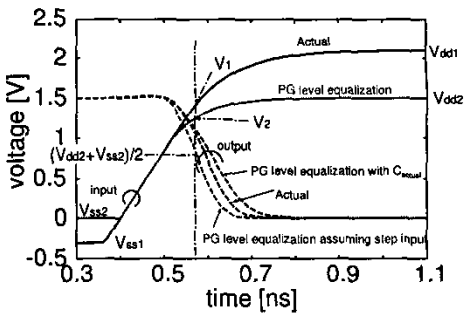

Figure 11: Problem on long input transition time.

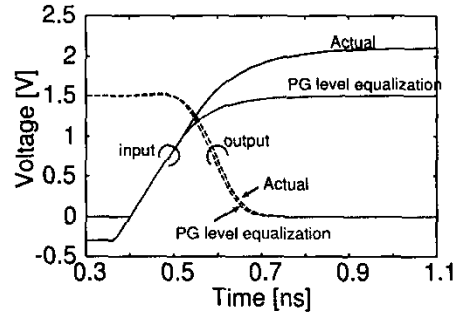

Figure 12: Input and output waveforms by PG level equalization with slope consideration.

can see that the output waveform derived by PG level equalization gets close to the actual output waveform.

We evaluate the accuracy in various conditions. We vary V_{dd2} from 1.6 to 2.0V. We apply rise transitions whose minimum level is -0.2 to 0.2 V and whose maximum level is 1.6 to 2.0 V. The actual output loading is varied from 10 to 100fF, and T_{12} of the input transition is 5ps to 200ps, which roughly corresponds to 30 to 1200ps in 0-100% transition time. Figure 13 shows the error when assuming step input, and Figure 14 indicates the accuracy when the slope of the input waveform is considered. Thanks to the consideration of the input slope, the maximum error is reduced from 78ps to 13ps.

3.5. Generic Output Load

In VDSM technologies, wire resistance affects propagation delay. The output load is once translated into a CRC π model [12], and the CRC π model is replaced with an effective capacitance [13] to obtain the gate output waveform.

We here show that the proposed concept can be applied consistently to generic output loading. Figure 15 shows the proposed concept for generic output loading, where Y_{actual} is the driving point admittance of the actual circuit, and Y_{eq}

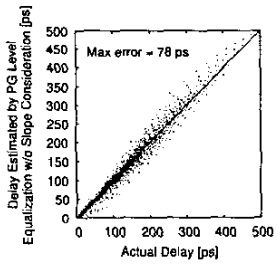

Figure 13: Delay estimation accuracy of PG level equalization w/o slope consideration (INV, fall transition).

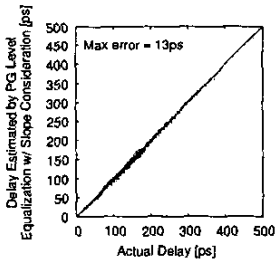

Figure 14: Delay estimation accuracy of PG level equalization w/ slope consideration. (INV, fall transition).

Figure 15: PG level equalization for generic load.

is the driving point admittance after PG level equalization. Similar to Section 3.1, Y_{eq} is calculated by

$$Y_{eq} = \frac{I_{eq}}{I_{actual}} \cdot Y_{actual}. \quad (7)$$

We can see that Eq. (4) is one of the special cases of Eq. (7). In the case of CRC π model, C_{1eq}, C_{2eq} and R_{eq} can be simply expressed as follows.

$$\begin{aligned} C_{1eq} &= C_{1actual} \cdot I_{eq}/I_{actual} \quad (8) \\ C_{2eq} &= C_{2actual} \cdot I_{eq}/I_{actual} \\ R_{eq} &= R_{actual} \cdot I_{actual}/I_{eq} \end{aligned}$$

We evaluate the estimation accuracy. We generate CRC π load models of 1-2mm long interconnect with 100fF receiver input capacitance by Ref. [12]. The other evaluation conditions are the same with Section 3.4. Figure 17 shows the accuracy. The proposed concept works well for CRC π load model. Subsequently the effective capacitance can be calculated by conventional methods such as Ref. [13].

3.6. Characterization Cost

We here briefly review the characterization cost. Suppose a 3-input gate, and compare seven-dimensional table model in Eqs. (1) and (2) with the proposed method. When we construct the model of Eqs. (1) and (2), we assume five sample points in output load and input transition time, and three sample points in voltage level. As for the proposed method, we assume five sample points in output and input transition time and three points in voltage level in Eqs. (5) and

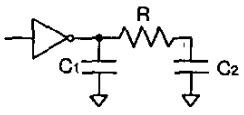

Figure 16: CRC π model.

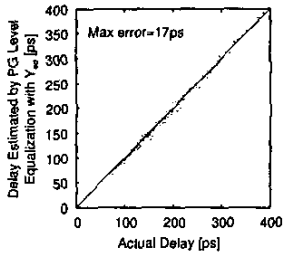

Figure 17: Delay estimation accuracy for CRC π load model (4x INV, fall transition).

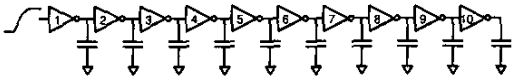

Figure 18: Experimental circuit for path delay evaluation.

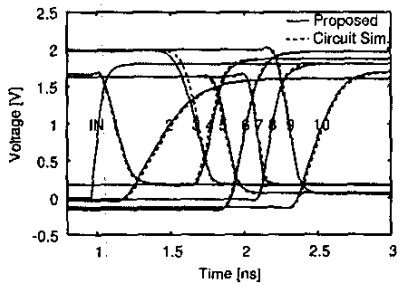

Figure 19: An example of propagating waveforms.

(6). When building the response surface function of current, we use five sample points for each voltage level. In summary, we have to execute 36,450 transient analysis for the seven-dimensional table model, whereas 1250 DC analysis and 150 transient analysis for the proposed method. The computational times are 3,584s and 15s respectively. The proposed method is 240 times as efficient as the naive table look-up model in characterization cost.

4. PATH DELAY CALCULATION

We show the results of path delay calculation by the proposed concept. We evaluate the propagating waveform in the circuit of Figure 18. The voltage levels of each gate and the capacitances are randomly varied, and the path delay is evaluated by a circuit simulator and by the proposed concept. The variation range is the same with Section 3.4. The total number of evaluation is 100. Figure 19 shows an example of propagating waveforms. The output waveform of each gate is shown, and the waveforms of the pro-

posed method are close to the circuit simulation results. The average estimation error is 1.6% and the maximum error is 3.3%. The proposed concept with the implementation shown in this paper achieves accurate timing analysis.

5. CONCLUSION

This paper presents a concept of "PG level equalization" that aims to perform timing analysis considering spatial power/ground level variation. By equalizing power/ground levels of driver and receiver and compensating current change by output load replacement, we can consider spatial PG level variation with a common compact gate delay model that has three variables. We confirm that the error of each gate delay is below 20ps in a 0.18μm technology, and the maximum estimation error of path delay is 3.3%.

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