Design and Measurement of 6.4 Gbps 8:1 Multiplexer in 0.18μm CMOS Process

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Abstract— We develop and measure a 8:1 multiplexer in a CMOS 0.18μm process. We design the hybrid multiplexer based on a prior detailed performance evaluation both of CMOS static and current mode logic circuits, and build a hybrid structure. The fabricated chip operates at up to 6.4 Gbps with power consumption of 84mW.

I. Introduction

Recently, over 10 Gbps/channel high-speed serial communication systems with all CMOS transceivers have been reported [1]. In such high-speed systems, key components are a multiplexer (MUX, parallel-to-serial converter)[2, 3] and a demultiplexer (DEMUX, serial-to-parallel converter). In these circuits, hybrid-type architecture, which consists of CMOS static logic and CML (Current Mode Logic), is often used because it can operate at high speed though the power consumption is relatively small[2]. To get the best performance, we must design a hybrid-type circuit based on accurate performance evaluation of CMOS static logic and CML.

In this work, we first evaluate and compare the performance of dividers composed of CMOS static logic and CML in a 0.18μm digital CMOS process. We then design and fabricate a hybrid 8:1 MUX based on the evaluation. We use CML for the final stage of the tree-type 8:1 MUX, which consists of 2:1 MUX and high-speed 1/2 divider. Measurement results show that it operates at 6.4 Gbps with power consumption of 84mW.

II. Comparison of CMOS Static Logic and CML

When we design high-speed serial communication circuits, we have two choices in logic style; CMOS static logic and CML. In such high-speed circuits, 1/2 divider is one of the highest-speed circuit, and the total performance of circuits depends on the divider performance. Hence, we first examine CMOS static and CML 1/2 dividers which consist of two D-latchs. Figure 1 shows the schematic of a D-latch.

Figure 2 shows the characteristics of the operating frequency versus current consumption evaluated by SPICE simulation using a 0.18μm process with 1.8 V power supply. In case of a CMOS static divider, the current consumption is proportional to the operating frequency. The maximum operating frequency is 2.5 GHz. In case of a CML divider, it can operate at higher frequency than a CMOS static divider, though it dissipates more current. When the current is 4 mA, a CML divider can operate at 12 GHz. It is over four times higher frequency. Table I summarizes the performance comparison of a CMOS static divider and a CML divider. A CML divider is superior to static divider in speed, but it consumes more power and its area is ten times larger. We should choose a CMOS divider in the part of circuits operating at below 2.5 GHz and a CML divider above 2.5 GHz from the point of area and power efficiency.

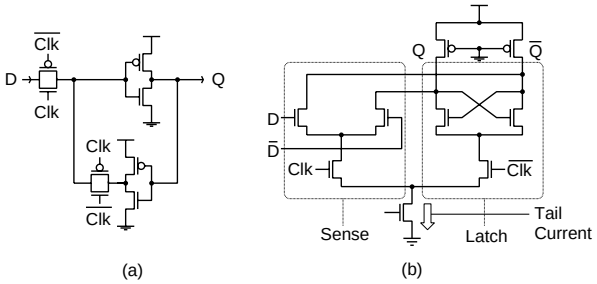

Fig. 1. Schematic of D-latch : (a) CMOS static logic, (b) CML.

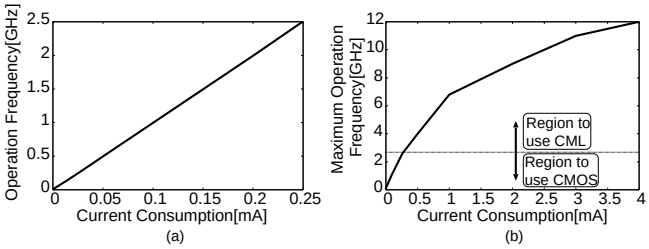

Fig. 2. Operating Frequency vs. Current of a divider: (a) CMOS Static Logic, (b) CML.

TABLE I
Performance Comparison of CMOS static and CML Divider.

	Maximum Frequency	Area
Static Logic	2.5 GHz	10μm×15μm
CML	12 GHz	40μm×60μm

III. Design of Hybrid 8:1 MUX

We design a high-speed, low power 8:1 MUX based on the discussion in the previous section. There are several choices in architecture: shift register-type, multi-phase type, tree-type, and so on. In such architecture, tree-type architecture is often used, because it can operate at the highest speed in these architectures. Moreover, its power consumption is the smallest. We also have three choices in logic style;

Choice 1: all CMOS static logic

Choice 2: all CML

Choice 3: hybrid of CMOS static logic and CML

In Choice 1, the area is the smallest of all. The operation frequency of MUX is limited by 1/2 divider. From Figure 2, it is 5 Gbps. In Choice 2, the maximum operating frequency is very high, and it is more than 20 Gbps. However, the area is over ten times larger than Choice 1, and power consumption is also large. A hybrid-type MUX of Choice 3 can operate at high frequency while saving area and power dissipation. We hence choose Choice 3, and design a hybrid high-speed, low power MUX. Figure 3 shows the configuration of the hybrid 8:1 MUX. The final 2:1 MUX and the first 1/2 divider, which operate at the highest speed, adopt CML, and the other part consists of CMOS static logic.

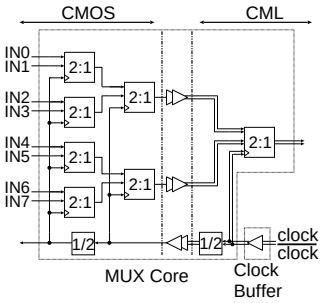

Fig. 3. Configuration of hybrid 8:1 MUX.

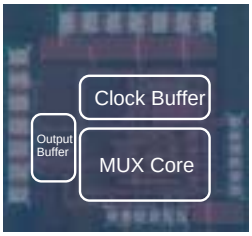

Fig. 4. Chip photograph of hybrid 8:1 MUX.

In designing a hybrid MUX, good determination of CML design parameters is important[4]. Especially, tail current is a key parameter that determines the maximum operating frequency and the total power consumption. Section II shows the relationship between tail current and operation frequency of a divider. We determine the current of a CML divider from the result of Figure 2. In case of the configuration in Figure 3, the operation frequency of MUX is less than 10 Gbps, because its operation frequency is limited by the maximum operation frequency of a CMOS static divider. A CMOS static divider operates at less than 2.5 GHz, and hence the overall operation frequency is limited to twice of the maximum operation frequency of a divider, 5 GHz. Therefore we should choose the necessary CML current for more than 5 GHz operation. Figure 2 (b) tells that CML current must be more than 700μA. We set 1.5mA as the tail current because of the robust operation.

IV. Measurement Results

We designed and measured a hybrid MUX in a 0.18 μm digital CMOS process. Figure 4 shows the chip photograph of the designed 8:1 MUX. Figures 5 and 6 show the measurement results by on-wafer probing. We measure the output waveform by a digital sampling oscilloscope. We give differential sin signals whose single-ended peak-to-peak amplitude is 400 mV. We give eight DC values for MUX input. In this case, the MUX outputs the corresponding eight-bit pattern periodically. Figure 5 shows the output of the designed MUX when IN0 - IN7 inputs are (1 0 1 0 1 0 0 1). Figure 5 (a) shows the waveform at 2 Gbps, and Figure 5 (b) shows the 6.4 Gbps output waveform. For this input configuration, the output should repeats (1 1 1 0 0 0 0 1) periodically. We confirm that the output is logically correct. Similarly, Figure 6 shows the output waveform when IN0 - IN7 inputs are (0 1 0 0 1 0 1 1). Although the output is logically correct, the attenuation in high frequency portion is remarkable, since the bandwidth of the integrated output buffer is not wide enough. From the measurement results, we confirm that the designed MUX operates at up to 6.4 Gbps. Table II shows the performance of the designed MUX. The total power consumption is 84 mW, and the area is 0.142mm^2. Although the MUX is designed for 10Gbps operation, the maximum throughput becomes 6.4Gbps, because of severe transistor mismatch in CML buffers used for clock distribution.

V. Conclusion

We design a CMOS hybrid 8:1 multiplexer in a 0.18μm digital process. We carefully evaluate and compare CMOS static logic and CML in speed, power and area, and determine the MUX structure and design parameters such as tail current and transistor width. Measurement results show that the fabricated chip operates at up to 6.4 Gbps.

Acknowledgement

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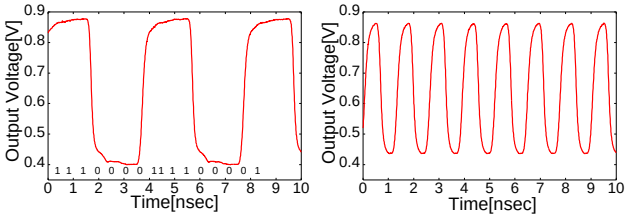

Fig. 5. Measured output waveform (IN0-IN7:10101001): (a) 2Gbps, (b) 6.4Gbps.

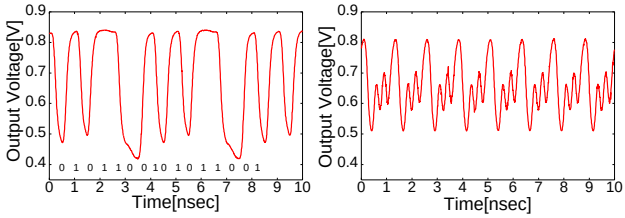

Fig. 6. Measured output waveform (IN0-IN7:01001011): (a) 2Gbps, (b) 6.4Gbps.

TABLE II
Performance of MUX.

	clockbuffer	core	total
Power Supply Voltage	1.8 V		
Process	0.18 μm		
Power@6.4 Gbps(mW)	59	25	84
Area(mm^2)	0.0495	0.0925	0.142