Return Path Selection for Loop RL Extraction

Akira Tsuchiya[1]   Masanori Hashimoto[2,3]   Hidetoshi Onodera[1]

[1]Dept. CCE, Kyoto University, [2]Dept. ISE, Osaka University, [3]PRESTO, JST

e-mail: {tsuchiya,onodera}@vlsi.kuee.kyoto-u.ac.jp, hasimoto@ist.osaka-u.ac.jp

Abstract— This paper propose a systematic method to select power/ground wires that should be considered in interconnect RL extraction. The return current distribution affects loop characteristic of interconnects. To extract exact RL value, all of return paths have to be considered. However it is impossible because there are huge number of P/G wires in LSIs. As more wires are considered, the extraction accuracy improves but the extraction cost increases undesirably. The proposed method focuses the energy dissipated at P/G wires and utilizes it for screening return paths. Experimental results reveal that our method enables accurate and computationally efficient RL extraction with considering return current distribution.

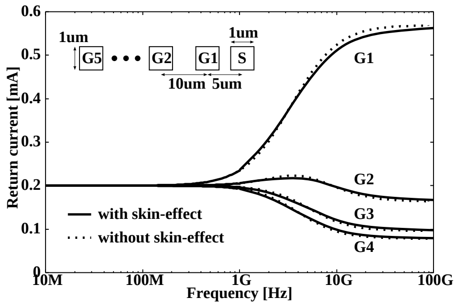

Fig. 1. Return current distribution with and without skin effect.

I. Introduction

According to advances in LSI fabrication technology, operating frequency is significantly increasing. In modern LSIs, on-chip inductance has a remarkable impact on circuit design e.g. timing analysis and noise estimation [1]. However it is hard to extract accurate inductance from on-chip interconnects. One reason for the difficulty is that the distribution of current return paths can not be easily predicted in LSI chips.

Conventionally, RL extraction is performed with considering the nearest one or two P/G wires [2]. Extraction with one or two P/G wires assumes that the almost all of the return current concentrate to the nearest P/G wires. In reality, the return current widely spreads even if the frequency is above multi-GHz. Reference [3] points out the problem that the extraction ignoring the return current distribution causes serious error. We have to consider the return current distribution when discussing high-performance interconnects [4]. However, there are tremendous number of P/G wires in LSIs. It is impossible to consider such huge number of wires because of the computational cost. To perform accurate and quick extraction, we have to choose P/G wires that contribute to dominant return current. However no systematic selection method has been proposed so far.

This paper proposes a method to screen necessary and sufficient P/G wires. As increasing the number of P/G wires in extraction, the extraction error decreases. We use energy dissipation as an indicator to decide how many P/G wires should be considered. Experimental results show that the energy dissipation of the modeled interconnect system correlates closely with the extraction error. Our method iteratively evaluates the energy dissipation as increasing the considered return-paths. We observe that the return-current distribution can be calculated without considering skin-effect, which considerably helps to reduce computational cost to screen P/G wires. The proposed method saves the unnecessary extraction cost imposed by the consideration of negligible P/G wires, while maintaining the extraction accuracy since it indicates the necessary and sufficient P/G wires with small additional computational cost.

In Section II, we introduce fundamental characteristics of return current and explain the problem discussed in this paper. In Section III, the proposed method is described. We then show some experimental results in Section IV, and Section V concludes the discussion.

II. Problem description

In this section, we explain a basic behavior of return current. The distribution of return current depends on the impedance of the power/ground net [1]. The return current distribution also depends on frequency because the impedance of power/ground net depends on frequency. Figure 1 shows a frequency characteristic of return current distribution. Y-axis is the return current of each ground wire when the signal wire is excited by a 1mA AC current source. The interconnect structure is shown in Fig. 1. There is a 1μm width signal wire and five ground wires are located with the pitch of 10μm in the same layer with the signal wire. The resistance and the inductance are extracted by a field-solver [5]. At low frequency, the same amount of return current flows in each ground wire because, in this case, the resistances of all ground wires are the same. As frequency becomes higher, return current concentrates to the closest ground wire (G1) because the reactance dominates the resistance. At near 100GHz, the return current distribution saturates to the distribution that is determined by the reactance only. Please note that all the return current does not concentrate to the nearest interconnect no matter how high frequency is. In high frequency, the resistance value and the inductance value depends on frequency because of skin- and proximity-effect. In Fig. 1, the solid lines show the result with considering skin- and proximity-effect. The dashed lines are that without considering skin- and proximity-effect. As you see, the current distribution ignoring skin- and proximity-effect is almost the same as the result with considering skin- and proximity-effect. Therefore we can estimate the current distribution without considering skin- and proximity-effect.

As mentioned in Reference [3], the number of power/ground wires considered in extraction affects the inductance value. This is because the return current distribution is different from

0-7803-8736-8/05/$20.00 ©2005 IEEE.

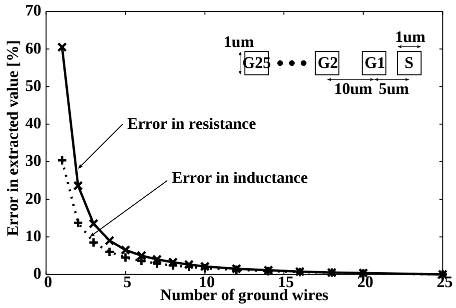

Fig. 2. Errors in extracted value. (at 100GHz)

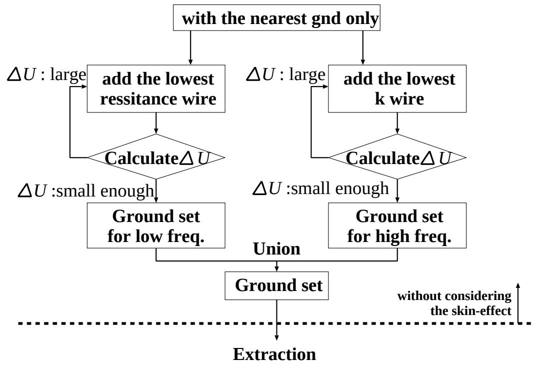

Fig. 3. Flow of the proposed method.

the actual one if only few power/ground wires are considered. Figure 2 shows the number of ground wires considered versus the extraction error at 100GHz. We assume the extracted value with 25 ground wires is a correct value, and Y-axis shows the error from the correct value. Figure 2 indicates that the extracted value only with the nearest ground contains more than 30% error. Return current is frequently misunderstood such that all current flows in the nearest ground wire at high frequency. However Figure 2 demonstrates that considering only the nearest ground causes extraction error even at high frequency such as 100GHz.

III. Proposed Method

In this section, we propose a return path screening method. As discussed so far, we have to consider several return paths for accurate RL extraction. Our method selects the necessary and sufficient ground wires by evaluating the variance of the energy consumed at the ground wires.

A. Flow of the proposed method

As mentioned in Section II, the return current distribution depends on frequency. Therefore the contribution of each ground wire to return current path is also frequency dependent. In low frequency, less resistive wires strongly affect the return current distribution. In high frequency, on the other hand, ground wires that have strong inductive coupling with the signal wire have a great impact on return current distribution. Therefore the return current distribution is frequency dependent as shown in Figure 1. To handle this frequency dependence, we merge two configurations; one is for low frequency, and the other is for high frequency.

The flow of the proposed method is summarized in Figure 3. The proposed method increments the number of considered P/G wires and judge whether enough P/G wires are selected or not by the value of ΔU, which will be explained in the next subsection. In the case of low frequency, we evaluate the energy difference ΔU_i by adding a ground wire in order from low resistance wires to high resistance ones. As mentioned in Section II, at the low frequency the resistance of P/G wires is a dominant factor to the return current distribution and the return current concentrates to low resistance wires. The inductances are ignored because the resistance is much larger than the reactance. In the case of high frequency, we evaluate the energy difference ΔU_i by adding a ground wire in order from the wires that have the largest inductive coupling coefficient k. Here the coupling coefficient is defined by $M/\sqrt{L_1 L_2}$ where M is the mutual-inductance, L_1 and L_2 are the self-inductance. The coupling coefficient depends on the geometry of two wires and easily calculated from the inductance matrix of PEEC model. The resistances are ignored in high frequency range because the reactance is much higher than the resistance. By combining these two sets, our method obtains a necessary and sufficient ground wire set that can cover low to high frequency.

B. Indicator for return path selection

We explain the indicator ΔU of the proposed method. The proposed method calculates the energy dissipated at the ground wires when a signal wire is excited. The accurate estimation of the dissipated energy is a necessary condition that the return current distribution is well estimated. In nature, the loop current flows in the path where the dissipated energy becomes the smallest. As the number of ground wires increases, the freedom of the return current paths increases, and hence the dissipated energy must decrease monotonously as the number of power/ground wires increases. Finally the dissipated energy approaches to a certain value. Therefore the configuration of ground wires whose energy dissipation is close to the saturated value corresponds to accurate return current distribution.

First, we evaluate the PEEC model of the interconnects. As mentioned in Section II, we ignore skin effect, because skin and proximity effects are secondary factors that determine return current distribution and less important. The interconnect resistances are determined by interconnect length, cross section and metal resistivity. The partial-self-inductance is determined similarly. The partial-mutual-inductance between paired wires is determined by the positional relationship of the pair of wires. Thus we can easily construct a PEEC model by analytical methods [6].

From the PEEC model, we can calculate the return current distribution analytically. For low frequency region, we index ground wires in the ascending order of resistance. For high frequency region, we index ground wires in order of the distance from the signal wire, i.e., the closest ground wire to the signal wire is labeled 1. We write the return current flowing in the i-th ground as i_i.

Next, we calculate the energy dissipation at ground wires

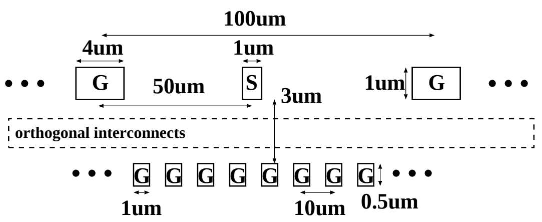

Fig. 4. Evaluated interconnect structure.

incrementally. At the beginning, we evaluate the signal wire only with the closest ground wire. In this case, all return current flows in the closest ground wire. We next calculate the energy with two ground wires. We write the energy consumption U_i when i ground wires are considered. U_i is expressed by using the return current distribution,

$$U_i = \sum_j R_{jj} i_j, \qquad (1)$$

where R_{jj} is the resistance of the j-th ground wire. We here define the difference of the energy as

$$\Delta U_i = (U_{i-1} - U_i)/U_{i-1}. \qquad (2)$$

The difference ΔU_i means the energy variation when i-th ground wire is added. If the difference ΔU_i becomes small, the extracted RL values are expected to converge to the accurate value. Therefore we have to add ground wires until the difference ΔU_i becomes small enough. In extraction, we use the ground wire set that makes the difference ΔU_i small enough.

As explained so far, return current flows such that the energy of the system becomes minimum. The experimental results show that ΔU points the upper limit of extraction error. Furthermore, the calculation cost for ΔU is negligible small. In PEEC based field-solvers such as Ref. [5] calculate current distribution to evaluate the loop characteristics. The proposed method can use this information of current distribution. Section B describes the computational cost of our method.

IV. Experimental Results

This section shows some experimental results to verify that our method can select necessary and sufficient return paths. Then the computational cost of our method is discussed. We show the calculation cost to select the return paths is much smaller than that of RL extraction.

A. Extraction accuracy

In real chips, the interconnect structure is a complicated 3D structure. We assume a bus structure as shown in Figure 4. There are 4μm width ground wires at the pitch of 100μm. These wires represent P/G wires and shielding wires in bus structure. In the lower layer, there are orthogonal interconnects but they do not affect return current distribution. In the further lower layer, 1μm width ground wires are located with the pitch of 10μm. These width and pitch correspond to P/G wires in standard cell.

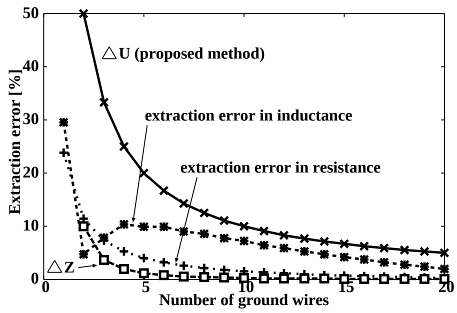

Fig. 5. Extraction error of the loop impedance and the proposed indicator ΔU (realistic structure, at 1MHz).

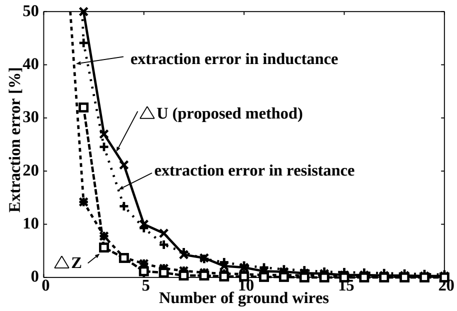

Fig. 6. Extraction error of the loop impedance and the proposed indicator ΔU (realistic structure, at 100GHz).

Figure 5 shows the relation between the number of considered return paths and the extraction error in low frequency region. Here the resistances of ground wires dominantly decide the return current distribution, and the return current tends to flow in thick wires. Figure 5 shows the proposed ΔU gives a good indication for error convergence. ΔZ is the loop impedance difference and it is defined by

$$\Delta Z_i = (Z_{i-1} - Z_i)/Z_{i-1}. \qquad (3)$$

in a similar way to ΔU. On the other hand, although the convergence tendency of ΔZ is close to the extraction error and ΔZ could be used as an indicator, it is difficult to set the threshold value, because the ratio of the extraction error and ΔZ varies in disorder. In addition, the calculation of ΔZ requires more computation than that of ΔU, and hence the proposed method adopts ΔU as an indicator.

Figure 6 shows the results in high frequency region. In high frequency region, the return current distribution depends on inductive coupling. The return current concentrates to nearer ground wires. Therefore the proposed method selects return paths from the nearest ground wire. By the case of Figure 4, the return current concentrates to the thin wires in lower layer. Figure 6 shows the convergence of ΔU is close to the extraction error.

Figure 7 shows the selected wires when we set the target ΔU to 10% in Figure 5 and Figure 6. In Figure 7, "Conventional" shows the result of Ref. [2]. Reference [2] is a method to choose return-paths by the geometry of P/G wires. The conventional method selects 2 wires and the proposed method select 16 wires. The extracted loop characteristics are shown

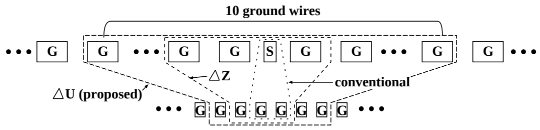

Fig. 7. Considered ground wires for RL extraction (realistic structure).

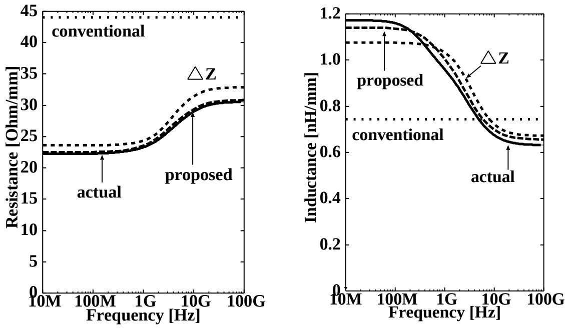

Fig. 8. Frequency characteristics of selected interconnects (realistic structure of Figure 7).

in Figure 8. The conventional method selects too few ground wires and causes over 90% error in loop resistance and over 30% in loop inductance. On the other hand, the results of the proposed method agree with the actual values.

B. Computational cost

The proposed method needs a certain extra cost to select return paths. We evaluate the computational cost of the proposed method. Figure 9 shows the relation between the number of considered wires and extraction cost. The interconnect structure is Figure 4 and we use a field-solver [5] on a 750MHz SPARC workstation. The solid line is the extraction cost only, and the dashed line labeled "extraction + return path selection" is the sum of the extraction time and the time to select return paths by our method. The dashed line labeled "increase of extraction time" shows the ratio of the additional cost to the extraction cost. Figure 9 shows the extraction cost increases rapidly as the number of wires increases. On the other hand, the additional cost by the proposed method is relatively small and grows slowly as increasing the number of wires. This is because the proposed method ignores skin-effect when it selects return paths. When the number of wires is large, the additional cost by our method is only several percent of the extraction cost. The extra cost to use the proposed method is much smaller than the extraction cost with conservatively considering many interconnects. When the number of wires is small, the ratio of the additional cost to the extraction cost may be over 30%. But in this case, the absolute value of the additional cost is several seconds at most. From above discussion, we conclude the proposed method can select adequate return paths with negligible additional computational cost.

V. CONCLUSION

A return path screening method for interconnect RL extraction is proposed. The proposed method evaluates the energy dissipated at ground wires, and judges whether the energy dissipation in the ground wires is small enough or not, because the return current flows in the paths with the minimum energy consumption in nature.

The return current distribution strongly depends on frequency. At low frequency, the resistance is dominant and the inductance becomes significant as frequency becomes higher. The proposed method calculates two windows for the resistance-dominant low-frequency region and for the inductance-dominant high-frequency region. By merging these two windows, the proposed method provides a necessary and sufficient ground wire configuration that enables accurate extraction at all frequencies.

The proposed method can also save the extraction cost. The extraction cost by a 3D field-solver increases exponentially as the number of considered wires increases. The proposed method can select the necessary and sufficient ground wires with negligible small extra computational cost. Therefore the proposed method enables the accurate and efficient extraction considering return current distribution.

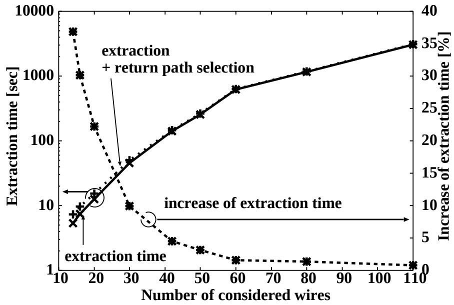

Fig. 9. Extraction cost and the additional cost by the proposed method.

ACKNOWLEDGEMENT

This work is supported in part by the 21st Century COE Program (Grant No. 14213201).

REFERENCES

[1] C.-K. Cheng, J. Lillis, S. Lin, and N. H. Chang, "Interconnect Analysis and Synthesis," A Wiley-Interscience Publication., 2000.

[2] K. L. Shepard and Z. Tian, "Return-Limited Inductances: A Practical Approach to On-Chip Inductance Extraction," *IEEE Trans. CAD*, vol.19, no.4, pp.425–436, Apr 2000.

[3] S. Y. Kim, Y. Massoud, and S. S. Wong, "On the Accuracy of Return Path Assumption for Loop Inductance Extraction for 0.1μm Technology and Beyond," *ISQED*, pp.401–404, 2003.

[4] X. Huang, P. Restle, T. Bucelot, Y. Cao, T.-J. King, and C. Hu, "Loop-based Interconnect Modeling and Optimization Approach for Multigigahertz Clock Network Design," *IEEE JSSC*, vol.38, no.3, pp.457–463, Mar 2003.

[5] M. Kamon, M. J. Tsuk, and J. K. White, "FASTHENRY: a multipole-accelerated 3-D inductance extraction program," *IEEE Trans. MTT*, vol.42, no.9, pp.1750–1758, Sept. 1994.

[6] R.-B. Wu, C.-N. Kuo, and K. K. Chang, "Inductance and Resistance Computations for Three-Dimensional Multiconductor Interconnection," *IEEE Trans. MTT*, vol.40, no.2, pp.263–271, Feb 1992.