

Timing Analysis Considering Temporal Supply Voltage Fluctuation

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Abstract— This paper proposes an approach to cope with temporal power/ground voltage fluctuation for static timing analysis. The proposed approach replaces temporal noise with an equivalent power/ground voltage. This replacement reduces complexity that comes from the variety in noise waveform shape, and improves compatibility of power/ground noise aware timing analysis with conventional timing analysis framework. Experimental results show that the proposed approach can compute gate propagation delay considering temporal noise within 10% error in maximum and 0.5% in average.

I. INTRODUCTION

Power integrity has become a critical problem in LSI design, and many techniques have been studied to suppress power supply noise, such as topology optimization[1], decoupling capacitance insertion[2]. However, it is impossible to supply ideal power/ground voltage for every element inside a chip, and a certain amount of power/ground (PG) noise must be taken care of in chip design. So far, PG noise is considered in best/worst case analysis that applies high/low supply voltage to all instances in a chip. This analysis worked well as long as the influence of PG noise on timing is not significant. However, recently supply voltage becomes lower and modern LSIs become current hungry, which makes delay variation due to PG noise as well as PG noise itself severe, and hence it becomes difficult to set the best/worst case scenarios without over- and underestimation.

Recently timing analysis considering PG noise is studied, and the problem is broken down into following two issues; how to find the worst-case noise pattern[3], and how to compute propagation delay[4, 5, 6, 7]. These works on timing analysis including power supply noise assume that ground levels of a driver and its receiver are the same. This is true when the driver and the receiver are placed in neighborhood. However when they are placed far away, ground level as well as power level becomes different because power/ground noise varies spatially. Some recent works on propagation delay computation focus on the mismatch problem of power/ground level between driver and receiver[5, 6, 7, 8, 9]. Another problem of the conventional studies is that temporal voltage variation, which means steep supply voltage change whose time constant is comparable with gate propagation delay, is not appropriately handled. Reference [9] indicates that circuit delay is approximately estimated not by peak noise voltage but by average supply voltage. However it is not clear how the temporal power/ground noise should be considered in common gate-level static timing analysis. Reference [10] shows a trend that (cycle time)/(FO4 delay) is decreasing. Generally speaking, at clock edges, power supply noise becomes large because current and its derivative are large. Therefore, the voltage variation is getting steeper, and it becomes difficult to regard power supply voltage constant during gate switching. Gate delay calculation considering temporal voltage variation is difficult, since the noise waveform can become various shapes. Therefore pre-characterization approach for various noise shapes is impractical.

This paper focuses on temporal supply voltage fluctuation, and proposes an approach to handle temporal voltage fluctuation in a com-

patible manner with gate-level static timing analysis. The proposed approach replaces the temporal variation with an equivalent constant supply voltage that makes gate propagation delay equal. We then reveal that the proposed method works well for path delay calculation.

This paper is organized as follows. Section II shows impact of temporal supply voltage fluctuation on timing and clarifies motivation of this work. Section III proposes an approach that replaces temporal voltage fluctuation with an equivalent supply voltage. Section IV shows experimental results, and Section V concludes the discussion.

II. MOTIVATION

This section demonstrates the problem of temporal supply voltage fluctuation. We evaluate the impact of temporal supply noise on gate propagation delay using an experimental circuit of Figure 1. We give a triangle power or ground noise and evaluate the output waveform, where the given triangle noise is expressed by three parameters; V_d , t_d and t_s . We assume a $0.18\mu\text{m}$ CMOS technology, and the nominal supply voltage is 1.8V.

Figure 2 shows an example of transition waveforms with and without power supply noise, where $V_d=0.2\text{V}$, $t_d=0.2\text{ns}$, $t_s=0.8\text{ns}$, $C_o=100\text{fF}$ and the input transition time is 0.1ns . In this case, the 50%-50% propagation delays with and without noise are 122ps and 132ps respectively. The delay with noise is shorter than that without noise by 8%. Because the power noise is injected just before the input transition starts, the output voltage is below V_{dd} when the input transition begins. The amount of charge that must be discharged through NMOS becomes small, and hence the propagation delay gets shorter.

Another example is shown in Figure 3. Power noise is injected to rise output transition, where $V_d=0.2\text{V}$, $t_d=0.2\text{ns}$, $t_s=1.0\text{ns}$, $C_o=25\text{fF}$ and the transition time of the input signal is 0.1ns . In this situation, the power noise reduces the charging ability of PMOS, because PMOS gate-source voltage V_{gs} changes. The propagation delay increases from 201ps to 232ps by 15%.

The temporal power/ground noise has various voltage waveforms, even if the shape is assumed to be triangle. In this example, there are three parameters, t_s , t_d , V_d . Pre-characterization approach to evaluate the propagation delay in advance for various noise waveforms is prohibitive due to computational cost, and hence we need a simple yet accurate modeling that can capture the impact of temporal power/ground noise on delay.

III. EQUIVALENT POWER/GROUND VOLTAGE APPROACH

This section presents a new approach to cope with the temporal power/ground noise. The propagation delay variation must be modeled in a simple way with small computational cost while maintaining the accuracy. In addition, compatibility with the conventional static timing analysis method is desirable.

We propose an approach called “equivalent power/ground voltage” that satisfies the above requirements. The proposed approach replaces the temporal power/ground noise with an equivalent power/ground voltage that makes the propagation delay equal to the delay with the original temporal noise. This replacement condenses the power/ground noise shape into one parameter of the equivalent power/ground voltage, and the number of parameters that should be

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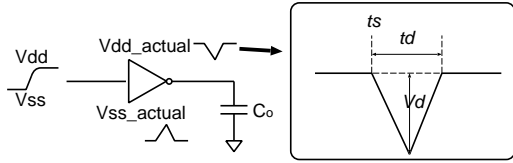


Fig. 1. Experimental circuit.

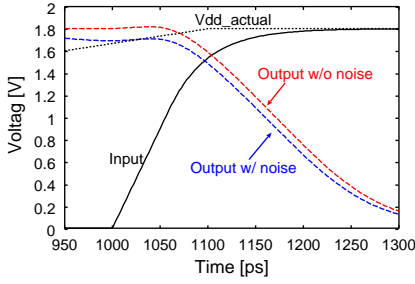


Fig. 2. A waveform example of fall transition with power noise (charge change case).

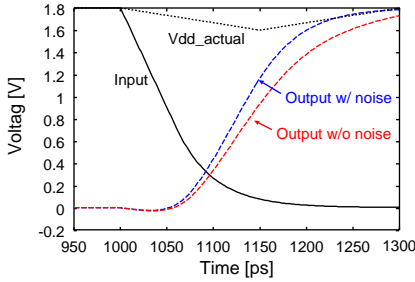


Fig. 3. A waveform example of rise transition with ground noise (current change case).

considered is much reduced. Once the equivalent voltage is obtained, the models that can handle power/ground voltage level variation, such as [5, 6, 7, 8, 9], can be used for path delay calculation.

As shown in Figures 2 and 3, there are two mechanisms to change the propagation delay. Although power noise cases are shown in the previous section, delay variation by ground noise is also classified into the same two mechanisms, that is rise transition with ground noise is similar with Figure 2, and the fall transition with ground noise corresponds to Figure 3. We therefore consider these two mechanisms separately, and develop a way to compute the equivalent power/ground voltage. Hereafter, we call the situation in Figure 2 as “charge change case”, which means that the power/ground noise varies the amount of charge to be charged/discharged. The situation in Figure 3 is called as “current change case”, since the power/ground noise changes the charging/discharging ability.

A. Charge Change Case

We first discuss the charge change case. Suppose that the output is falling with power supply noise as shown in Figure 4. In this case, the output voltage V_{t0} at the timing when the output transition starts (t_0) is important, because the output swing becomes different from V_{dd} and the amount of charge poured to the output loading changes, which results in variation in propagation delay. From another point of view, the propagation delay in this case is close to the delay when the supply voltage is V_{t0} . Actually, this is true when the input transition time is small, because PMOS immediately becomes off. We hence set the equivalent power voltage to V_{t0} .

$$V_{dd_eq} = V_{t0}. \quad (1)$$

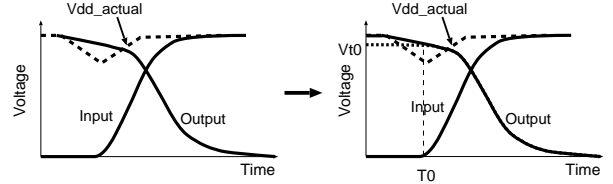


Fig. 4. Calculation of equivalent power voltage in charge change case.

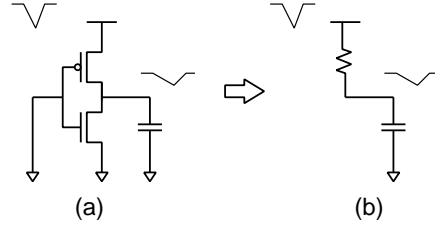


Fig. 5. Calculation of output voltage V_{t0} .

An issue is how to obtain V_{t0} . The output is connected to power or ground through MOS transistors (Figure 5 (a)). Also the gate output has fan-out loading and interconnect capacitance. Therefore, the power/ground voltage and the output voltage are not necessary the same. The difference becomes large, as the time constant of the output load and MOS resistance increases relatively compared with the time constant of the power supply noise. From another point of view, filtered noise through RC network appears at the output. It is not trivial to calculate V_{t0} considering MOS non-linear characteristics. We then approximately calculate the output voltage by using the equivalent circuit in Figure 5 (b). The resistance that corresponds to the hold PMOS transistor is calculated by operating point analysis. When power noise waveform is given in a closed-form expression, the output waveform can be analytically derived.

Above discussion handles power supply noise, but the equivalent ground voltage V_{ss_eq} can be modeled and calculated similarly.

B. Current Change Case

We next discuss the current change case. We here suppose that power supply voltage is fluctuated when the output is rising as shown in Figure 3. In this case, power supply noise affects the current to charge output loading, which results in variation in gate delay. To capture this effect, we should know the average charging ability, because the gate propagation delay is the time required to charge up the output loading. We therefore calculate the equivalent power voltage V_{dd_eq} as follows.

$$V_{dd_eq} = \frac{\int_{t_1}^{t_2} V_{dd_actual} dt}{t_2 - t_1}, \quad (2)$$

where V_{dd_actual} is the actual power voltage with noise, and t_1 and t_2 are the start and end timings of the integration. Figure 6 explains the calculation of V_{dd_eq} . We calculate the average power voltage between t_1 and t_2 . The problem here is how to set t_1 and t_2 . We empirically found that the modeling error becomes minimum when we set t_1 to the timing when the output starts the transition, and t_2 to the timing when the output voltage swing becomes 60% of V_{dd} . More reasonable combination of t_1 and t_2 may exist, but above setting still provides accurate estimation. Rigidly speaking, we can not estimate these timings exactly because these timings depend on power supply noise, and it is a chicken-and-egg problem. However, we experimentally observe that the modeling accuracy is hardly degraded even if we calculate the timings of t_1 and t_2 without considering power noise.

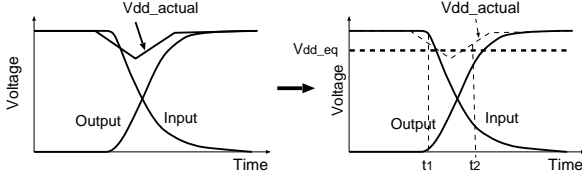


Fig. 6. Calculation of equivalent power voltage in current change case.

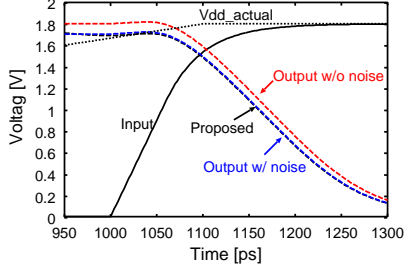


Fig. 7. Waveform estimated by proposed method (experimental setup is the same with Figure 2).

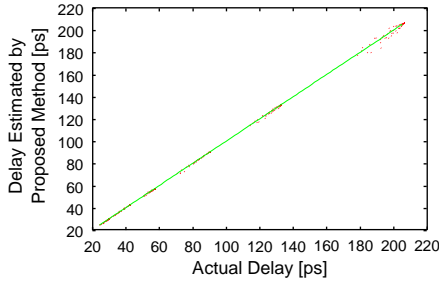


Fig. 8. Estimation accuracy of delay (INV, fall transition, power noise).

We can similarly calculate the equivalent ground voltage in the case that the output is falling.

$$V_{ss_eq} = \frac{\int_{t_1}^{t_2} V_{ss_actual} dt}{t_2 - t_1}, \quad (3)$$

where V_{ss_actual} is the actual ground voltage with noise.

IV. EXPERIMENTAL RESULTS

This section shows experimental results to verify the proposed approach.

A. Charge Change Case

We first evaluate the accuracy of the charge change case. Figure 7 shows the output waveform estimated by using the proposed approach. The experimental conditions are the same with Figure 7. The waveform of the proposed approach is almost the same with the actual waveform with noise. The proposed approach that replaces temporal noise with an equivalent power/ground voltage works well.

We evaluate the fall propagation delay of inverter with power noise varying t_s (0ns, 0.2ns, 0.4ns, 0.6ns, 0.8ns, 1.0ns, 1.2ns, 1.4ns, 1.6ns, 1.8ns), V_d (0.1V, 0.2V), t_d (0.3ns, 0.6ns, 1.0ns, 1.5ns), C_o (5fF, 25fF, 100fF) and the input transition time (0.1ns, 0.5ns). The total number of evaluation is 480. Figure 8 shows the accuracy of the proposed approach. The x-axis is the delay estimated by circuit simulation with actual temporal noise. The y-axis is the delay estimated by circuit simulation with the equivalent power voltage. We can see that the proposed approach provides the accurate propagation delay. The average and maximum estimation errors are 0.3% and 4.3% respectively.

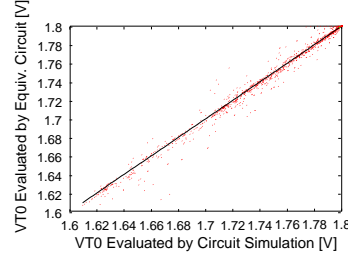


Fig. 9. Estimation accuracy of V_{t0} (PMOS is holding).

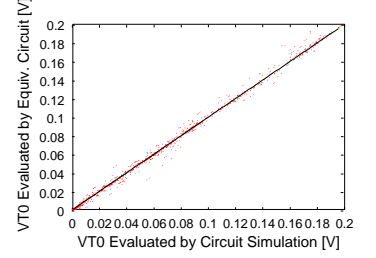


Fig. 10. Estimation accuracy of V_{t0} (NMOS is holding).

We next show the estimation error of V_{t0} caused by simplified calculation. We calculate and compare V_{t0} using the two circuit models shown in Figure 5. Figure 9 shows the result when PMOS is holding the output voltage, and Figure 10 corresponds to the case that NMOS is holding. We use inverter, 2-input nand, 2-input nor, 4-input nand and 4-input nor gates in the experiment. The variation of C_o and the noise waveform shape is the same with the above experiment. The total number of evaluation is 1920 for PMOS and 1920 for NMOS. The maximum error is 55mV and the average error is 2mV. The benefit of the simplified calculation in Figure 5 (b), which enables us to compute V_{t0} analytically when the power/ground noise waveform is given by a closed-form expression, dominates the accuracy degradation of V_{t0} . The estimation error of the propagation delay due to V_{t0} error will be discussed in the next paragraph.

Table I summarizes the maximum and average accuracy of the delay estimation. We compare the proposed method with the following three methods.

Method 1 V_{t0} is accurately estimated using the circuit model in Figure 5 (a). This accuracy is expected to be better than the proposed method that uses Figure 5 (b).

Method 2 V_{t0} is the power/ground noise voltage at the timing when the output transition starts. In other words, MOS holding resistance is ignored.

Ignore Noise The delay is evaluated assuming ideal power/ground voltage without considering power/ground noise.

The maximum error of the proposed method is 10.3%, and the average error is 0.5%. When ignoring power/ground noise, the estimation error becomes 75% at maximum, which reveals the necessity of the delay modeling that can cope with temporal power/ground noise. The maximum and average errors of Method 1 are 7.3% and 0.4% respectively. The estimation error of V_{t0} shown in Figures 9 and 10 slightly increases the average error by 0.1%. Compared with Method 2, the maximum error of the proposed method is smaller by 3.1%. The consideration of MOS holding resistance and output capacitance contributes to improve the accuracy.

B. Current Change Case

We next demonstrate experimental results of current change case. Figure 11 shows the output waveform derived by the proposed approach. The experimental setup is the same with Figure 3. The waveform of the proposed approach is close to the actual waveform with noise.

Figure 12 demonstrates the delay estimation accuracy when the output of inverter is rising with power noise. The maximum and average errors are 3.6% and 0.3%. The proposed approach works well in current change case as well as in charge change case.

Table II lists the maximum and average error in various conditions. The maximum and average error is 9.6% and 0.4%. We conclude that the proposed “equivalent power/ground voltage” approach is effective.

TABLE I
ACCURACY OF DELAY ESTIMATION (CHARGE CHANGE CASE).

Rise/ Fall (Noise)	Cell	Estimation Error (%)							
		Proposed		Method 1		Method 2		Ignore Noise	
		Max	Avg	Max	Avg	Max	Avg	Max	Avg
Rise (Vss)	INV	5.8	0.4	5.4	0.4	9.9	0.7	61.2	3.9
	NAND2	3.9	0.4	3.7	0.3	8.0	0.8	48.6	4.2
	NAND4	6.0	0.5	2.8	0.2	9.5	1.1	34.6	3.5
	NOR2	6.2	0.5	5.9	0.5	7.7	0.7	34.3	3.3
Fall (Vdd)	INV	4.3	0.3	4.3	0.3	9.7	0.9	75.1	4.1
	NAND2	4.7	0.6	4.1	0.5	8.3	0.9	39.7	3.3
	NAND4	7.2	0.8	7.3	0.8	8.8	1.1	23.8	2.5
	NOR2	6.7	0.4	2.9	0.2	9.2	1.2	54.1	4.0
NOR4	10.3	0.6	1.4	0.1	13.4	1.7	32.8	3.0	
Average		-	0.5	-	0.4	-	0.9	-	3.5

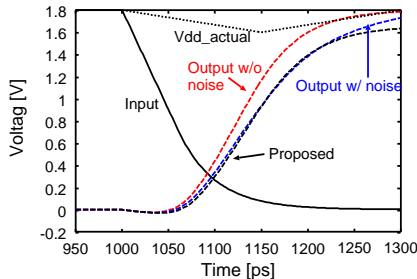


Fig. 11. Waveform estimated by proposed method (experimental setup is the same with Figure 3).

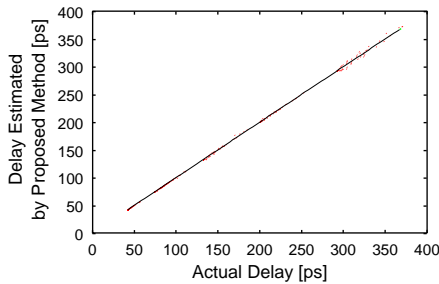


Fig. 12. Estimation accuracy of propagation delay (INV, rise transition, power noise).

TABLE II
ACCURACY OF DELAY ESTIMATION (CURRENT CHANGE CASE).

Rise/ Fall	Noise	Cell	Estimation Error (%)			
			Proposed		Ignore Noise	
			Max	Avg	Max	Avg
Rise	Vdd	INV	3.6	0.3	33.5	4.6
		NAND2	4.1	0.3	35.1	4.7
		NAND4	4.5	0.3	36.1	4.7
		NOR2	2.8	0.3	26.8	4.0
Fall	Vss	INV	8.9	0.3	51.3	6.0
		NAND2	6.3	0.3	39.4	5.1
		NAND4	9.3	0.5	30.6	4.5
		NOR2	9.2	0.3	52.5	6.1
NOR4	9.6	0.5	49.3	5.9		
Average		-	0.4	-	5.0	

C. Path Delay Evaluation

We finally apply the proposed approach to path delay evaluation. The experimental circuit is Figure 13. We give four noise waveform shapes, and evaluate the path propagation delay. Figure 14 shows an

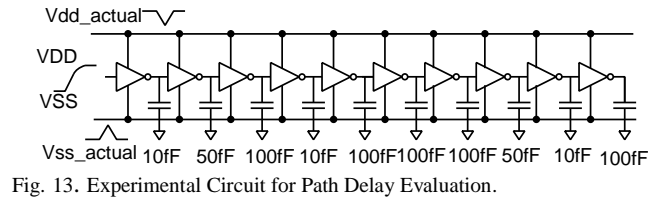


Fig. 13. Experimental Circuit for Path Delay Evaluation.

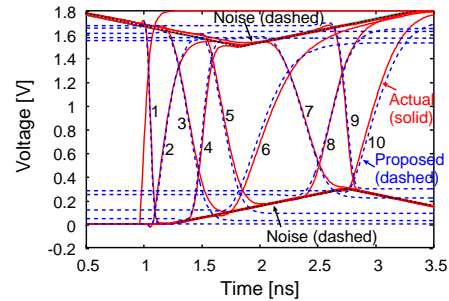


Fig. 14. Path Delay Evaluation (Case1).

example of the propagation waveforms. We can see that the transition waveforms at each gate are well estimated. The estimation error of the path delay is -0.1% to 4.4%.

V. CONCLUSION

This paper presents an approach to consider delay variation due to temporal power/ground noise in gate-level timing analysis. The proposed approach replaces temporal power/ground noise with an equivalent power/ground voltage that provides the equal propagation delay. We find that there are two mechanisms of delay variation due to temporal noise, and devise a method to derive the equivalent power/ground voltage for each mechanism. We experimentally verify the accuracy of the proposed approach. The maximum and average estimation errors of gate propagation delay are 10 and 0.5% respectively. We also demonstrate that the proposed approach can work well for path delay calculation.

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