Statistical Analysis of Clock Skew Variation in H-tree Structure

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Abstract

This paper discusses clock skew due to manufacturing variability and environmental change. In clock tree design, transition time constraint is an important design parameter that controls clock skew and power dissipation. In this paper, we evaluate clock skew under several variability models, and demonstrate relationship among clock skew, transition time constraint and power dissipation. Experimental results show that constraint of small transition time reduces clock skew under manufacturing and supply voltage variabilities, whereas there is an optimum constraint value for temperature gradient. Our experiments in a 0.18μm technology indicate that clock skew is minimized when clock buffer is sized such that the ratio of output and input capacitance is four.

1. Introduction

Clock skew minimization is an important design task to ensure correct circuit behavior of sequential circuits, and many works have been done to design zero-skew clock tree (see Reference [1]). Factors that cause clock skew are classified into three categories; design uncertainty, manufacturing variability and environmental change. The main problem of design uncertainty is error of capacitance estimation. Even if we reduce design uncertainty by using detailed analysis and optimization, clock skew occurs due to manufacturing and environmental variabilities. As clock frequency increases, clock skew specification becomes severer, and hence we must design a clock tree that is robust against those variabilities.

Recently, high-performance microprocessor design adopts techniques that adjust clock skew after fabrication [1, 2]. These techniques are effective for microprocessor design. However, ASIC can not utilize it due to cost problem. In clock design, limiting signal transition time is an important factor that controls clock skew and power dissipation. Reference[3] discusses clock skew variation due to interconnect variations. References[4, 5] analyze clock skew under manufacturing and environmental variabilities. However it is not clear how the limitation of transition time affects clock skew. We must understand how the limitation of transition time varies robustness of clock tree, and determine a proper limitation under given constraints of clock skew and power dissipation.

In this paper, we design five clock trees that have different transition time constraint, and evaluate clock skew under voltage fluctuation, transistor length variation, and temperature gradient. We demonstrate the relationship among clock skew, transition time constraint and power consumption. This paper is organized as follows. Section II explains a clock tree model and variability models used in our analysis. Section III evaluates clock skew under the variability models of supply voltage, transistor length and temperature. We finally conclude the discussion in Section IV.

2. Evaluation Model of Clock Skew

This section explains experimental setup for clock skew evaluation. We first show a design policy of clock tree, and then explain variation models of transistor length, supply voltage and temperature.

2.1. Clock Tree Design

We design and analyze clock trees whose topology is H-tree. In this paper, we assume a uniform distribution of flip-flops. We assume a 10x10mm chip in a 0.18μm technology. The number of stages in H-tree is four as shown in Figure 1, and we place a driver at each junction (b–i) and sink.(a) The half of the chip area is occupied by flip-flops. In this condition, each sink (a) has 1,250 flip-flops that correspond to 8.75pF.

We assume the interconnect structure shown in Figure 2. In the case of a nominal width interconnect, coupling capacitance $C_{\rm c}$ is 0.0575fF/μm, and capacitance to ground $C_{\rm g}$ is 0.0950fF/μm. Resistance R is 0.0846Ω/μm.

In clock tree design, wire sizing is a common technique, and in the experiments, we assign 8x wire between g and i, 4x between e and g, 2x between c and e, and 1x between a and c. For each width, we approximately calculate interconnect capacitance $C_{\rm int}$ as follows.

$$C_{\rm int} = (2C_{\rm c} + C_{\rm g}w)l, \quad (1)$$

where w is the wire width ratio to the nominal width, and l is the wire length. This approximation is not accurate, but

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the effect of wire sizing can be considered. Interconnect resistance $R_{\rm int}$ is

$$R_{\rm int} = R \cdot l/w. \quad (2)$$

In simulations, we model an interconnect as a 3-π ladder model, since Reference [6] indicates that 3-π model provides accurate simulation whose error is below 3%. In this paper, wire inductance is not considered.

In clock tree design, determination of the maximum transition time is important both for skew control and power dissipation, because there is a tradeoff between power dissipation and skew[7]. In this paper, we quantitatively examine the relationship among the maximum transition time, power dissipation and skew. We use a parameter $\lambda = C_{\rm out}/C_{\rm in}$ to control the transition time, where $C_{\rm in}$ is the input capacitance of the driving inverter and $C_{\rm out}$ is its output load capacitance to drive. $C_{\rm out}$ includes the input capacitances of the receiver gates, wire capacitance and the diffusion capacitance of the driver. Reference [6] indicates that the delay of a cascaded driver, which drives a large load, becomes minimum when $\lambda = e$. In practical designs, λ is often set 4 – 6.

In this paper, we vary λ from 3 to 7, and evaluate skew, transition time and power dissipation under various variation models. We place inverters at each junction and sink. The driver sizes are decided from sink (a) to source (i) in sequence to satisfy the given constraint of λ. Table 2.1 shows the sizes of each driver. The columns of a – i correspond to the driver positions shown in Figure 1. The transistor sizes are normalized by a unit inverter, whose NMOS is L=0.2μm, W=2.6μm and PMOS is L=0.2μm, W=5.5μm. The size ratio of PMOS and NMOS is determined such that the output impedance for rise and fall transitions becomes the same. The output impedance of the unit inverter is 1.1kΩ. The input capacitance is 14.3fF, and the output diffusion capacitance is 5.8fF. The driver size at i is different, but this difference does not cause clock skew because the upper path from PLL to i is shared by all sinks, although it may affect jitter.

Figure 3(a) shows the relation between λ and the propagation delay from source (i) to sink (a). The delay becomes the minimum when λ is 4. Figure 3(a) also shows the transition time. The transition time is proportional to $\lambda = C_{\rm out}/C_{\rm in}$. Figure 3(b) demonstrates the power dissipation when the clock frequency is 250MHz. As λ becomes small, the power dissipation increases. The power consumed by drivers is much different for each λ value. When $\lambda = 3$, it is 0.82W and four times larger than that of $\lambda = 7$.

2.2. Variation Model

We next explain variation models used in the experiments. We focus on three variation sources; transistor length

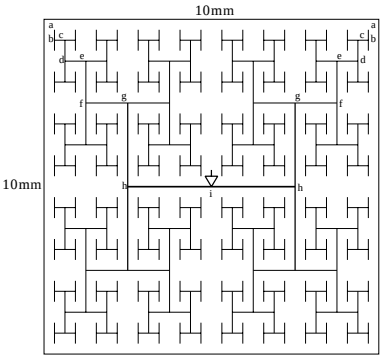


Figure 1. Clock topology of H-tree.

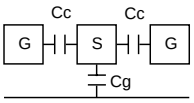
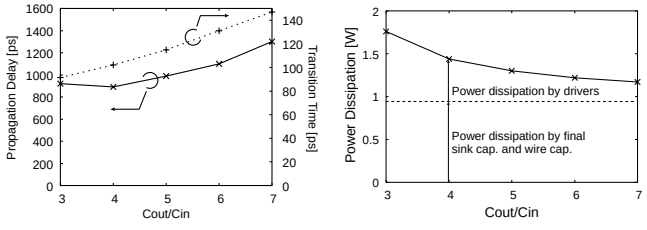


Figure 2. Interconnect structure.

variation due to manufacturing variability, power supply fluctuation and temperature gradient. Generally there are two types of variations; random variation according to a probability density function and a spatial variation. In this paper, we assume the following two variation models.

1. Variables fluctuate randomly according to a normal distribution.
2. Variables change according to a function whose variable is the distance from a position. We can regard the position as a hot spot, i.e. the temperature and the supply voltage change gradually from the position. The manufacturing variability also has a spatial variation[8].

We assume six patterns of spatial variation. Figure 4 shows the contour maps. The center of the concentric circle is different. The spatial variations are expressed as fol-



(a) Delay and transition time. (b) Power dissipation.

Figure 3. Propagation delay, transition time and power dissipation vs. $C_{\rm out}/C_{\rm in}$.

$C_{\rm out}/C_{\rm in}$	a	b	c	d	e	f	g	h	i	total buffer size
3	235	184	145	121	103	112	119	209	278	100,580
4	169	96	55	37	27	39	45	109	145	61,543
5	132	59	27	17	13	24	29	78	100	44,388
6	109	40	15	10	8	18	21	62	76	34,860
7	92	29	10	7	6	14	17	51	61	28,567

The driver size is normalized by a unit inverter (NMOS: L=0.2μm, W=2.6μm, PMOS: L=0.2μm, W=5.5μm).

Table 1. Driver sizes.

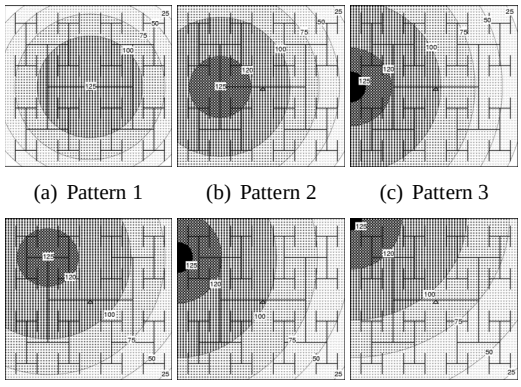
lows.

$$Z(x,y) = \begin{cases} -k_1((x-5)^2+(y-5)^2)+m & (\text{Pattern1}) \\ -k_2((x-2.5)^2+(y-5)^2)+m & (\text{Pattern2}) \\ -k_3(x^2+(y-5)^2)+m & (\text{Pattern3}) \\ -k_4((x-2.5)^2+(y-7.5)^2)+m & (\text{Pattern4}) \\ -k_5(x^2+(y-7.5)^2)+m & (\text{Pattern5}) \\ -k_6(x^2+(y-10)^2)+m & (\text{Pattern6}), \end{cases} \quad (3)$$

where m and $k_1 - k_6$ are coefficients. These coefficients are decided when the maximum and minimum values are given.

The nominal transistor length is 0.200μm. We think that the transistor length variation consists of random and spatial variations[8]. In random variation, we set $\sigma = 0.011\mu$m. In the case of spatial variation, the maximum and minimum values are 0.220 and 0.180μm respectively. Figure 5(a) shows the relation between transistor length and oscillation cycle of a 5-stage ring oscillator. The variation of 0.02μm corresponds to 12% delay change.

The nominal supply voltage is 1.8V. We think that power noise has random and spatial variations. The standard deviation is set to be 0.1V. The maximum and minimum voltages in spatial variation are 1.98 and 1.62V. In this paper, we assume that only voltage of power line fluctuates and voltage of ground line is fixed, because Reference[9] reports that ground noise is smaller than power noise thanks to presence of substrate. The relation between oscillation period and supply voltage is shown in Figure 5(b). The voltage drop of 0.18V causes 9% delay increase.



(a) Pattern 1 (b) Pattern 2 (c) Pattern 3

(d) Pattern 4 (e) Pattern 5 (f) Pattern 6

Figure 4. Spatial variation models.

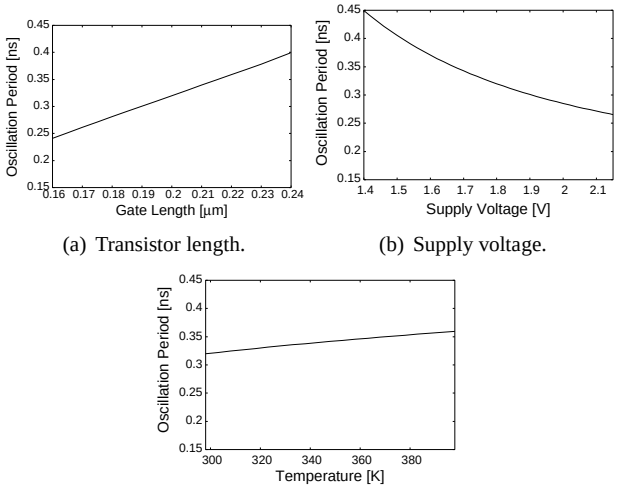
In the case of temperature, we only consider spatial variations, because heat conductivity of silicon substrate is good and temperature changes smoothly inside a chip. We assume that the maximum and minimum temperatures are 90°C and 40°C. Figure 5(c) shows the temperature dependency of MOSFETs. The temperature rise of 50 °C increases delay by 6.3%. The resistance variation of interconnect is expressed as [7]

$$R(T) = R_0[1 + \alpha_T(T - T_0)], \quad (4)$$

where R_0 is the resistance at temperature T_0 and the coefficient α_T of aluminum is 0.004°C^{-1}. Rigidly speaking, α_T is dependent of temperature, but we use the value at 25°C for simplicity. The temperature increase of 50 °C corresponds to 20% increase of wire resistance.

3. Analysis Results

This section shows results of clock skew analysis under the variation models explained in the previous section. We first evaluate clock skew under each variation model.



(a) Transistor length. (b) Supply voltage.

(c) Temperature.

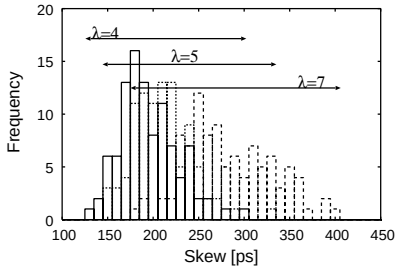
Figure 5. Oscillation cycle vs. transistor length, supply voltage and temperature.

We then apply all models and evaluate clock skew. When we evaluate clock skew under a random variation model, we perform Monte Carlo analysis whose evaluation count is 100.

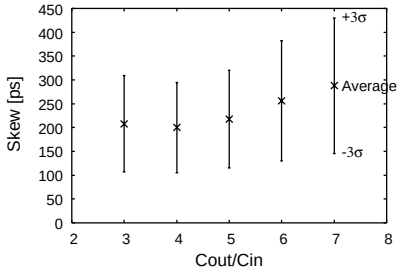
3.1. Skew Analysis under Power Supply Fluctuation

We first evaluate clock skew statistically under the random variation model. Figure 6(a) shows the histograms in the case that $C_{\rm out}/C_{\rm in}$ is 4, 5 and 7. We can see that the distribution moves to the right as $C_{\rm out}/C_{\rm in}$ increases, which means that the clock network becomes sensitive to power supply fluctuation. Figure 6(b) shows the average m and $m \pm 3\sigma$ of clock skew. When λ=3, the average skew is 208ps, whereas it is 288ps when λ=7. Clock tree design with small $C_{\rm out}/C_{\rm in}$ ratio helps to reduce clock skew due to random power supply noise.

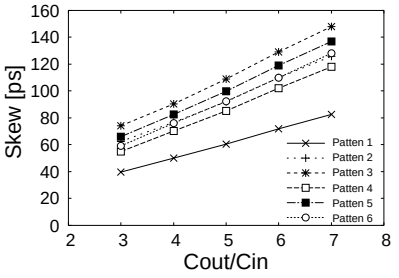
We next evaluate clock skew under spatial power supply fluctuation. Figure 6(c) shows the clock skew under the spatial variation models. In all cases, the clock skew increases as $C_{\rm out}/C_{\rm in}$ becomes large. We can conclude that clock skew due to power supply noise can be reduced by setting small $C_{\rm out}/C_{\rm in}$ value in clock tree design irrespective of random and spatial variation.



(a) Skew histogram (random variation).



(b) Average and best/worst case skew (random variation).

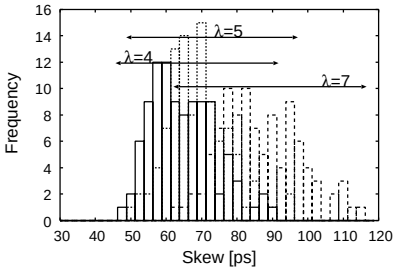


(c) Skew vs.$C_{\rm out}/C_{\rm in}$ (spatial variation).

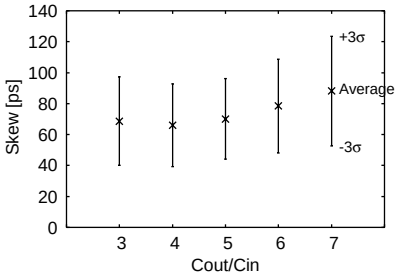
Figure 6. Clock skew under supply voltage fluctuation.

3.2. Skew Analysis under Transistor Length Variation

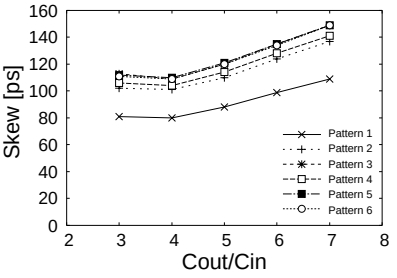
We next evaluate clock skew under transistor length variation. Figure 7(a) is the histogram under the random variation model. Figure 7(b) shows m and $m \pm 3\sigma$. Similar with power supply variation, clock tree with smaller $C_{\rm out}/C_{\rm in}$



(a) Skew histogram (random variation).



(b) Average and best/worst case skew (random variation).



(c) Skew vs.$C_{\rm out}/C_{\rm in}$ (spatial variation).

Figure 7. Clock skew under transistor length fluctuation.

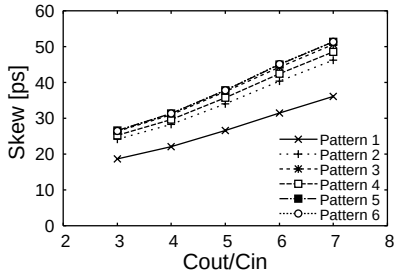
value is more robust. The average skew is 69ps and 88ps when λ is 3 and 7.

Figure 7(c) shows the relation between skew and $C_{\rm out}/C_{\rm in}$ under the spatial transistor length variation. The smaller $C_{\rm out}/C_{\rm in}$ value is preferable to reduce skew.

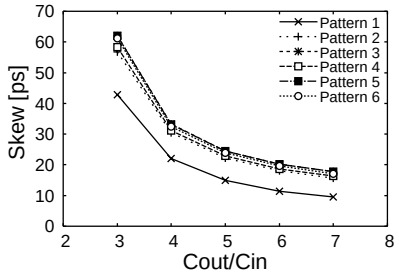
3.3. Skew Analysis under Temperature Variation

Temperature variation affects both MOS transistor characteristics and wire resistance. We first evaluate clock skew caused by MOS transistor and wire resistance separately. We next consider both MOS and wire variation.

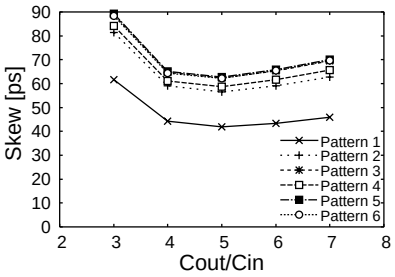
Figure 8(a) shows the relation between skew and $C_{\rm out}/C_{\rm in}$ when only MOS transistors are affected by temperature variation. We can see that the constraint of small $C_{\rm out}/C_{\rm in}$ value contributes to suppress clock skew.



(a) Only MOS is varied.



(b) Only wire is varied.



(c) Both MOS and wire are varied.

Figure 8. Clock skew vs. $C_{\rm out}/C_{\rm in}$ under temperature gradient.

Figure 8(b) shows the skew when only wire resistance is varied by temperature gradient. The relation between clock skew and $C_{\rm out}/C_{\rm in}$ is different from others shown before. As $C_{\rm out}/C_{\rm in}$ is varied from 3 to 7, the skew decreases to one third. In this case, larger $C_{\rm out}/C_{\rm in}$ value decreases clock skew. Let us discuss the reason. 50%-to-50% delay that includes both gate and interconnect delay is expressed as follows[10].

$$T_{50\%} = R_{tr}(0.693C_{int}+0.693C_L) + R_{int}(0.377C_{int}+0.693C_L), \quad (5)$$

where, R_{int}, C_{int} is the total resistance and capacitance of the interconnect. R_{tr} is the output resistance of the driver, and C_L is the load capacitance connected to the end of the interconnect. In the clock design policy explained in Section II, interconnect width and length are fixed, and only driver strength is adjusted according to the given constraint of $C_{\rm out}/C_{\rm in}$. When we choose a small $C_{\rm out}/C_{\rm in}$ value, the driver resistance R_{tr} becomes small. In Eq. (5), the first term becomes relatively small, and the second term becomes the dominant factor of the delay. In this situation, the variation of the interconnect resistance R_{int} affects the delay strongly. Conversely, when $C_{\rm out}/C_{\rm in}$ and R_{tr} are large, the impact of R_{int} variation decreases. We give an example of actual values of R_{tr} and R_{int} used in the clock trees. The wire between g and h and the driver at h in Figure 1 are taken up. The interconnect resistance between g and h is 26.4Ω. The driver resistance is from 5.2Ω ($\lambda = 3$) to 21.6Ω ($\lambda = 7$). As driver resistance becomes small, the impact of wire resistance variation on skew gets stronger.

We next evaluate clock skew considering both MOS and wire variation due to temperature gradient. Figure 8(c) shows the relation between skew and $C_{\rm out}/C_{\rm in}$. We can see that there is an optimal value of $C_{\rm out}/C_{\rm in}$ that minimizes clock skew, since MOS and wire have the opposite tendencies as shown in Figures 8(a) and 8(b). In this case, $C_{\rm out}/C_{\rm in}$=5 is optimal for temperature gradient.

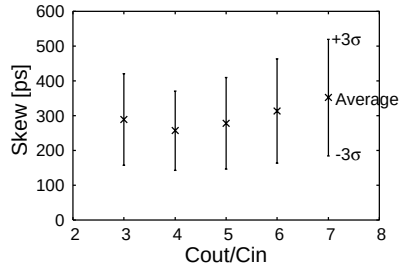
It is well known that temperature affects drain current of a MOS transistor in two mechanisms. One is mobility degradation, and the other is decrease of threshold voltage. These two factors compensate drain current variation, i.e. mobility degradation decreases drain current, whereas decrease of threshold voltage increase drain current. The total variation of drain current depends on supply voltage and threshold voltage of MOS transistors[11, 12]. There are combinations of supply voltage and threshold voltage that make drain current insensitive to temperature[12]. In these situations, Figure 8(b) becomes the actual relationship between clock skew and $C_{\rm out}/C_{\rm in}$ under temperature variation. Reference [13] also indicates that a long interconnect in upper layer suffers from temperature increase due to Joule heating. Global clock distribution usually uses long interconnects in upper layer, and hence temperature may in-

crease clock skew considerably. Thus, the impact of temperature on skew is not monotonic, and it is dependent of $C_{\rm out}/C_{\rm in}$, supply and threshold voltage of MOS transistors.

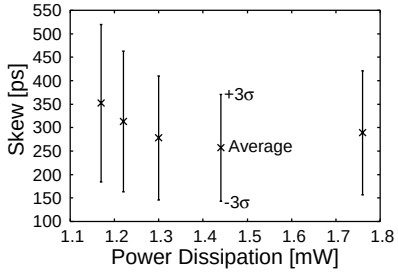
3.4. Overall Skew Analysis

We perform statistical analysis of clock skew taking all variabilities into consideration. Random and spatial power supply variation, random and spatial transistor length variation, and spatial temperature gradient are considered. Temperature gradient is correlated with distribution of power consumption, and hence we assume that temperature gradient and spatial power supply variation have the same spatial variation patterns. We perform 100 evaluations for each combination of spatial transistor length variation and spatial supply voltage (temperature) variation.

Figure 9(a) shows the relationship between clock skew and $C_{\rm out}/C_{\rm in}$. The average clock skew is 257ps to 352ps, and mean+3σ is 371ps to 520ps. We can see that clock skew becomes minimum when $C_{\rm out}/C_{\rm in}$ is 4. This result comes from the fact that the clock skew caused by wire resistance variation due to temperature gradient becomes larger as $C_{\rm out}/C_{\rm in}$ decreases, as shown in the previous section. When we minimize clock skew, the optimal value of $C_{\rm out}/C_{\rm in}$ i.e. transition time constraint, should be selected. Figure 9(b) shows the relationship between clock skew and power dissipation. Large power dissipation does not necessarily reduce clock skew.



(a) Skew vs. $C_{\rm out}/C_{\rm in}$.



(b) Skew vs. power dissipation.

Figure 9. Clock skew under all variations.

4. Conclusion

We evaluate clock skew under manufacturing and environmental variabilities focusing on transition time constraint given to clock tree design. As for transistor length variation and supply voltage fluctuation, a constraint of small transition time helps to increase the robustness of clock tree. However, in the case of temperature gradient, the relationship between transition time constraint and clock skew is not monotonic, and it depends on supply voltage and threshold voltage of MOS transistors. In our experimental analysis using a 0.18μm technology, clock skew is minimized when $C_{\rm out}/C_{\rm in}$ of drivers is set 4.

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