Interconnect Capacitance Extraction for System LCD Circuits

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ABSTRACT

This paper discusses interconnect capacitance extraction for system LCD circuits, where coupling capacitance is much significant since a ground plane locates far away unlike LSI interconnects. We focus on a pattern matching method with interpolation to implement an accurate and efficient capacitance extraction system, and present good implementations that are suitable for system LCD circuits. To reduce computational cost, interconnect structures are spatially divided into several sub-regions considering capacitance coupling range, and analyzed in each sub-region using a capacitance database pre-characterized by a 3-D field solver. This paper evaluates tradeoff curves between characterization cost and extraction accuracy for four division methods in lattice structures that are basic and common structures in LCD driver circuits. Experimental results reveal efficient division methods for accurate capacitance extraction.

Categories and Subject Descriptors: B.7.2 [Integrated Circuits]: Design Aids - *Simulation.*

General Terms: Design.

Keywords: Interconnect capacitance, capacitance extraction, system LCD.

1. INTRODUCTION

Recently, system LCDs (Liquid Crystal Displays) that have additional circuits integrated on a glass panel are widely adopted for mobile terminals[1]. In design of system LCD circuits, insufficient accuracy of capacitance extraction emerges as a serious problem. The inaccuracy comes from the location of a ground plane. In system LCD circuits, a ground plane locates 100∼1000 times farther from interconnects than that in LSI circuits. As the ground plane locates farther, parasitic capacitance between interconnects becomes more dominant. It is hard to extract capacitance accurately by using conventional methods for LSI circuits, because these methods are tailored for on-chip interconnect structures. For precise capacitance extraction, relation between capacitance and ground plane location should be analyzed, and an extraction method suitable for system LCD circuits must be developed. Several capacitance models for basic structures are proposed for the distant ground plane. In Ref. [2], coupling capacitance between two conductors is modeled semi-analytically. However, it is not usable for capacitance extraction in large circuits, because it can cope with only two conductors though several conductors are coupled in practical circuits. A systematic method that can handle lots of interconnects is highly demanded. Numbers of capacitance extraction methods are proposed for LSI circuits. Until deep sub-micron process, 2-D[3] or 2.5D[4] method is mainly used since they run fast and attain sufficient accuracy for simple structures. From deep sub-micron process, interconnect structure becomes more complicated and much accurate extraction is required. Thus, 3D field solver, such as [5], is currently used for capacitance estimation; some methods analyze the entire layout directly[6, 7], and others calculate capacitance based on pre-analyzed capacitance database, where the latter method is called pattern matching method[8]. Key factors of pattern matching that determine performance in accuracy and computational cost are characterized primitive structures and interpolation of pre-characterized database.

In this paper, we first investigate relation between ground plane location and coupling capacitance, and the coupling range that must be considered in capacitance extraction is examined compared with LSI interconnects. We then discuss capacitance extraction methods suitable for system LCD circuits. From the viewpoint of accuracy and ease of implementation, we focus on a pattern matching method with interpolation. To decrease computational cost required for practical large structures, we present four methods that spatially divide interconnect structure into several sub-regions, and evaluate them in lattice structures to clarify the tradeoff between characterization cost and extraction accuracy. Our contributions are 1) to propose spatial division methods for system LCD circuits and 2) to present a systematic procedure to evaluate the tradeoff between cost and accuracy.

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2. CAPACITANCE VS. GROUND LOCATION

This section discusses difficulty of capacitance extraction in system LCD circuits in comparison with LSI circuits, and demonstrates capacitance characteristics of interconnects far from a ground plane.

2.1 Coupling capacitance of parallel wires

In order to discuss the influence of a ground plane, we consider three parallel wires above a ground plane shown in Fig. 1. In LSI circuits, the range of the ground distance is 1 to 10μm and that of system LCD is roughly 1000μm. We first assume that the distance between the ground plane and the wires is set to H=1∼1000μm. Wire width W, wire space S, and wire thickness T are set to 5μm, 5μm, 1μm, respectively. Relative permittivity ε_r is 3.9. Focusing

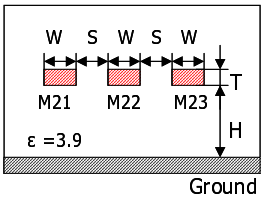

Figure 1: Cross-section of three parallel wires.

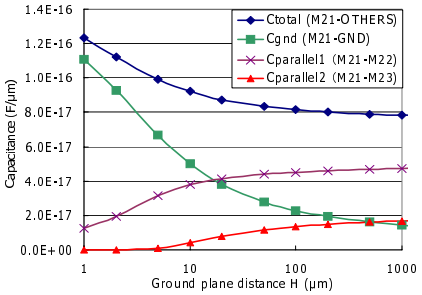

Figure 2: Relation between ground plane location and capacitance.

on the left wire M21, capacitance is computed by a commercial 2D field solver[5]. Figure 2 shows the result. In the distance range of LSI circuits (H=1∼10μm), the dominant capacitance is ground capacitance (M21-GND), and occupies 50 to 90% of the total capacitance. The coupling capacitance between the adjacent wires (M21-M22) takes 10 to 50%, and the coupling capacitance to the wire next to the adjacent wire (M21-M23) is less than 10%. On the other hand, in the distance range of system LCD circuits, the coupling capacitance between adjacent wires (M21-M22) occupies 60% and becomes dominant. The coupling capacitance to the second nearest wire (M21-M23) takes 22% and becomes larger than the ground capacitance (M21-GND) that takes 18%. In design of LSI circuits, a single adjacent wire at each side is enough for coupling capacitance estimation. On the other hand, for system LCDs, at least two wires should be considered for accurate capacitance extraction.

2.2 Coupling capacitance of crossing wires

In order to discuss 3D effects of capacitive coupling, we examine two crossing wires shown in Fig. 3. Reassume that wire length R1 and ground plane distance H are set to 10∼10000μm, and 1, 10, 100, 1000$\}\mu$m, respectively. The wire width, wire length of the upper wire, the thickness and vertical distance of the two wires are set to W=5μm, R2=1000μm, T=1μm, and d=1μm, respectively. The coupling capacitance between the crossing wires is calculated by a 3D field solver[5]. Figure 4 shows the result. In the distance range of LSI (H=1∼10μm), the coupling capacitance remains almost constant, which means that the coupling capacitance arises mainly from a parallel-plate capacitance at the intersection. On the other hand, in the distance range of system LCD circuits (H=1000μm), the coupling capacitance does not converge within 5000μm, because the ground plane locates far way, and then 3D effects of coupling capacitance become prominent.
From these results, in system LCD circuits, the coupling range is much wider than in LSI circuits, and coupling capacitance is more significant. To extract capacitance accurately, we should consider two adjacent wires at each side for parallel wires, and a few millimeter wide range for crossing wires.

3. CAPACITANCE EXTRACTION

This section discusses capacitance extraction methods suitable for system LCD circuits. A preferable capacitance extraction

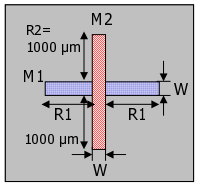

Figure 3: Layout of two crossing wires.

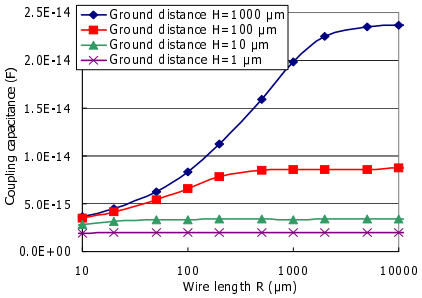

Figure 4: Capacitive coupling range of two crossing wires.

method depends on the specification given for a target design, required accuracy and allowable computational cost. In order to choose a proper capacitance extraction method, tradeoff between characterization cost and extraction accuracy must be studied. This paper focuses on a pattern matching method with interpolation from the viewpoint of accuracy and ease of implementation.

3.1 Pattern matching method

Pattern matching method works in two steps. As a preparation of capacitance extraction, capacitance model database is constructed for primitive structures with typical parameter variations suitable for the target design by using a field solver. The primitive structures and the number of parameter variations are determined by design specification such as process data and desired accuracy. Some tools for LSI interconnects characterize capacitance for all possible variations and provide accurate extraction, but it needs extremely many patterns and high computational cost. In this paper, the number of the variation in each parameter is limited and other variations are calculated by interpolation. In extraction process, the target net is firstly selected, and then the neighboring structure is extracted which includes the neighboring parallel and crossing wires coupled with the target net. Finally, each capacitance of the extracted structure is calculated by the pre-analyzed capacitance database for the pattern matched with the target structure. If a completely matched pattern does not exist, similar patterns are used for calculation.
The determining factor in performance is the primitive structures and interpolation. Each primitive structure must be characterized considering coupling capacitance and electric field, and plenty number of primitive structures must be prepared since lack of a proper primitive structure may causes an unacceptable large error. As for the interpolation, the number of variation in each parameter is the most important and the values of sampling points are also crucial. We must determine them properly considering tradeoff between accuracy and computational cost.

3.2 Spatial division of wire structure

In order to realize efficient pattern matching, we discuss spatial division of a wire structure into primitive structures. The process is to divide a wire structure into several sub-regions considering range of coupling capacitance and symmetry of electric field. Each subregion corresponds to a primitive structure and is analyzed by a 3D field solver. Neumann boundary condition is given for each primitive library to analyze. Capacitance is calculated by summing up

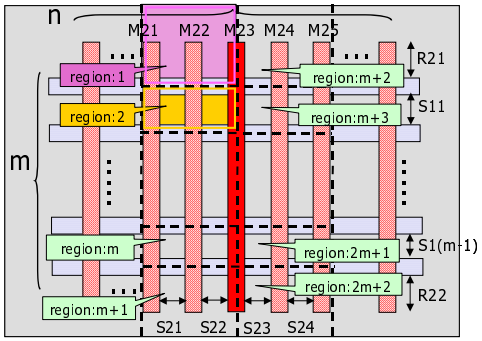

Figure 5: m×n lattice structure (dashed lines correspond to division method (2)).

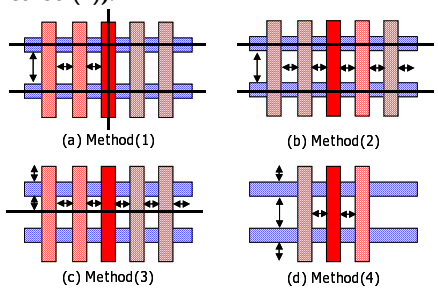

Figure 6: Example of each division method (arrows represent spacing parameters in a sub-region).

the capacitance in each sub-region. In this paper, four spatial division methods are presented. The spatial division causes capacitance estimation error due to mismatch in boundary condition. Therefore spatial division methods heavily affect estimation accuracy. Also the complexity and the number of primitive structures depend on spatial division methods, which means characterization cost varies significantly according to the spatial division methods.

As a target design, we assume LCD driver circuits that are typically implemented in system LCDs. They have two metal layers, and form various lattice structures. Thus, we use m×n lattice structures (Fig. 5) for capacitance extraction. Figure 6 shows an example of each division method for 2×5 lattice structure to help understanding.

Method (1): Divide the region at the center of the observed wire and the crossing wires

As shown in Fig. 5, 6(a), the target structure is divided at the center of the observed wire and the crossing wires. m×n lattice structure is divided into (m+1)×2 sub-regions. Sub-regions are classified into two structures; region1 and region2. In region1, a crossing wire lies on either top or bottom, and capacitance is modeled with parameters R21, S21, S22. In region2, two crossing wires lie on both top and bottom, and capacitance is modeled with S11, S21, S22. This method uses simple primitive structures with at most five conductors specified by just three parameters, which reduces characterization cost. However, it suffers from the low accuracy for asymmetric structures, such as a structure that has dense wires on one side and sparse wires on the other side. The inaccuracy is caused by Neumann boundary condition. Electric field in the divided sub-region sometimes becomes much different from that in the original structure.

Method (2): Divide the region at the center of the crossing wires

To avoid the asymmetry problem, this method divides structures only at the center of the crossing wires(Fig. 6(b)). Compared with Method(1), the number of required parameters is roughly doubled. m×n lattice structure is divided into (m+1) regions, which are classified into two primitive structures and modeled with five parameters. The number of conductors in each structure is seven at most.

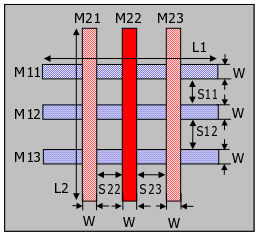

Figure 7: 3×3 lattice structure.

Table 1: Error of division method (%)

division method		focusing on M23 (1)	(2)	(3)	(4)	focusing on M22 (1)	(2)	(3)	(4)
C_{total}	average	-1.2	-0.3	0.1	0.0	2.0	-0.7	0.7	0.0
	σ	0.7	0.3	0.2	0.0	2.9	0.4	0.4	0.2
C_{para}	average	1.3	0.1	0.1	0.0	0.1	0.2	0.1	5.7
	σ	0.5	0.1	0.0	0.0	3.1	0.1	0.0	1.5
C_{cross}	average	-1.4	-1.4	-1.4	0.0	-1.9	-1.1	-1.8	0.3
	σ	0.6	0.6	0.6	0.0	0.8	0.7	0.8	0.1

Method (3): Divide the region at the intermediate point of the crossing wires

This method divides a target structure at the middle of two crossing wires (Fig. 6(c)). Since the electric field between crossing wires is well modeled, higher accuracy is enabled. m×n lattice structure is divided into m sub-regions, which are classified into two structures and modeled with six parameters. The number of conductors in each structure is six.

Method (4): Consider only the adjacent parallel wires

This method considers only the adjacent wires(Fig. 6(d)). Focusing on M23 in Fig. 5, the second nearest wires M21 and M25 are ignored. m×n lattice structure is not divided but we trim the second nearest wires and so forth. The structure is modeled with m+3 parameters, S22, S23, R21, R22, S11, ..., S1(m-1). The number of conductors in the structure is m+3.

4. PERFORMANCE EVALUATION

The proposed division methods are applied to 3×3 lattice structure shown in Fig. 7, and accuracy and computational cost are evaluated.

4.1 Accuracy of division method

Width of each wire is set to W={2, 5, 10}μm. Wire space and wire length are set to S11∼S22 = {5, 50, 1000}μm, and L1, L2 = {50, 200, 1000, 3000}μm, respectively. Excluding the redundant combinations, 432 patterns in total are simulated using a 3D field solver. Accuracy of each division method is evaluated by the following equation

$$error = \frac{C(\text{original}) - \Sigma C(\text{division})}{C_{total}(\text{original})} \times 100\ [\%], \qquad (1)$$

where C_{total} is the total capacitance of the observed wire, C(original) represents each capacitance component calculated without division, and ΣC(division) means the summation of capacitance calculated in divided sub-regions. Simulation results are shown in Tables 1. Average and standard deviation(σ) of estimation error are listed for total capacitance, parallel coupling capacitance and cross coupling capacitance.

4.2 Accuracy of interpolation

The accuracy of interpolation for capacitance computation in a primitive structure depends on the interpolation expression, the

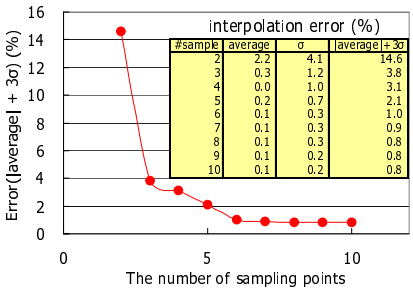

Figure 8: Relation between # sampling and accuracy.

Table 2: Performance comparison of each method.

division method	CPU time(sec.)*	#structure	#param.
(1)	5.8	2	3
(2)	17.2	2	5
(3)	14.0	2	6
(4)	95.9	1	6
no-division	193.3	1	8

*CPU: Ultra SPARCIII 900MHz, Memory: 5GB

number of sampling points and the choice of sampling points. For simplicity, we utilize the relation between accuracy and number of sampling points in simple two crossing wires. Of all the possible combinations in sampling points, the most accurate combination that minimizes |average| + 3σ is computed and used for accuracy evaluation. The results are shown in Fig. 8. As the number of sampling points increase, error caused by the interpolation is reduced; 14.6% with two sampling points, 3.8% with three sampling points and less than 1% with six points.

4.3 Total performance of capacitance extraction

Since the division method and interpolation in a primitive structure is independent, total error is denoted as

$$average(\text{total}) = average(\text{div.}) + average(\text{interp.}), \quad (2)$$

$$\sigma(\text{total}) = \sqrt{\sigma^2(\text{div.}) + \sigma^2(\text{interp.})}. \quad (3)$$

Table 2 shows the cost of each division method required for characterization. CPU time is simulation time for a single divided subregion using a 3D field solver, and #structure is the number of primitive structures required for capacitance database, and #param is the number of parameters for each primitive structure such as spacing or wire length. Total computational cost for generating capacitance database COST is defined by the following equation.

$$COST = T_{CPU} \times N_{model} \times \prod_{i=1}^{N_{parameter}} N_{sample}, \quad (4)$$

where T_{CPU} is CPU time for a primitive structure, N_{model} is the number of primitive structures, $N_{parameter}$ is the number of parameters which should be varied, and N_{sample} is the number of sampling points.

Figure 9 shows the relation between cost and accuracy for C_{total}, $C_{parallel}$, C_{cross}. The horizontal axis is the computational cost calculated by Eqn. (4) (logarithmic scale). The vertical axis is the |average| + 3σ of extraction error. From these figures, the most appropriate method for required performance is determined. If 25% error is acceptable for total capacitance, method(1) is the most cost effective, which takes only 90sec., while no-division takes 50000sec.($\simeq$14 hours). If 10% error is required for parallel coupling capacitance, method(4) is unusable because it causes more than 16% error. For cross coupling capacitance, all methods do not cause above 15% error. If 10% error is required for each capacitance, method(2) is suitable, and it takes 8400 sec.

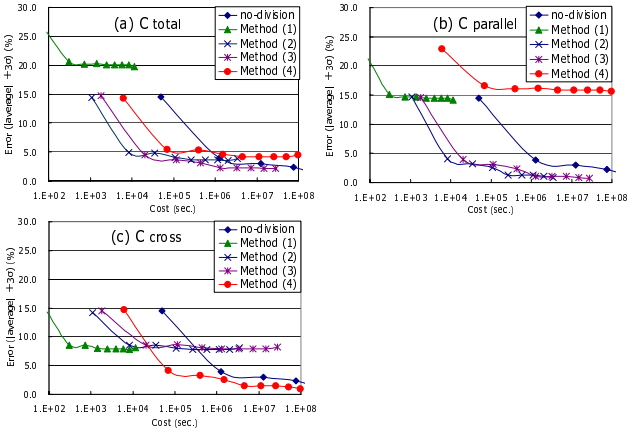

Figure 9: Relation between accuracy and computational cost.

As the number of conductors becomes larger, the computational cost of no-division and method(4) increases drastically, while that of other division methods remain constant. The CPU time increases in proportion to the number of wires cubed. In addition, the error caused by the asymmetry is reduced for large structures. Thus, the division methods presented in this paper become more efficient for large structures.

5. CONCLUSIONS

This paper discusses interconnect capacitance extraction suitable for system LCD circuits. By analyzing the relation between ground plane location and capacitance, the spatial size of each primitive structure is examined to estimate coupling capacitance accurately. To reduce simulation time and size of database for pattern matching method, four spatial division methods are presented and evaluated. Considering the capacitive coupling range and symmetry of electric field, computational cost is reduced with reasonable accuracy. We evaluate the accuracy and the computational cost for 3×3 lattice structure, and tradeoff between accuracy and cost of each capacitance extraction is clarified. Future work includes evaluation and enhancement to cope with irregular structures.

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