Substrate Loss of On-chip Transmission-lines with Power/Ground Wires in Lower Layer

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Abstract

This paper discusses shielding effect of power/ground wires in lower layer. A conducting substrate affects characteristics of on-chip transmission line. However in many cases on actual chips, there are P/G wires between the signal wire and the substrate that may shield the substrate coupling. We show measurement and simulation results of on-chip transmission-lines with narrow yet many power/ground wires in a lower layer. Experimental results show that narrow power/ground wires in a lower layer in parallel to the signal wire, which are common in LSI power distribution network, shield substrate coupling and suppress substrate loss. On the other hand, orthogonal power/ground wires in a lower layer hardly mitigate substrate coupling.

Introduction

As improving LSI performance, on-chip interconnect is one of the most significant factors which limit chip performance. To break through the interconnect bottleneck problem, several signaling methods are discussed [1–4]. In such high-performance design, accurate modeling of on-chip transmission-lines is needed. Modeling error may cause crucial problems such as impedance mismatch and estimation error in attenuation. A conducting substrate is one of difficulties in modeling on-chip interconnects. The effect of silicon substrate and its modeling are discussed so far [5–8]. Substrate coupling in a co-planar interconnect structure on resistive substrate has been studied. However in real chips, there are other power/ground wires and signal wires between the transmission-line and the substrate. Reference [9] reports that interconnects in lower layers affect the inductance of the transmission-line. The interconnects in lower layers are expected to shield the coupling to the substrate. However the interconnects in lower layers have various dimension, direction and wire density. Therefore it is not clear which wires in lower layers shield substrate coupling.

This paper reports the measurement results of transmission-lines with narrow ground wires in lower layer which represent P/G wires in standard cell. Experimental results show the effect of substrate loss depends on the structure of wires in lower layer. If the direction of ground wires in lower layer are orthogonal to the signal wire, these orthogonal wires have no shielding effect and substrate loss is significant. On the other hand, if the ground wires in lower layer are parallel, substrate loss is suppressed. From comparison with 3D field solver, substrate loss is negligible when parallel ground wires exist in lower layer. We reveal that considering parallel P/G wires in lower layer is important and substrate loss is not significant if parallel P/G wires exist between transmission-lines and the substrate. The contribution of this work is to show which wires in lower layer affect substrate coupling.

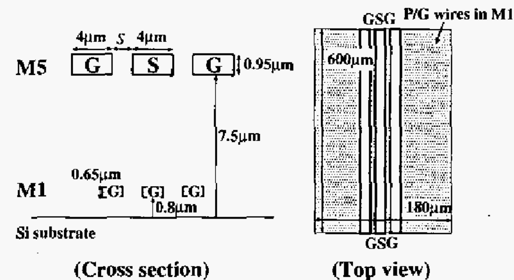

Figure 1: Cross section and top view of test structure.

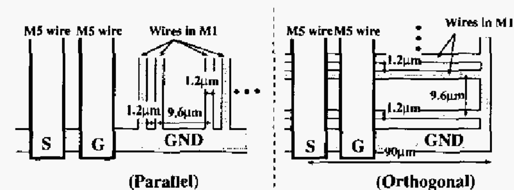

Figure 2: Structure of ground wires in M1 (top view).

Test structure

This section describes the test structure. The cross section and the top view of the test structure are shown in Fig. 1. In the top layer (M5), three wires construct G-S-G co-planar structure. Each line width is $4\mu m$ and the spacing between signal and ground is $S = 2\mu m$ or $S = 19\mu m$. The length of co-planar line is $600\mu m$. In the lowest layer (M1), we align grounded wires that represent power/ground wire in standard cell. M1 wires are located uniformly in the area of $180\mu m \times 600\mu m$, as shown in Fig. 1. Figure 2 shows the detailed structure of M1 wires. The structure of M1 wires is divided into parallel and orthogonal main branches. In "parallel" structure, M1 ground wires are parallel to the co-planar wires in M5. "Orthogonal" has M1 wires that are orthogonal to the co-planar wires. The wire width of M1 wires is $1.2\mu m$, and the spacing is $1.2\mu m$ and $9.6\mu m$. We decide the dimension of M1 wires assuming a $0.18\mu m$ standard cell library. All M1 wires are connected to each other at the end of wires, and connected to the ground pad. For comparison, test structures with a ground plane in M1 layer and test structures without M1 wires are also evaluated.

Figure 3 shows a micrograph of a test structure. We evaluate the interconnect characteristics by using a network analyzer.

Measurement results

Here we show the measurement results. Figure 4 shows the self-resistance of the test structure whose spacing S is $2\mu m$. The curve labeled "plate" is the result that the ground plane is placed in M1 layer, and "w/o M1" is that result that no ground wires in M1. The measurement results are shown in lines with

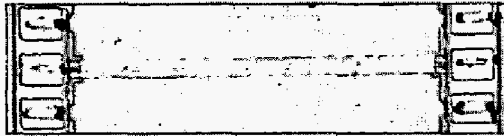

Figure 3: Micrograph of a test structure (without M1 wires).

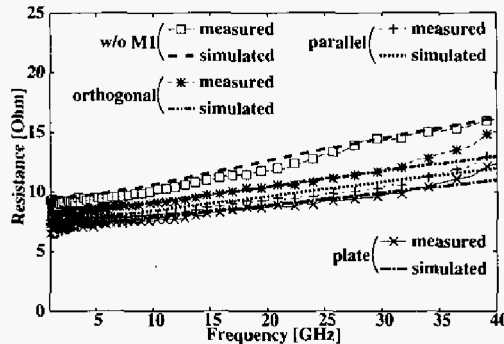

Figure 4: Self-resistance (spacing $S = 2\mu$m).

points. The dotted lines labeled "simulated" mean the result of 3D field-solver [10] without considering substrate conductivity (substrate conductivity is set to 0). If the measurement result (labeled "measured") agrees with the simulation result, the substrate effect is not significant. From Fig. 4, the measured results are close to the simulation results. This means that substrate effect is not significant where the spacing S is 2μm.

Figure 5 shows the resistance where the spacing S is 19μm. In the results of "w/o M1" and "orthogonal", the simulation result underestimates the self-resistance by about 30%. This is because the simulation result ignores the substrate effect. On the other hand, the simulation results agree with the measured results in the case of "parallel" and "plate". Parallel M1 wires behave as current return path and shields magnetic coupling between the signal wire and the substrate. Therefore if parallel ground wires or a ground plane exists in the lower layer, substrate effect on interconnect characteristics is negligible.

From above discussion, parallel ground wires in M1 layer prevent the substrate coupling even if the signal-ground spacing is 19μm. On the other hand, orthogonal wires cannot shield substrate coupling. If there are P/G wires in lower layer and they are parallel to the signal wire, substrate loss is not significant and considering the wires in lower layer is important for accurate modeling even though P/G wires are narrow.

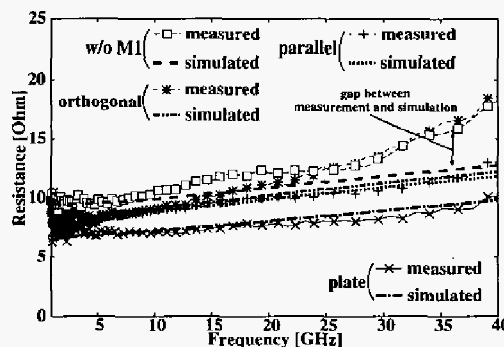

Figure 5: Self-resistance (spacing $S = 19\mu$m).

Conclusions

Substrate coupling and the ground wires in lower layer are discussed. From measurement results, shielding effect of the ground wires in lower layer depends on the direction of wires. The ground wires that are parallel to the signal wire prevent the magnetic coupling and suppress the substrate loss. When ground wires in lower layer are orthogonal to the signal wire, the self-resistance is almost the same as the result of the interconnect without M1 wires. Therefore the substrate loss is negligible if dense power/ground grid such as P/G for standard cells exists in the lower layer.

Acknowledgments

This work is supported in part by the 21st Century COE Program (Grant No. 14213201).

References

[1] I. B. Dhaou, M. Ismail, and H. Tenhunen, "Current Mode, Low-power, On-chip Signaling in Deep-submicron CMOS Technology," *IEEE Trans. CAS I*, vol.50, no.3, pp.397–406, Mar 2003.

[2] M. Hashimoto, A. Tsuchiya, and H. Onodera, "On-chip Global Signaling by Wave Pipelining," *Proc. EPEP*, pp.311–314, Oct 2004.

[3] P. Wang, G. Pei, and E. C. C. Kan, "Pulsed Wave Interconnect," *IEEE Trans. VLSI*, vol.12, no.5, pp.453–463, May 2004.

[4] H. Ito, J. Inoue, S. Gomi, H. Sugita, K. Okada, and K. Masu, "On-chip Transmission Line for Long Global Interconnects," *Proc. IEDM*, pp.677–680, Dec 2004.

[5] A. Weisshaar, H. Lan, and A. Luoh, "Accurate Closed-form Expressions for the Frequency-dependent Line Parameters of On-chip Interconnects on Lossy Silicon Substrate," *IEEE Trans. AP*, vol.25, no.2, pp.288–296, May 2002.

[6] M. F. Ktata, H. Grabinski, G. Gaus, and H. Fischer, "When are Substrate Effects Important for On-chip Interconnects?," *Proc. EPEP*, pp.265–268, 2003.

[7] J. Zheng, Y.C. Hahm, A. Weisshaar, and V. K. Tripathi, "Equivalent Circuit Modeling of Single and Coupled On-chip Interconnects on Lossy Silicon Substrate," *Proc. EPEP*, pp.185 –188, 1999.

[8] J. Mao, M. Swaminathan, J. Libous, and D. O'Connor, "Effect of Substrate Resistivity on Switching Noise in On-chip Power Distribution Networks," *Proc. EPEP*, pp.33–36, 2003.

[9] B. Kleveland, X. Qi, L. Madden, T. Furusawa, R. W. Dutton, M. A. Horowitz, and S. S. Wong, "High-frequency Characterization of On-chip Digital Interconnects," *IEEE JSSC*, vol.37, pp.716–725, Jun 2002.

[10] Ansoft Corp., HFSS Manual, 2001.