PAPER Special Section on VLSI Design and CAD Algorithms

Interconnect RL Extraction Based on Transfer Characteristics of Transmission-Line

Akira TSUCHIYA[†a)], **Masanori HASHIMOTO**[††b)], ***and*** **Hidetoshi ONODERA**[†c)], ***Members***

SUMMARY This paper proposes a method to determine a single frequency for interconnect RL extraction. Resistance and inductance of interconnects depend on frequency, and hence the extraction frequency strongly affects the modeling accuracy of interconnects. The proposed method determines an extraction frequency based on the transfer characteristic of interconnects. By choosing the frequency where the transfer characteristic becomes maximum, the extracted RL values achieve the accurate modeling of the waveform. Experimental results show that the proposed method provides accurate transition waveforms over various interconnect topologies.

key words: *parameter extraction, transmission-line, frequency dependence*

1. Introduction

According to advancements in LSI fabrication technology, performance of LSI chips is predicted to improve continuously [1]. As improving the chip performance, on-chip interconnects become important and accurate modeling of interconnects is crucial for circuit design. One difficulty of interconnect modeling is frequency dependency of the characteristics. Resistance and inductance depend on frequency because of skin- and proximity-effect [2], return current distribution [3] and the effect of lossy substrate [4]. In recent multilevel interconnects, the frequency-dependence is becoming more and more serious because adjacent and underlying interconnects increase frequency-dependence of the interconnect characteristics. In digital circuits, pulse waveforms are commonly used. The frequency spectrum of pulse waveforms widely spreads from DC to frequency several times as high as clock frequency. To model the behavior of interconnects precisely, designers have to take the frequency characteristics into consideration. To treat frequency dependent interconnects, several modeling methods are proposed [5]–[7]. These frequency-dependent models improve simulation accuracy and are suitable in the case that the best accuracy is required, for example sigh-off simulation. However, in circuit design, the conventional frequency-independent model has an advantage that there are a number of techniques and methods developed so far. Especially in the early stage of circuit design, quick modeling and evaluation are important and the accuracy of sign-off simulation is not necessary. Circuit design techniques of interconnects, such as analytical performance estimation, circuit reduction, buffer insertion and timing analysis, have been widely studied [2], [8]–[10]. Most of these techniques assume that interconnects can be modeled as a frequency-independent RLC ladder circuit. However, how to cope with frequency-dependency in modeling interconnects as a RLC ladder has not been studied enough, though its modeling accuracy affects design quality. Therefore developing an accurate modeling technique by frequency-independent model is indispensable for designing high-performance circuits, and hence this work focuses on RL extraction at a single frequency.

In this paper, an extraction frequency based on the transfer characteristic of interconnects is proposed. It is commonly adopted to determine the extraction frequency from the shape of an input signal waveform, especially from the rise time, focusing on the spectrum of the input signal [2]. This is natural and reasonable to analyze the incident waveform at the near-end (driver output) of the interconnects. On the other hand, the main interest is the analysis of the waveform at the far-end (receiver input). As signals are propagating through an interconnect, high-frequency components easily attenuate. The dominant frequency components that determine the far-end waveform are different from those for the near-end waveform. Experimental results imply that the transfer characteristic of interconnects is playing an important role in the waveforms at the far-end of interconnects. From this observation, this paper focus on the transfer characteristic of interconnects and select the frequency where the transfer characteristic becomes maximum as the frequency to use for interconnect RL extraction. A preliminary work is presented in Ref. [11] and Ref. [11] reports that the extraction frequency based on the transfer characteristics is suitable for interconnect modeling. However, the frequency determination method in Ref. [11] is not practical because it can treat only open-ended uniform transmission-lines without branches. If the interconnect is branching or nonuniform, the transfer characteristic of each segment is different. The proposed method in this paper gives a respective extraction frequency to every segment of an interconnect instead of enforcing a single extraction frequency on the entire interconnect. The proposed method systematically determines the extraction frequencies successively from the sinks to the source by replac-

Manuscript received March 14, 2006.
Manuscript revised June 13, 2006.
Final manuscript received August 7, 2006.

[†]The authors are with the Department of Communications and Computer Engineering, Kyoto University, Kyoto-shi, 606-8501 Japan.
[††]The author is with the Department of Information Systems Engineering, Osaka University, Suita-shi, 565-0871 Japan.
a) E-mail: tsuchiya@vlsi.kuee.kyoto-u.ac.jp
b) E-mail: hasimoto@ist.osaka-u.ac.jp
c) E-mail: onodera@vlsi.kuee.kyoto-u.ac.jp

DOI: 10.1093/ietfec/e89–a.12.3585

ing the downstream interconnect with the equivalent load impedance. Experimental results show that the equivalent circuit of interconnects extracted at the proposed frequency can achieve the most accurate waveform modeling compared with the conventional extraction frequencies. From experimental results, the maximum errors are below 10% in signal propagation delay and signal transition time. The contribution of this paper is that the proposed method provides a method to determine an extraction frequency and improves the modeling accuracy of frequency-independent models.

In Sect. 2, the problems in interconnect modeling are described. Section 3 explains the detail of the proposed method. Then experimental results are shown in Sect. 4. Section 5 concludes the discussion.

2. Problem Description

This section describes the problem discussed in this paper. First, the frequency-dependence of interconnect characteristics is shown. Next a conventional extraction frequency is explained. Then the impact on transient analysis is demonstrated.

2.1 Frequency-Dependence of Interconnect Characteristics

Frequency-dependence of interconnect characteristics is mainly caused by skin- and proximity-effect, return current distribution and the effect of lossy substrate. The characteristics variation is strongly related with the interconnect structure as well as the frequency. Skin- and proximity-effects are remarkable on wide and thick interconnects because skin depth becomes comparable to the interconnect size in relatively lower frequency. Return current distribution and lossy substrate also affect the characteristic of interconnects. However return current distribution and the effect of lossy substrate strongly depends on the condition of the neighboring interconnects. For simplicity, this paper does not consider the return current distribution and the effect of lossy substrate.

To demonstrate the frequency dependence of the interconnect characteristics, we evaluated an interconnect structure shown in Fig. 1. The interconnect in Fig. 1 assumes a co-planar transmission-line in the top metal layer. The structure and materials of Fig. 1 are based on a 130 nm process. The material of the metal wire is copper (resistivity is $2.2\,\mu\Omega$·cm). The thickness of wires T is $1\,\mu$m and the distance from the substrate is $10\,\mu$m. The relative dielectric constant of the substrate is 11.9, and that of the ILD (Interlayer dielectric) is 4.0. The conductivity of Si substrate is zero.

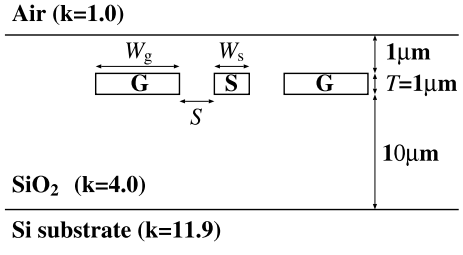

Fig. 1 Cross section of the interconnect structure under study.

We evaluate the interconnect characteristics by a field-solver [12]. The width of the signal wire W_s is $4\,\mu$m, the width of the ground wires W_g is $10\,\mu$m, and the spacing between wires S is $2\,\mu$m. Figure 2 shows the result. In this case, the resistance increases by 38% from DC to 10 GHz, and the inductance decreases by 14% from DC to 10 GHz. The resistance and the inductance start changing at relatively low frequency of 1 to 2 GHz, and thus frequency-dependence is not negligible to model interconnects in current high-performance circuits any longer.

2.2 Conventional Extraction Frequencies

In digital circuits, a trapezoidal pulse that contains multiple frequency components is a common waveform. To model long interconnects that have transmission-line characteristics, an RLC ladder circuit as Fig. 3 is used. This ladder model cannot consider the frequency-dependence of interconnect RL values. In order to derive frequency-independent model of Fig. 3, a single extraction frequency has to be chosen.

There are several representative frequencies of periodic pulse waveform. One of them is significant frequency [2]. The significant frequency f_{sig} is expressed by signal transition time t_r and defined such that the signal energy from DC to f_{sig} becomes 85% of all signal energy. In the range $7 \le T_w/t_r \le 13$ where T_w is the pulse width, f_{sig} is given by $0.34/t_r$ [2]. On the other hand, DC is often used for

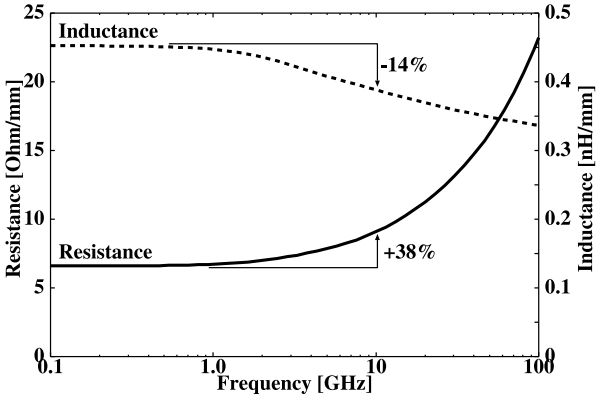

Fig. 2 Frequency-dependence of resistance and inductance. (co-planar structure, signal line width $W_s = 4\,\mu$m, ground line width $W_g = 10\,\mu$m, spacing $S = 2\,\mu$m)

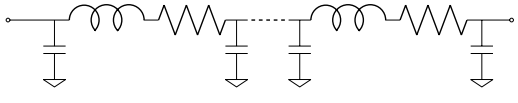

Fig. 3 RLC ladder circuit model.

extraction. Reference [13] concludes that the extraction at DC is accurate enough to estimate signal propagation delay and overshoot/undershoot. DC extraction is acceptable when frequency-dependence is weak, e.g. for narrow interconnects or in low frequency. However as shown in the next section, interconnect modeling at these frequencies causes error in evaluating the propagation waveform.

2.3 Interconnect Models and Their Impact on Waveform

Generally, interconnects in VLSIs are expressed by lumped RLC for circuit design. As explained in the previous section, the frequency-independent RLC ladder circuit in Fig. 3 is used to model on-chip interconnects. A number of frequency-dependent models are proposed [5]–[7]. In this paper, the model of Ref. [7] is used as a golden frequency-dependent model. It is implemented in HSPICE [14] as w-element model. Although frequency-dependent models such as Ref. [7] can provide accurate waveforms, the frequency-dependent model does not tell the designers which frequency component is important in circuit design. Conversely, if it is known which frequency component dominantly forms and affects the waveforms at the far-end, it is not necessary to use the frequency-dependent model. However the frequency spectrum spreads widely and depends on circuit behavior and interconnect characteristics, and hence it is difficult to specify the most representative frequency from the frequency spectrum. The goal of this research is to determine the representative frequency for modeling interconnects at a single frequency.

Figure 4 shows the impact of frequency-dependence on transient analysis. The simulated circuit is shown in Fig. 4. The interconnect shown in Fig. 2 is driven by a voltage source and a resistor R_d that correspond to a CMOS driver whose output impedance is 150 Ω. The solid line labeled "FD" shows the voltage waveform at the far-end by the frequency-dependent model. In this paper, the label "FD" is used as the abbreviation of "Frequency-Dependent model." The dashed lines labeled "DC" and "f_{sig}" are the results of frequency-independent models shown in Fig. 3.

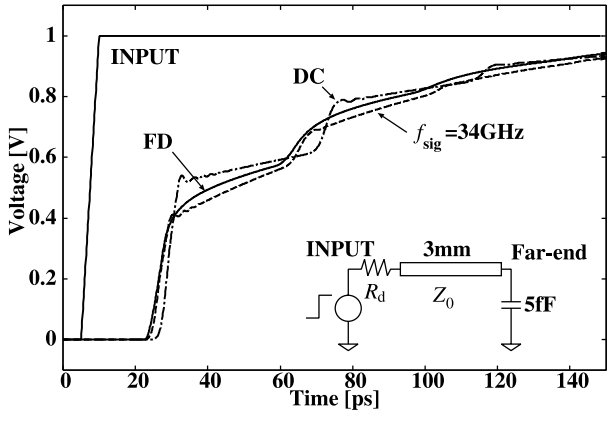

Fig. 4 The impact of frequency-dependence on transition waveform. (interconnect structure is shown in Fig. 2, R_d = 150 Ω)

"DC" means the RLC ladder model extracted at DC, and "f_{sig}" corresponds to RLC extraction at the significant frequency. The number of ladder is 51. As you see, both waveforms of the conventional frequency-independent models ("DC" and "f_{sig}") are far from that of frequency-dependent model ("FD"). We evaluate the modeling accuracy in the signal propagation time and the signal transition time. The signal propagation delay means the time interval from 50% of the input transition to 50% of the output transition. The signal transition time means the time required to change the output voltage between the 20% and 80% of the supply voltage. In the signal propagation delay time and the signal transition time, the errors of "DC" are −28% in delay and −13% in transition time. The errors of "f_{sig}" are 19% in delay and 10% in transition time. When R and L are extracted at DC, the extracted resistance is too low, and, the resistance extracted at significant frequency is too high. From the above observations, it is expected that a certain frequency between DC and significant frequency provides the waveform that is close to the waveform of the frequency-dependent model. If the representative frequency can be determined systematically, the modeling accuracy of the frequency-independent model can be improved by using the representative frequency as the extraction frequency. In the following section, the way to determine the representative frequency to model interconnects at a single frequency is discussed.

3. A Method to Determine an Extraction Frequency

This section proposes a method to determine the representative frequency for interconnect RL extraction. The proposed method determines the extraction frequency focusing on the transfer characteristic of interconnects. First the transfer characteristic of transmission-lines is explained. Then the detail of the proposed method is described.

3.1 Transfer Characteristic of Transmission-Lines

The basic idea of our method is to choose the frequency where the transfer characteristic becomes maximum. The nature of the transfer characteristic of interconnects can be derived from transmission-line theory. For simplicity, an uniform transmission-line shown in Fig. 5 is discussed. The characteristic impedance is Z_0, the propagation constant is γ, the length of the transmission-line is l and the velocity of electromagnetic wave is v. The velocity v is equal to $c/\sqrt{\varepsilon_r}$, where c is the velocity of light in vacuum and ε_r is the relative dielectric constant of insulator. The load impedance Z_t

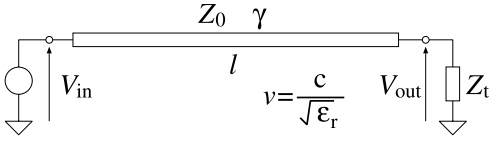

Fig. 5 Transmission-line with impedance load.

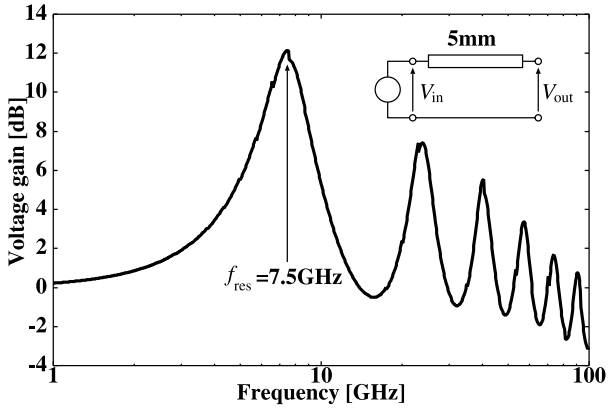

Fig. 6 Transfer characteristic of a transmission-line with 5 mm long.

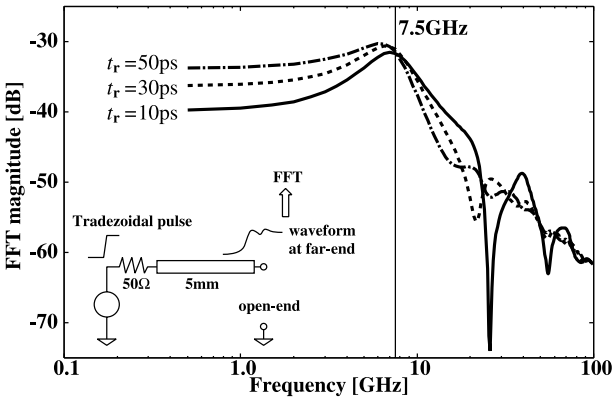

Fig. 7 Frequency spectrum of waveform at the far-end.

is connected to the far-end of transmission-lines. The voltage V_{in} and V_{out} mean the voltage at the near-end and that at the far-end respectively.

According to transmission-line theory, the voltage and the current at the position x is expressed as [15]

$$\begin{cases} V(x) = V(0)\cosh\gamma x - Z_0 I(0)\sinh\gamma x \\ I(x) = -\frac{V(0)}{Z_0}\sinh\gamma x + I(0)\cosh\gamma x. \end{cases} \quad (1)$$

The position $x = 0$ is the input side, and the position $x = l$ is the output of the transmission-line. Since the output of the transmission-line is terminated by the impedance Z_t, the boundary condition is expressed as

$$V(l) = Z_t I(l). \quad (2)$$

From Eqs. (1) and (2), the voltage transfer characteristic V_{out}/V_{in} is expressed as

$$\frac{V_{out}}{V_{in}} = \frac{V(l)}{V(0)} = \frac{1}{\cosh\gamma l + \frac{Z_0}{Z_t}\sinh\gamma l}, \quad (3)$$
$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)},$$

where R, L, G, and C are the resistance, the inductance, the shunt-conductance, and the capacitance per unit length of the transmission-line respectively. Figure 6 shows an example of the transfer characteristic of an open-ended transmission-line. The transmission-line shown in Fig. 1 with $W_s = 4\,\mu$m, $W_g = 10\,\mu$m, and $S = 2\,\mu$m. The frequency characteristics are extracted by a 2D field solver and the interconnect is modeled by the frequency-dependent model [7]. When the transmission-line is open-ended, the transfer characteristic V_{out}/V_{in} becomes maximum where the quarter wavelength $\lambda/4$ is equal to the line length l. This nature is used for quarter wavelength transmission-line resonators. In this case, the resonance frequency f_{res} where V_{out}/V_{in} becomes maximum is $v/4l = 1.5 \times 10^8/(4 \times 5 \times 10^{-3}) = 7.5$ GHz.

This transfer characteristic affects the waveform at the far-end of transmission-lines. The frequency components near the resonance frequency tend to appear at the far-end. On the other hand, the frequency components near the antiresonance frequency hardly affect the waveform at the far-end. Therefore the frequency spectrum at the far-end depends on the input pulse and the transfer characteristic of the interconnect. If the frequency spectrum of the input pulse spreads over the resonance frequency, the frequency components around the resonance frequency are expected to affect the waveform at the far-end. If the resonance frequency is higher than the significant frequency, the frequency components around the resonance frequency are small because almost all of the frequency components concentrate in the range from DC to the significant frequency.

Figure 7 shows the frequency spectrum of the waveform at the far-end in the case that trapezoidal pulses with various transition time t_r are injected to the near-end of the interconnect shown in Fig. 6. The transition time t_r is varied from 10 ps to 50 ps, and hence the significant frequency changes from 34 GHz to 6.8 GHz. The resonance frequency is 7.5 GHz. In this case, the significant frequency is nearly equal to or higher than the resonance frequency. The frequency spectrum has a unique peak at the resonance frequency even if the signal transition time t_r is changed. This result indicates the frequency component at the resonance frequency is an important factor which determines the waveform at the far-end of the interconnect. Reference [11] reports that the resonance frequency is suitable for the extraction frequency of open-ended uniform transmission-lines without branches. However, on-chip interconnects is not uniform and have branches. If the interconnect is branching, the transfer characteristic from the driver to one receiver is not the same as that from the driver to the other receiver. Therefore the method in Ref. [11] is not applicable to branching wire directly.

3.2 Flow of the Proposed Method

This section proposes a method to determine the extraction frequency based on the transfer characteristic. Figure 8 is the conceptual diagram of the proposed method. Interconnects are divided into segments at the branch points or discontinuous points and considered as a tree such that the root

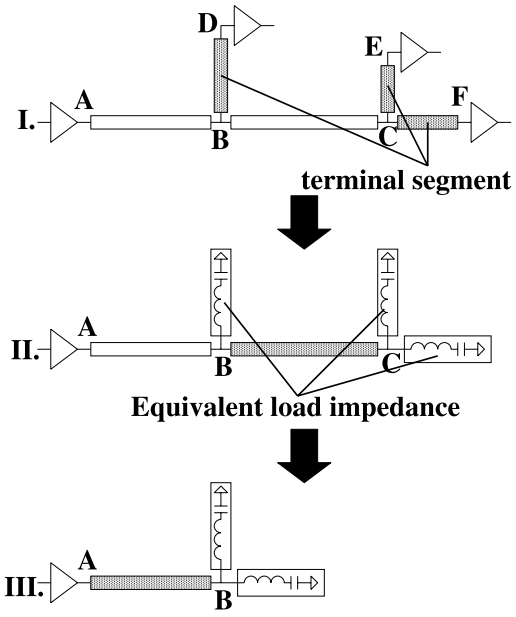

Fig. 8 Conceptual diagram of the proposed method.

node is the output of the driver and the input of the receiver is the leaf node. The proposed method determines the extraction frequencies for each segment from leaf to root by replacing the downstream branches with the equivalent load impedances.

Assumptions of the Proposed Method

The proposed method determines the extraction frequency from the topology of interconnects and the length of each segment. The velocity of electromagnetic wave v is assumed to be known and a constant value. In LSIs, this assumption is valid because the velocity v depends on the relative dielectric constant ε_r and it is constant in the same fabrication process. The significant frequency f_{sig} is also assumed to be known. As described in following step, the significant frequency is used as the upper limit of the extraction frequency. Additionally, the characteristic impedances of each segment are assumed to have the same value. Strictly speaking, this assumption is not correct. However in LSIs, the characteristic impedance of on-chip interconnects does not vary drastically even if the interconnect structure changes. The typical value of co-planar structures is from 50 Ω to 100 Ω. The following section experimentally verifies that these assumptions are reasonable.

Step 1. Determine the Extraction Frequency for Terminal Segments

If the length of the segment and the load impedance are known, the frequency f_{res} at which the transfer characteristic of the segment becomes maximum can be determined from Eq. (3). The resonance frequency f_{res} depends on the length of the segment and the load impedance. Generally, as short the segment is, the extraction frequency becomes higher. The frequency f_{res} can be too high frequency to use as an extraction frequency. If the frequency component of the input is too small at the frequency, extracting at the frequency at which the transfer characteristic becomes maximum is meaningless. Therefore an upper limit of the extraction frequency should be used. As mentioned so far, the significant frequency f_{sig} is defined as the frequency that the 85% of all the energy is included from DC to f_{sig}. In the case that the resonance frequency is higher than significant frequency, the frequency components around the resonance frequency are small and hardly affect the waveform at the far-end. It is reasonable to use the significant frequency as the upper limit of the extraction frequency. Extraction frequency $f_{proposed}$ is expressed as

$$f_{proposed} = \min\left(f_{res}, f_{sig}\right). \tag{4}$$

Reference [11] reports the case of open-ended uniform transmission-lines. In CMOS circuits, the input capacitance of the gates is small and the segments connected to the receiver are assumed as an open-ended transmission-line. The extraction frequencies of these open-ended branches are the frequency where the quarter wavelength is equal to the interconnect length. When the length of a segment is l, the resonance frequency f_{res} is $v/4l$. The method in Ref. [11] is not applicable to interconnects which have a large capacitive load or a resistive termination because Ref. [11] assumes open-ended transmission-lines. By using Eq. (3), the proposed method can be applied to the interconnects that cannot be regarded as open-ended transmission-lines.

Step 2. Replacing Terminal Segments with Equivalent Load Impedances

At step 1, the extraction frequencies of terminal segments are decided. To decide the extraction frequencies of the preceding segments, the segments whose extraction frequency is already decided are replaced with equivalent load impedances. This step corresponds to Fig. 8. II. By replacing with the equivalent load impedance, the extraction frequency can be calculated by Eq. (3). For example, in Fig. 8, the extraction frequency for the segment B-C by replacing the segment C-E and C-F are determined by using the equivalent load impedances.

The load impedance of a certain segment is the input impedance of the downstream branches. For example, the load impedance of the segment B-C in Fig. 8 is the input impedance of the segment C-E and the segment C-F. As shown in Fig. 8. II, the input impedance of transmission-lines can be modeled by a RLC series resonator circuit whose resonance frequency is equal to f_{res}. The resistance is ignored because the proposed method needs only the resonance frequency. The input impedance of a certain segment is expressed as

$$Z_{in} \simeq \frac{Z_0}{\mathrm{j}\tan\left(\frac{\omega l'}{v}\right)} \tag{5}$$

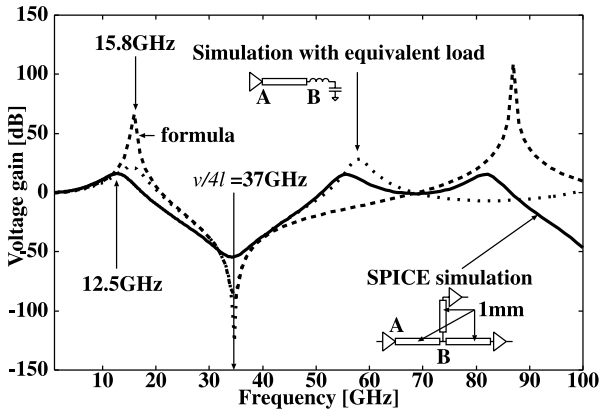

Fig. 9 Voltage gain estimated by the equivalent load impedance.

where l' is equivalent length defined as $l' = v/4f_{\mathrm{res}}$. The derivation of Eq. (5) is described in Appendix. The characteristic impedances Z_0 of each segment are assumed to be the same. Therefore the value of the inductance L and the capacitance C are determined from the characteristic impedance Z_0 and the resonance frequency f_{res}. This means that once the resonance frequency f_{res} is calculated, the equivalent load impedance is uniquely determined.

Figure 9 shows an example of transfer characteristic estimated by Eq. (3) and the equivalent load impedance defined by Eq. (5). Figure 9 is the voltage gain between node A and node B. The interconnect topology is a branching wire as shown in Fig. 9. The solid line is the transfer characteristic by SPICE AC analysis. The dashed line labeled "Simulation with equivalent load" is the result of SPICE simulation using the equivalent load, and the dashed line labeled "formula" is that by Eq. (3) with the equivalent load impedance. The resonance frequency f_{open} when the segment A-B is assumed as open-ended is 37.5 GHz. As shown in Fig. 9, the transfer characteristic estimated by Eq. (3) with equivalent load impedance is valid to estimate the peak of the transfer characteristic. On the other hand, the frequency f_{open} becomes antiresonance frequency on the segment A-B and the transfer characteristic at f_{open} becomes minimum. This result shows that the load impedance has to be considered to estimate the first peak frequencies of the transfer characteristic. From the above discussion, the transfer characteristic can be estimated by Eq. (3) with equivalent load impedance by Eq. (5).

By replacing the terminal segments with equivalent load impedance, the terminal segments are eliminated and other segments become terminal segments. We can return to step 1 and determine the extraction frequency for new terminal segments. The proposed method determines extraction frequencies for each segment by iterating the step 1 and step 2.

4. Experimental Results

This section demonstrates experimental results. The experimental results of two major interconnect topology, H-tree and stub-bus are shown. Then the statistics of experimental results in various situations are shown.

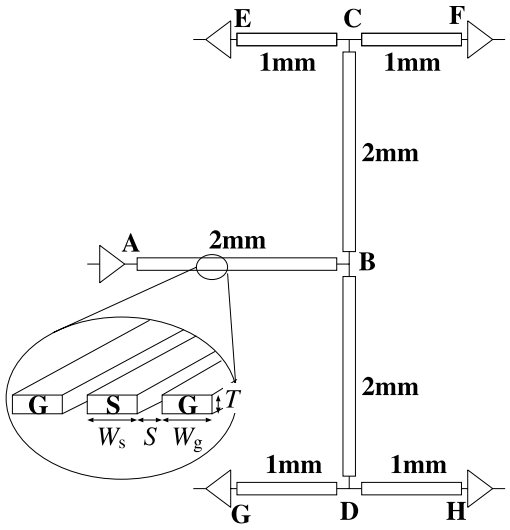

Fig. 10 H-tree topology.

4.1 H-Tree Topology

First the result of H-tree is shown. Figure 10 shows the topology of the H-tree. As shown in Fig. 10, the cross section of interconnects are co-planar structure. The detail of the structure is shown in Fig. 1. The segments A-B, B-C and B-D have the same structure that signal wire width W_{s} is $10\,\mu$m, ground wire width W_{g} is $4\,\mu$m, spacing between wires S is $2\,\mu$m and the thickness of wire T is $1\,\mu$m. The other segments, C-E, C-F, D-G and D-H, have the structure that $W_{\mathrm{s}} = 4\,\mu$m, $W_{\mathrm{g}} = 4\,\mu$m, $S = 2\,\mu$m and $T = 1\,\mu$m. The input transition time t_{r} is set to 10 ps and the output impedance of the driver is set to $50\,\Omega$.

The frequency determination process is shown step by step. First, the segments C-E, C-F, D-G and D-H are connected to the receiver. Thus these segments are assumed as open-ended and the resonance frequency $f_{\mathrm{res}} = v/4l = 37.5$ GHz. However the significant frequency f_{sig} is calculated to $0.34/(10 \times 10^{-12}) = 34$ GHz. Therefore the extraction frequency of these segments is 34 GHz. From Eq. (5) and the extraction frequency 34 GHz, the equivalent load impedance is expressed as

$$\frac{Z_0}{\mathrm{j}\tan\left(\frac{\omega l'_{\mathrm{CE}}}{v}\right)}. \tag{6}$$

Since the segment C-E is open-ended, the equivalent length l'_{CE} is equal to the actual length (1 mm). For the segments B-C and B-D, the voltage gain is expressed as

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{1}{\cos\left(\omega l_{\mathrm{BC}}/v\right) - 2\tan\left(\omega l'_{\mathrm{CE}}/v\right)\sin\left(\omega l_{\mathrm{BC}}/v\right)}, \tag{7}$$

where l_{BC} is 2 mm. From above expression, the extraction frequency for the segments B-C and B-D is calculated to

Table 1 Extracted characteristics of segment A-B in H-tree.

Ext. frEq.	R [Ω]	L [nH]	C [pF]	Z_0 [Ω]
DC	4.95	0.371	0.126	54.3
Proposed (3.9 GHz)	5.65	0.357	0.126	53.1
f_{sig} (34 GHz)	10.83	0.309	0.126	49.5

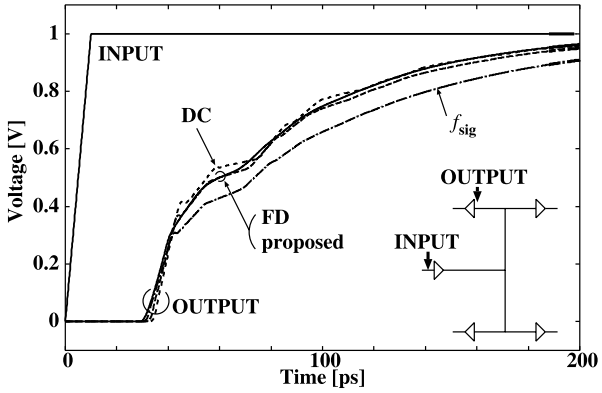

Fig. 11 Waveform at the node E of H-tree.

Table 2 Errors in the delay time and the transition time on H-tree (node E).

Extraction	delay		transition time	
Frequency	[ps]	error [%]	[ps]	error [%]
FD	54.9	—	76.3	—
DC	50.0	−8.9	73.2	−4.1
Proposed	54.7	−0.4	79.6	4.3
f_{sig}	68.6	24.9	108.7	42.4

10 GHz. In a similar way, the extraction frequency for the segment A-B is 3.9 GHz.

Table 1 shows the extracted RLC and characteristics impedance of segment A-B. As the extraction frequency becomes higher, the resistance increases and the inductance decreases. The resistance extracted at the significant frequency is 2.2 times larger than that of DC. The inductance extracted at the significant frequency is about 83% of the inductance at DC. The difference in the characteristic impedance between the significant frequency and DC is about 9%. Figure 11 shows the waveform at the node E. The RLC ladder model extracted at DC and the proposed frequency is almost the same as the result of frequency-dependent model. When the ladder extracted at f_{sig} is used, the waveform differs from that of the frequency-dependent model. The extraction at the f_{sig} estimates the resistance too large, so the attenuation on the interconnect is overestimated. Table 2 shows the signal propagation delay time and the transition time at the node E. The error is calculated by assuming that the result of FD is reference data. The ladder extracted at f_{sig} causes large error, 25% in delay and 42% in transition time. The extraction at DC also causes about 9% error in delay. The ladder extracted at the proposed frequency provides the most accurate modeling.

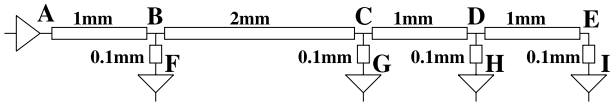

Fig. 12 Stub-bus topology.

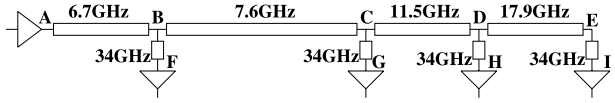

Fig. 13 Extraction frequencies by the proposed method.

Table 3 Extracted characteristics of segment A-B in the stub-bus.

Ext. frEq.	R [Ω]	L [nH]	C [pF]	Z_0 [Ω]
DC	3.33	0.380	0.133	53.5
Proposed (6.7 GHz)	5.15	0.326	0.133	49.6
f_{sig} (34 GHz)	9.21	0.291	0.133	46.8

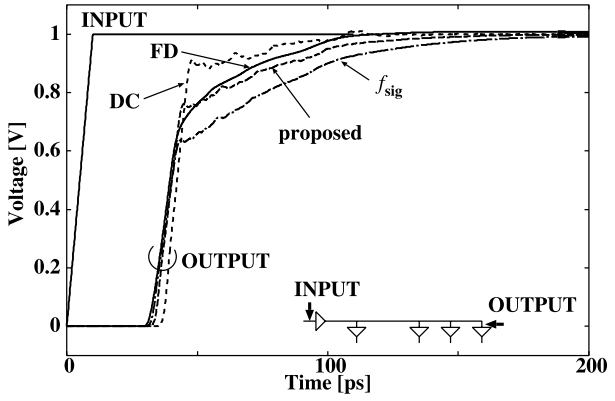

Fig. 14 Waveform at the node I of stub-bus.

4.2 Stub-Bus Topology

Here the experimental result of stub-bus structure is shown. Figure 12 shows the interconnect topology. The bus line A-B-C-D-E is a fat wire that the signal width $W_s = 10\,\mu$m, the ground width $W_g = 10\,\mu$m and the spacing $S = 2\,\mu$m. The stubs are short and thin wires, that $W_s = 1\,\mu$m, $W_g = 1\,\mu$m and $S = 2\,\mu$m. The driver output impedance is 50 Ω and the transition time of input is 10 ps.

The extraction frequencies by the proposed method are determined as shown in Fig. 13. The extraction frequency of the stubs is $f_{sig} = 34$ GHz because the stub is short and its resonance frequency is 375 GHz.

Table 3 shows the extracted RLC and characteristics impedance of segment A-B. The resistance extracted at the significant frequency is 2.8 times larger than that of DC. The inductance extracted at the significant frequency is about 77% of the inductance at DC. The difference in the characteristic impedance between the significant frequency and DC is about 13%. Figure 14 shows the waveform at the node I and Table 4 shows the errors in delay and transition time. The ladder model extracted at DC or significant frequency

Table 4 Errors in the delay time and the transition time on stub-bus (node I).

Extraction	delay		transition time	
Frequency	[ps]	error [%]	[ps]	error [%]
FD	34.5	—	19.5	—
DC	37.3	8.1	6.8	−65.4
Proposed	35.3	2.3	21.2	8.7
f_{sig}	35.3	2.3	40.6	108.2

Table 5 Statistical summary of overall experiments.

Extraction	delay		transition time	
Frequency	Max. error	$> 5\%^*$	Max. error	$> 5\%^*$
DC	−88.1 %	11.5 %	−71.9 %	27.8 %
proposed	−9.9 %	5.4 %	−9.8 %	12.5 %
f_{sig}	110.0 %	12.2 %	160.3 %	35.2 %

($*$: The ratio of the experiments that the error is over 5%.)

causes serious error especially in signal transition time. As shown in Fig. 14, DC extraction underestimates the attenuation and f_{sig} overestimates. DC extraction also causes 8% error in delay because the extraction at DC causes estimation error in phase velocity. On the other hand, the RLC ladder by the proposed method provides accurate modeling of frequency-dependent interconnect.

4.3 Results of Overall Experiments

The proposed method is evaluated under various conditions for verification. This section shows the statistical summary of all experiments. The topology of net, lengths of each segment, interconnect structure, driver size and transition time of input are changed. The number of segments in one net is varied from 1 to 5. As mentioned in Sect. 3.2, the proposed extraction frequency becomes the same as the significant frequency f_{sig} when the wire is short. We selectively evaluate the region where the proposed frequency is different from the significant frequency. Thus the length of segments is 200 μm, 500 μm, 1 mm, 2 mm, 3 mm, 4 mm or 5 mm. In this experiments, the main cause of frequency-dependence is the skin- and proximity-effect. If the wire is narrow, the skin- and proximity-effect is not significant and the frequency-dependence is negligible. We evaluate a coplanar structure and the wire width is set to relatively large values. The signal width W_s and ground width are 1 μm, 4 μm or 10 μm and the spacing S is 2 μm, 4 μm or 8 μm. The output impedance of the driver is changed from 25 Ω, 50 Ω, 75 Ω or 100 Ω. The transition time of input pulse is changed from 10 ps, 30 ps, or 100 ps. By changing those parameters, 9,545 patterns of net and the waveforms at 43,199 nodes are evaluated in total.

Table 5 shows the summary of overall experiments. Table 5 contains the maximum error in delay time and transition time (rows of "Max. error"), and the ratio of nodes where the error is over 5% (rows of "> 5%"). The ladder extracted at DC tends to underestimate the delay and transition time, and the ladder extracted at significant frequency f_{sig} overestimates. In the case of the ladder extracted at DC, the error in delay exceeds 5% at the 12% of all nodes and the maximum error is −88.1%. In transition time, the error at 28% of nodes exceeds 5% and the maximum error is −71.9%. In the case of significant frequency, the error in delay at about 12% of all nodes is over 5% and the maximum is 110.0%, and the error in transition time at about 35% of all nodes is over 5% and the maximum is over 160%. Those errors are serious problem for evaluating the circuit behavior, such as timing analysis. On the other hand, the proposed method achieves the error less than 10% in both delay and transition time. The results above confirm the RLC ladder extracted at the proposed frequency provides accurate modeling of frequency-dependent interconnects.

5. Conclusion

The frequency that should be used to extract RL values is discussed. When frequency-independent equivalent circuits are used for circuit design, the extraction frequency must be carefully determined to maximize the fidelity in interconnect characteristics. This paper proposes an RL extraction scheme that uses the frequency determined by interconnect length. The proposed method is experimentally verified that the proposed method achieves the most accurate estimation in signal propagation delay and transition time. The maximum error is within 10% in delay and in transition time in our experiments. With the proposed representative frequency, we can determine a suitable extraction frequency and improve the modeling accuracy of frequency-independent models. The proposed method is useful especially in the early stage of circuit design. The proposed method also helps the interconnect design because the proposed method indicates which frequency is important for signal propagation.

Acknowledgement

This work is supported in part by the 21st Century COE Program (Grant No. 14213201).

References

[1] Semiconductor Industry Association, International Technology Roadmap for Semiconductors 2003 Edition, 2003.
[2] C.K. Cheng, J. Lillis, S. Lin, and N.H. Chang, Interconnect Analysis and Synthesis, Wiley-Interscience, 2000.
[3] S.Y. Kim, Y. Massoud, and S.S. Wong, "On the accuracy of return path assumption for loop inductance extraction for 0.1 μm technology and beyond," Proc. ISQED, pp.401–404, 2003.
[4] M.F. Ktata, H. Grabinski, G. Gaus, and H. Fischer, "When are substrate effects important for on-chip interconnects?," Proc. IEEE Topical Meeting on Electrical Performance of Electronic Packaging, pp.265–268, Oct. 2003.
[5] H.A. Wheeler, "Formulas for the skin-effect," Proc. Institute of Radio Engineers, vol.30, pp.412–424, Sept. 1942.
[6] B. Krauter and S. Mehrotra, "Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis," Proc. ACM/IEEE Design Automation Conference, pp.303–308, 1998.
[7] D.B. Kuznetsov and J.E. Schutt-Ainé, "Optimal transient simulation of transmission lines," IEEE Trans. Circuits Syst., vol.43, no.2,

pp.110–121, Feb. 1996.
[8] J.A. Davis and J.D. Meindl, "Compact distributed RLC interconnect models—Part I: Single line transient, time delay, and overshoot expressions," IEEE Trans. Electron Devices, vol.47, no.11, pp.2068–2077, Nov. 2000.
[9] H.B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley, 1990.
[10] Y.I. Ismail and E.G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in vlsi circuits," Proc. ACM/IEEE Design Automation Conference, pp.721–724, 1999.
[11] A. Tsuchiya, M. Hashimoto, and H. Onodera, "Representative frequency for interconnect R(f)L(f)C extraction," IEICE Trans. Fundamentals, vol.E86-A, no.12, pp.2942–2951, Dec. 2003.
[12] Avant! Corporation, Raphael Reference Manual, Release 4.2, May 1998.
[13] Y. Cao, X. Huang, D. Sylvester, T.J. King, and C. Hu, "Impact of on-chip interconnect frequency-dependent r(f)l(f) on digital design," Proc. International ASIC/SOC Conference, pp.438–442, Sept. 2002.
[14] Synopsys Inc., HSPICE Manual, 2003.
[15] W.C. Johnson, Transmission Lines and Networks, McGraw-Hill, 1988.

Appendix: Derivation of Eq. (5)

At the resonance frequency, the transmission-line can be expressed by a series resonator shown in Fig. A· 1.

The input impedance of the equivalent circuit $Z_{\text{in, equiv}}$ is expressed as

$$Z_{\text{in, equiv}} = \sqrt{\frac{L'}{C'}}\frac{1-\omega^2 L'C'}{\mathrm{j}\omega\sqrt{L'C'}}, \qquad (\text{A}\cdot 1)$$

where $L' = 2Ll'/\pi$, $C' = 2Cl'/\pi$ and $l' = v/4f_{\text{res}}$. Since the characteristic impedance Z_0 is equal to $\sqrt{L/C}$ and the velocity of electromagnetic wave v is expressed as $v = 1/\sqrt{LC}$, Eq. (A· 1) is rewritten as

$$Z_{\text{in, equiv}} = Z_0\frac{1-\left(\frac{\omega l'}{v}/\frac{\pi}{2}\right)^2}{\mathrm{j}\left(\frac{\omega l'}{v}/\frac{\pi}{2}\right)} \simeq \frac{Z_0}{\mathrm{j}\tan\left(\frac{\omega l'}{v}\right)}. \qquad (\text{A}\cdot 2)$$

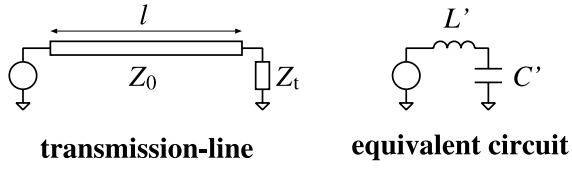

Fig. A· 1 Equivalent series resonator of a transmission-line.

Akira Tsuchiya received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 2001, 2003, and 2005, respectively. Since 2005, he was an Instructor in Department of Communications and Computer Engineering, Kyoto University. His research interest includes modeling and design of on-chip high-performance interconnects. He is a member of IEEE and IPSJ.

Masanori Hashimoto received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Since 2001, he was an Instructor in Department of Communications and Computer Engineering, Kyoto University. Since 2004, he has been an Associate Professor in Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University. His research interest includes computer-aided-design for digital integrated circuits, and high-speed circuit design. He is a member of IEEE, ACM and IPSJ.

Hidetoshi Onodera received the B.E., M.E., and Dr. Eng. degrees in Electronic Engineering from Kyoto University, Kyoto, Japan, in 1978, 1980, 1984, respectively. Since 1983 he has been an Instructor (1983–1991), an Associate Professor (1992–1998), a Professor (1999–) in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University. His research interests include computer-aided-design for integrated circuits, and analog and mixed analog-digital circuits design. He is a member of the IPSJ, ACM and IEEE.