

Quasi Event-Wise Measurement and Simulation of Neutron-Induced Multiple-Cell Upsets in 22- and 55-nm SRAMs

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Abstract—We experimentally investigated neutron-induced multiple-cell upsets (MCUs) in 22- and 55-nm bulk planar static random access memories (SRAMs) using self-scan circuits that detect bit flips at intervals of several hundred nanoseconds. This method accurately detects single event upsets (SEUs), including Distant MCUs generated by nuclear reactions, which are defined as MCUs with bit flips separated by more than one cell pitch. We quantitatively demonstrate that conventional static bitmap-based analysis faces an inherent trade-off between excluding Pseudo MCUs, in which multiple independent SEUs are erroneously grouped into a single event, and capturing Distant MCUs, making accurate event identification difficult. Our irradiation results show that 13.0% of the 516 MCU events were Distant MCUs for 22 nm at 0.7 V. Maximum MCU cluster sizes reached 7.0 μm for 22 nm and 15 μm for 55 nm at 0.7 V, with Pseudo MCU probability ratios on the order of 10^{-11} . This ratio represents the relative likelihood of multiple SEUs occurring during a full SRAM readout compared to the cases of only a single SEU occurring under a Poisson process. We also found that the bitmap-based method requires a small grouping distance for accurate SEU counts, preventing Distant MCU characterization. Particle and heavy ion transport code system (PHITS)-based simulations and particle-level analysis identified that approximately 78% of the observed Distant MCUs are attributed to alpha particles.

Index Terms—Dynamic tests, multiple-cell upset (MCU), neutrons, single event upset (SEU), soft errors, static random access memory (SRAM).

I. INTRODUCTION

SOFT errors refer to temporary failures occurring when radiation strikes electronic devices, representing an ongoing threat to system reliability. In particular, single event upsets (SEUs) in static random access memory (SRAM) are a primary concern. When terrestrial neutrons strike the silicon die, they induce nuclear reactions that generate charge-depositing

secondary particles, flipping memory bits and causing computational malfunctions.

SEUs are classified into single bit upsets (SBUs) and multiple-cell upsets (MCUs). While MCUs, which are commonly classified according to the Chebyshev distance between upset cells, are widely recognized as a key reliability metric because they can defeat error correction codes (ECCs) [1], and they are also fundamentally important as a physical signature of the neutron reaction. This significance is most pronounced in Distant MCUs, where a Distant MCU is defined as simultaneous upsets in physically separated cells caused by a single incident particle [2], [3]. These events are direct manifestations of one or more high-energy secondary charged particles generated by neutron-induced nuclear interactions, such as spallation and inelastic/elastic scattering, traversing multiple cells within the substrate. Therefore, accurately capturing Distant MCUs is essential not only for reliability assessment but also for validating the physics of secondary particle transport in Monte Carlo simulations.

Neutron irradiation tests on SRAMs have been conducted using both static and dynamic measurement methods. In static methods, a fixed data pattern is written to the memory prior to irradiation, and the memory contents are read out after exposure, such that upset events are identified through post-irradiation comparison. As illustrated in Fig. 1(a), Pseudo MCUs are independent SEUs accumulated over time that are erroneously grouped as a single MCU event. In static analysis, identifying MCUs relies solely on spatial proximity, which creates an inherent dilemma: expanding the grouping area to capture the long tracks of Distant MCUs inevitably inflates the Pseudo MCU count, obscuring the true physical phenomena. Conversely, restricting the grouping area filters out Pseudo MCUs but fails to capture the full spatial impact of secondary particles generated by the nuclear reaction. This trade-off means that static methods cannot strictly distinguish between a single physical event (Distant MCU) and multiple independent strikes (Pseudo MCU), limiting their utility for rigorous physical validation.

In contrast, dynamic methods continuously perform read-only or read-write operations during irradiation, enabling time-resolved detection of upset events and reducing the probability of Pseudo MCUs. From the perspective of measurement circuitry, autonomous error-capture circuits have long been

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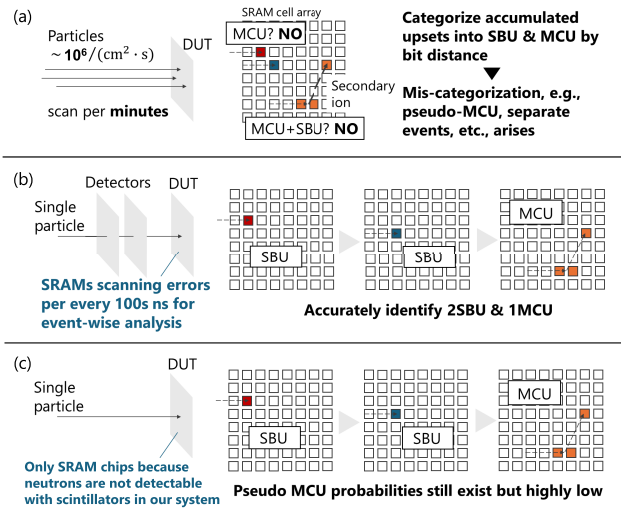


Fig. 1. (a) Conventional static measurement method, (b) event-wise dynamic measurement method proposed in [10] for charged particles, and (c) proposed quasi event-wise dynamic measurement method using quick self-scan SRAMs without detectors. The proposed method enables more accurate identification of SBU and MCU events than the traditional upset accumulation and bitmap-based approach. In this work, since neutrons are not charged particles, the quasi event-wise dynamic method (c) is introduced and employed. Pseudo MCUs may occur, but their probability is negligible compared with true MCU events (quantified in Section IV-A).

studied in the context of radiation effects, particularly for dynamic measurement methods. Representative examples include built-in self-test (BIST) circuits for single-event effects, such as the Cosmic Ray Effects on Semiconductor Technology (CREST) framework [4], which was originally developed to detect and classify radiation-induced errors in flip-flop-based logic circuits [5], [6]. Consistent with the CREST framework, the SRAM-based approaches in [7], [8], and [9] employ autonomous on-chip test schemes, in which repetitive memory access operations with local control logic are executed during irradiation to enable in situ detection and classification of upset events. Although dynamic measurement methods are inherently capable of capturing Distant MCUs, only a limited number of prior studies have explicitly focused on their detailed analysis, as discussed in Section II.

In this work, following the circuit-level approach exemplified by the CREST framework, we address this limitation by introducing a quasi event-wise dynamic measurement framework that autonomously captures SEUs during neutron irradiation. By implementing a dedicated on-chip scanning circuit with sub-microsecond readout intervals for 22- and 55-nm planar SRAMs [10], the proposed design enables in situ, event-resolved acquisition of SEU data, yielding a ground-truth dataset with negligible Pseudo MCU probability. Using this dataset, we first quantitatively evaluate the accuracy limits of conventional static bitmap methods, revealing the magnitude of measurement error introduced by the aforementioned trade-off. Second, we provide a detailed analysis of Distant MCUs, identifying cluster sizes significantly larger than typically assumed. Finally, we validate simulations based on the Particle and Heavy Ion Transport Code System (PHITS) [11], against this experimental ground truth while accounting for parasitic bipolar action (PBA), and utilize the simulation to identify

the specific secondary particles responsible for the observed Distant MCUs.

The rest of this article is organized as follows. Section II reviews prior MCU studies under irradiation, categorized into static and dynamic measurement methods. Section III describes the experimental setup and the quasi event-wise methodology. Section IV presents the experimental results, providing the detailed analysis of Distant MCUs and the quantitative critique of the conventional static bitmap-based method. Section V provides simulation results to validate the experimental findings and discuss the secondary particle effects. Finally, concluding remarks are provided in Section VI.

II. RELATED WORK

Neutron irradiation studies on SRAMs have traditionally relied on static measurement methods. Experimental studies in [12] demonstrated the supply-voltage dependence of SEUs in 90-nm SRAMs and technology-scaling trends from 250 to 90 nm. In [13], neutron-induced SEUs in a 90-nm SRAM were investigated using both conventional static testing and March-algorithm-based dynamic testing. The static measurements revealed three MCU events with a Chebyshev distance of two, whereas the dynamic test observed a large cluster of upsets due to micro-latchup and single event functional interrupt (SEFI). A comprehensive static MCU analysis of a COTS 90-nm SRAM over a wide supply-voltage range from 0.5 to 3.3 V was presented in [14], where map-based MCU patterns revealed five small-scale Distant MCU events, consisting of four cases with a Chebyshev distance of two and one case with a distance of four. The influence of supply voltage on MCU occurrence in 65-nm SRAMs was investigated in [15], although the discussion focused on MCU multiplicity rather than spatially distant patterns. Detailed analyses of bit-flip and MCU patterns in 65 nm SRAMs were performed in [16], where the similarity between neutron- and muon-induced MCUs was quantitatively evaluated and detailed map-based MCU patterns were presented. Map-based MCU pattern analyses were also reported for 65-nm SRAMs in [17], demonstrating a significant increase in MCU occurrence compared with 90-nm technology; however, no Distant MCUs were observed. In [18], SEUs in a 28-nm SRAM-based FPGA were analyzed using static methods; although the authors did not explicitly identify any Distant MCUs and suggested that the observed multi-bit upsets could be attributed to Pseudo MCUs, one MCU pattern with a Chebyshev distance of two was nevertheless reported. A detailed MCU study on a 20-nm SRAM was presented in [19], including map-based analyses that revealed strong angle and data-pattern dependencies; notably, seven Distant MCUs with a Chebyshev distance of two were observed. More recently, Narasimham et al. [20] reported SEU technology scaling in advanced 16-, 7-, and 5-nm SRAMs, showing that the fraction of MCUs relative to single-bit upsets increases with device scaling. Overall, among these prior works, Distant MCUs were explicitly identified only in a limited number of static-method studies, whereas their physical signatures are often obscured by Pseudo MCUs inherent to static measurement methodologies.

In contrast to static approaches, dynamic measurement methods have also been employed on both planar and FinFET SRAMs [21], [22], [23], [24], covering planar technologies at 65 and 45 nm as well as FinFET-based technologies at 22 and 14 nm. These studies adopted sufficiently short readout intervals to suppress the occurrence of Pseudo MCUs and successfully captured time-resolved upset events, where the complete readout of all memory bits was typically accomplished within a few seconds. In [25], MCU analyses were performed for 130- and 180-nm SRAMs, and multiple map-based MCU patterns were presented, including one Distant MCU with a Chebyshev distance of two. A dynamic measurement-based analysis of 2-bit MCU patterns in a 150-nm SRAM was presented in [26], where Monte Carlo simulations were also used to generate MCU patterns, and one Distant MCU with a Chebyshev distance of three was reported. In [8], MCU analyses were conducted for a 150-nm SRAM, and MCU patterns involving two or more bits were reported, including one 3-bit, two 8-bit, one 9-bit, and one 10-bit MCU, all with a Chebyshev distance of two. Although the authors noted the difficulty in distinguishing whether such error patterns originate from multiple reaction products of a single nuclear event or from a single long-range recoil, the presence of nonadjacent bit upsets suggests the possible occurrence of a Distant MCU. An SEU study on a 130-nm SRAM was reported in [7], where MCUs were defined as events with a Chebyshev distance of two or less; nevertheless, two distinct Distant MCU patterns were explicitly presented when checkerboard data patterns were applied. In [1], MCU characteristics in 90- and 130-nm SRAMs were analyzed, and map-based MCU patterns were provided; among them, one Distant MCU with a Chebyshev distance of four was identified. In addition, a recent study on a 5-nm SRAM [27] presented MCU analyses under irradiation with multiple particle species, including neutrons, employing a high-speed dynamic measurement capable of reading out the entire memory array within 1 s; however, bitmap-based MCU patterns for neutron-induced events were not explicitly reported. Despite these dynamic approaches and the availability of map-based MCU patterns, only a limited number of Distant MCU events were reported. Moreover, none of these studies focused on Distant MCUs as a primary observable for investigating neutron-induced physical mechanisms.

In many of these prior studies, MCUs were identified and analyzed primarily within relatively small Chebyshev distances. This treatment reflects practical considerations in SRAM design, where reliability requirements are often defined at the word level, and simultaneous bit flips within the same word constitute the dominant concern. In contrast, MCUs extending over larger Chebyshev distances are generally regarded as correctable by ECCs and therefore have not been treated as critical failure modes requiring detailed classification. As a result, widespread MCUs with large spatial extents have frequently been grouped into conventional MCU categories or excluded from focused discussion, even though they may carry important information about the underlying neutron-induced physical mechanisms.

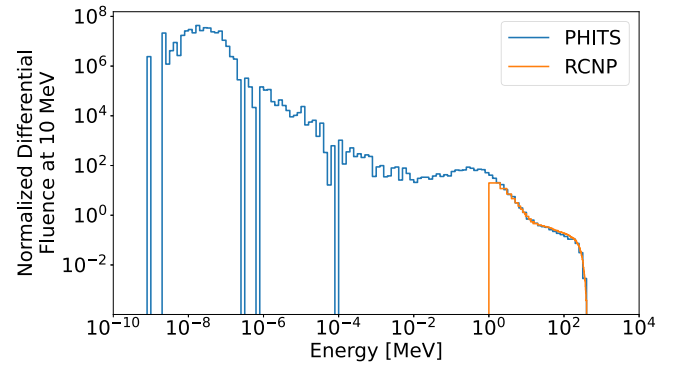


Fig. 2. Comparison of the differential neutron energy spectra obtained from the PHITS-based transport simulation and the RCNP measurement. Both spectra are normalized at 10 MeV.

III. EXPERIMENTAL SETUP

We conducted spallation neutron irradiation experiments at the Research Center for Nuclear Physics (RCNP), Osaka University, which provides a white neutron beam replicating the energy spectrum of terrestrial neutrons [28]. In the RCNP beamline, the neutron field at DUTs has an approximately uniform spatial distribution. Either a 108- or 300-mm-diameter collimator was used, depending on the irradiation configuration, but the two conditions showed no notable difference, indicating spatial flux uniformity, and were treated together in the SEU analysis. The typical flux for neutrons above 1 MeV at the DUT was about $1.11 \times 10^6/\text{cm}^2/\text{s}$, and the total fluence was $2.71 \times 10^{10}/\text{cm}^2$. The neutron energy spectrum provided by RCNP covers neutron energies above 1 MeV and was used as the primary reference for this work. Meanwhile, for the PHITS-based SEU simulations in Section IV, the neutron spectrum was extended down to 10^{-9} MeV using the spectrum obtained from PHITS simulations, based on private communication with D. Satoh (2024). The resulting unified spectrum shown in Fig. 2 is used to derive the SEU cross sections.

A. Quasi Event-Wise Dynamic Measurement Method

Fig. 1 illustrates the methods for soft error observation: (a) shows the conventional static measurement method, (b) the event-wise dynamic measurement method proposed in [10] for charged particles, and (c) the proposed quasi event-wise dynamic measurement method using quick self-scan SRAMs without detectors. In previous work, we developed an event-wise dynamic soft error measurement system for charged particles and validated it through a proton irradiation experiment [10]. The system (b) consists of a dedicated 55-nm SRAM chip capable of scanning data in 125 ns, a plastic scintillator, and a silicon detector. Thanks to the scintillator, the system can discard events caused by successive particles arriving within very short intervals, enabling accurate event-wise measurements.

In this work, we perform a quasi event-wise measurement for neutrons using the fast-scanning SRAM chips solely. Although we acknowledge that events caused by successive neutrons arriving within short intervals cannot be distinguished

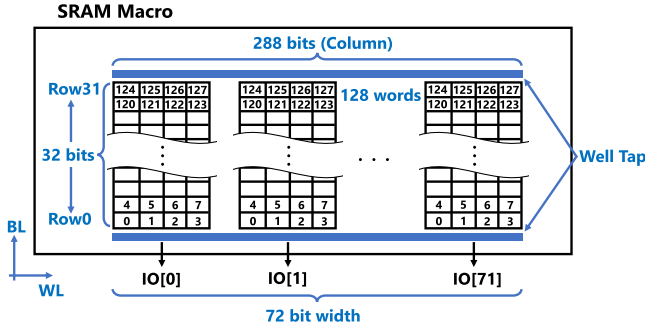


Fig. 3. SRAM macro consists of 32 rows (Row0–Row31) and 288 columns, organized into 128 words. The macro has a word width of 72 bits, corresponding to I/O ports IO[0]–IO[71]. WLs run horizontally across the rows, while BLs run vertically along the columns. Well taps are located at both ends of the BL direction. This macro structure is the same for both the 22- and 55-nm devices.

individually, we statistically confirm that such events, namely Pseudo MCUs, are negligible, as discussed in Section IV-A. Under this condition, we successfully obtain Distant MCUs, which are typically difficult to capture using static tests combined with bitmap-based event classification.

The chip incorporates SRAM macros with dedicated error checkers, a phase-locked loop (PLL), and a first-in-first-out (FIFO) buffer. The SRAM macro comprises 128 words, each 72 bits wide, as shown in Fig. 3. The SRAM macro is organized as a 2-D array of 32 rows and 288 columns. Each word consists of 72 bits, corresponding to 72 I/O ports. Word-lines (WLs) run horizontally across the rows, while bit-lines (BLs) extend vertically along the columns. Well taps are placed at both ends of the BL direction. The PLL generates a high-frequency clock to monitor bit-flips in the cells at several hundred megahertz. When a bit flip is detected, the event is forwarded to the FIFO for asynchronous readout.

B. Experimental Conditions

We used the fast-scanning SRAM chips fabricated in 22 and 55 nm bulk planar processes, arranging the device under test (DUT), as shown in Fig. 4. While 24 chips were in operation, high-speed scanning was performed on only 4 of them due to a heat dissipation issue. The memory capacities are 1.84 Mbit in 22 nm and 0.33 Mbit in 55 nm per chip, with supply voltages set to 0.7 and 0.9 V. At 0.9 V, the operating frequencies of the four tested chips were 708 MHz for the 22 nm devices and 474 MHz for the 55 nm devices, corresponding to scan intervals, which are the time to scan all 128 words, of approximately 181 and 270 ns, respectively. At 0.7 V, the frequencies decreased to 409 and 345 MHz, corresponding to scan intervals of approximately 313 and 371 ns, respectively. All SRAMs were initialized to zeros. Neutron irradiation was applied while continuously checking for any bit flips.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

This section presents and discusses the neutron irradiation results. In our SEU analysis, the probability that a single

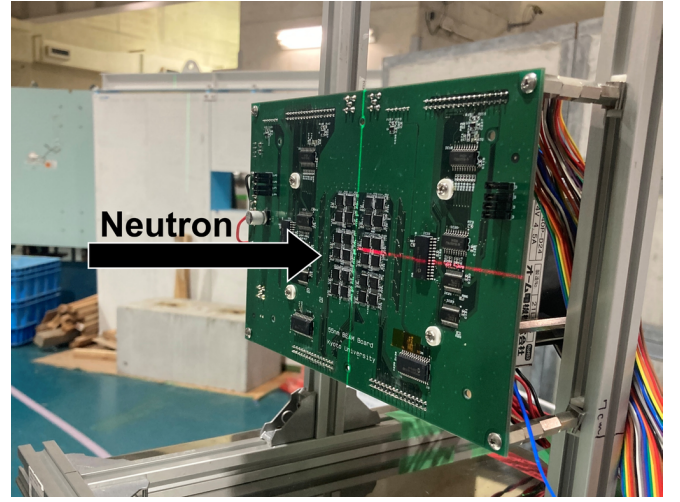


Fig. 4. Photograph of DUT used in the spallation neutron irradiation experiment at RCNP.

TABLE I

NEUTRON FLUX, SEU COUNTS, SCAN INTERVALS, SEU CROSS SECTION, AND THE RATIO OF THE PROBABILITY OF PSEUDO MCUs COMPARED TO SINGLE SEUs IN EACH MACRO

Configuration	Flux [$/\text{cm}^2/\text{s}$]	SEU counts	Scan interval [ns]	SEU CS [$/\text{cm}^2/\text{Mbit}$]	Prob. ratio in macro
22 nm, 0.9 V	1,498,406	2,247	181	4.939×10^{-9}	6.17×10^{-12}
22 nm, 0.7 V	1,766,673	2,638	313	6.770×10^{-9}	1.72×10^{-11}
55 nm, 0.9 V	1,591,130	617	270	2.397×10^{-8}	4.75×10^{-11}
55 nm, 0.7 V	1,654,833	923	371	2.805×10^{-8}	7.94×10^{-11}

particle induces bit flips in multiple macros is not theoretically zero. However, such events were not observed in this experiment.

A. SEU Cross Section and Pseudo MCU Probability

Table I lists the SEU cross sections, SEU counts, and neutron fluxes for each measurement configuration. The probability ratio represents the relative likelihood of multiparticle-induced events (i.e., Pseudo MCUs) compared to single SEU events within a single SRAM macro during one full-scan time window.

Let us derive the probability ratio mentioned in this section. Assuming that particle arrivals follow a Poisson distribution, the expected number of SEU events in one macro, denoted by λ , was given by

$$\lambda = \Phi \sigma B T \quad (1)$$

where Φ is the neutron flux (for energies above 10^{-9} MeV) in $/\text{cm}^2/\text{s}$, σ denotes the SEU cross section per Mbit in cm^2/Mbit , B is the number of Mbits in a macro (with each macro consisting of 72×128 bits), and T is the time window required to complete a full scan of an SRAM macro (i.e., the time needed to scan 128 words at the high-frequency operating clock). Under the Poisson model, the probabilities of zero and one SEU are

$$P(0) = e^{-\lambda} \quad (2)$$

$$P(1) = \lambda e^{-\lambda} \quad (3)$$

respectively, and the probability of two or more SEUs is

$$\begin{aligned} P(n \geq 2) &= 1 - P(0) - P(1) \\ &= 1 - (1 + \lambda) e^{-\lambda} \end{aligned} \quad (4)$$

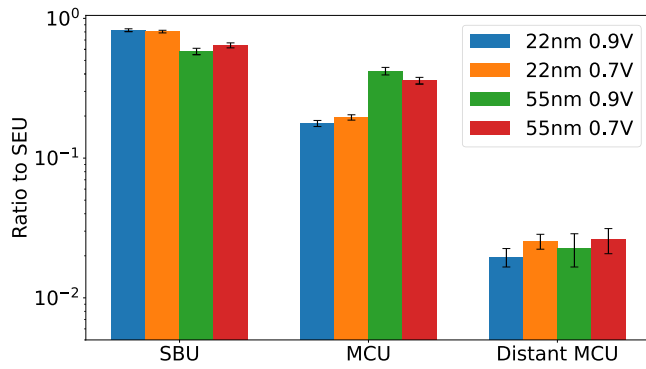


Fig. 5. Ratios of SBU, MCU, and Distant MCU relative to SEU. The total of SBU and MCU is 100%, with Distant MCU being a subset of MCU.

which quantifies the relative likelihood of multiparticle-induced events (i.e., Pseudo MCUs) compared to single SEU events.

As shown in Table I, for the 22 nm configurations, the probability ratio is on the order of 10^{-12} – 10^{-11} , while for the 55 nm configurations, it is on the order of 10^{-11} . This indicates that the likelihood of observing Pseudo MCUs is extremely small compared to that of single SEU events. Assuming 1000 SEUs are observed, the expected number of Pseudo MCUs is 10^{-7} or less. In contrast, the measured number of Distant MCUs is on the order of 10^1 or more per 1000 SEUs in all configurations (see Fig. 5). Therefore, the expected ratio of the number of Pseudo MCUs to that of Distant MCUs is below 10^{-8} . This confirms that Pseudo MCUs are negligibly rare compared to Distant MCUs and do not affect the statistics of Distant MCU events.

B. Ratio of SBU, MCU and Distant MCU to SEU

Fig. 5 shows the ratios of SBU, MCU, and Distant MCU relative to SEU for both 22 and 55 nm processes. Results at supply voltages of 0.7 and 0.9 V are presented for each process, and the error bars represent the standard error. Distant MCU refers to a phenomenon in which bit flips occur in cells that are physically distant due to secondary ions. In this article, we define a Distant MCU as an MCU that contains at least one pair of flipped bits whose Chebyshev distance is 2 or greater. For the 55 nm devices, the MCU ratio exceeds 35% at both supply voltages, whereas it remains below 20% for the 22 nm devices. Meanwhile, the proportion of Distant MCU is approximately 2%, which is comparable between the 22 and 55 nm processes; therefore, when considering only MCU events, Distant MCUs account for 13% of MCUs in the 22-nm devices at 0.7 V. Moreover, lowering the supply voltage increases the fraction of Distant MCU, since even secondary ions with lower linear energy transfer (LET), e.g., protons, can induce bit flips. These findings suggest that, with further technology scaling, both the occurrence of Distant MCUs and their fraction within MCUs may increase.

C. Analysis of MCU Characteristics Including Distant MCUs

1) *MCU Cluster Size*: Fig. 6 shows the MCU probability as a function of MCU cluster size, where the MCU

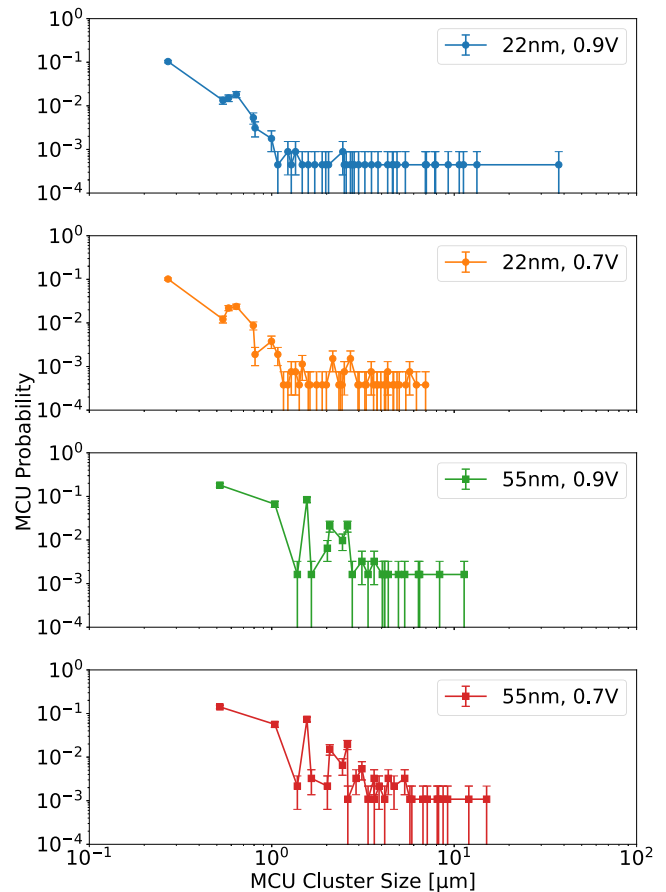


Fig. 6. MCU probability as a function of cluster size for four configurations: 22 nm at 0.9 and 0.7 V; 55 nm at 0.9 and 0.7 V.

probability is defined as the ratio of the number of MCUs with the cluster size of interest to the total number of observed SEUs, following the definition in [22]. The MCU cluster size is defined as the diagonal of the smallest rectangle that encompasses all bit flips within the MCU, to quantify the spatial extent of Distant MCUs. In [22], the largest MCU cluster sizes were 3 μm at the 45 nm node and 1.5 μm at the 65 nm node. However, our results indicate that the maximum MCU cluster size extends to 37 μm for the 22 nm device at 0.9 V, 7.0 μm for the 22 nm, 0.7 V, 11 μm for the 55 nm, 0.9 V, and 15 μm for the 55 nm, 0.7 V. In previous work, MCUs were inferred from bitmaps such that bit flips beyond a certain distance were not considered part of the same MCU. In contrast, our current experiments measure Distant MCUs directly, thereby capturing these larger cluster sizes. Furthermore, although the physical transport ranges of secondary ions are identical for both technology nodes, the node-dependent critical charge and sensitive volume (SVs) define a maximum spatial extent within which a secondary ion retains sufficient LET to induce a bit flip. As a result, the effective upset region extends up to approximately 320 μm in the 22 nm devices and 165 μm in the 55 nm devices [29], which can lead to an increase in the maximum observed MCU cluster size as more SEUs are observed. The MCU cluster size will be further investigated with PHITS simulations in Section V.

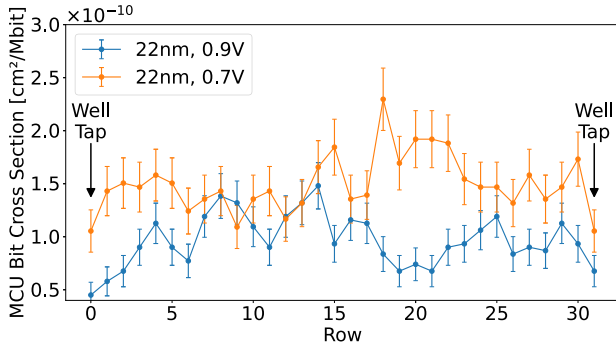


Fig. 7. MCU bit cross section as a function of row number for the 22 nm device at 0.9 and 0.7 V. Well taps are located at both ends along the row direction.

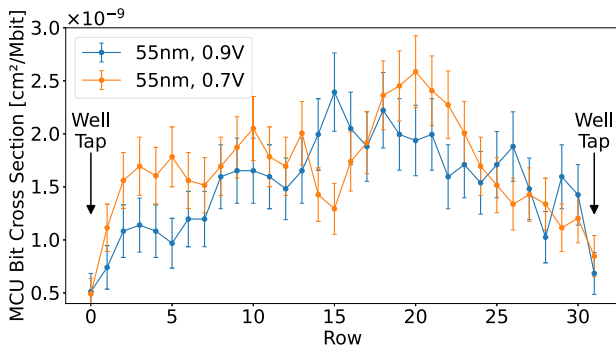


Fig. 8. MCU bit cross section as a function of row number for the 55 nm device at 0.9 and 0.7 V. Well taps are located at both ends along the row direction.

2) *MCU Dependence on Well Tap Distance*: Figs. 7 and 8 show the row-wise MCU bit cross sections for the 22 and 55 nm devices, respectively. In all configurations, the cross sections at the 0th and 31st rows, which contain well taps, are lower than those at the other rows. For the 22 nm device, the ratio of the maximum to minimum cross section is 3.3 at 0.9 and 2.2 at 0.7 V, indicating a greater influence of PBA at the higher voltage [7], [8], [30]. In contrast, for the 55 nm device, the ratios are 4.7 at 0.9 V and 5.3 at 0.7 V, showing that the row dependence of the cross section exhibits no significant difference between these two voltages.

3) *Distribution of MCU Pattern Types*: Fig. 9 shows the ratio of each MCU group to all observed MCUs for four configurations: 22 nm at 0.9 and 0.7 V, and 55 nm at 0.9 and 0.7 V. The MCU group $A \times B(C)$ is defined in [31], where A denotes the number of cells along the BL direction, B denotes the number of cells along the WL direction, and the number in parentheses C indicates the number of flipped bits in the pattern. Therefore, groups $2 \times 1(2)$ and $3 \times 1(2,3)$ correspond to bit patterns aligned along the BL direction, and $1 \times 2(2)$ corresponds to bit patterns along the WL direction. Group $2 \times 2(2)$ represents diagonal combinations of two flipped bits within a 2×2 bit-cell block. Group $2 \times 2(3,4)$ represents cases in which three of the four bits are flipped, or all four bits are flipped, within a 2×2 block. Except for $2 \times 1(2)$

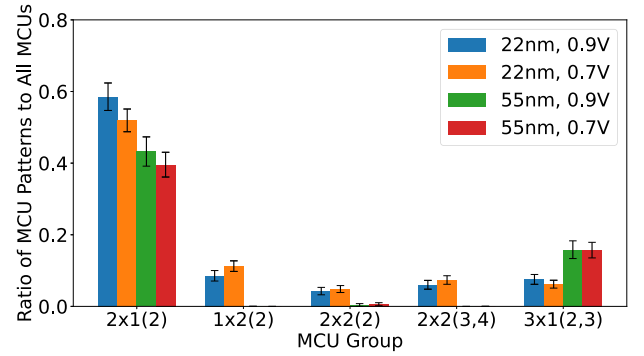


Fig. 9. Ratio of each MCU group to all observed MCUs for four configurations: 22 nm at 0.9 and 0.7 V; 55 nm at 0.9 and 0.7 V. Note that additional MCU groups exist; therefore, the ratios shown in the figure do not sum to one. The MCU groups are defined in [31].

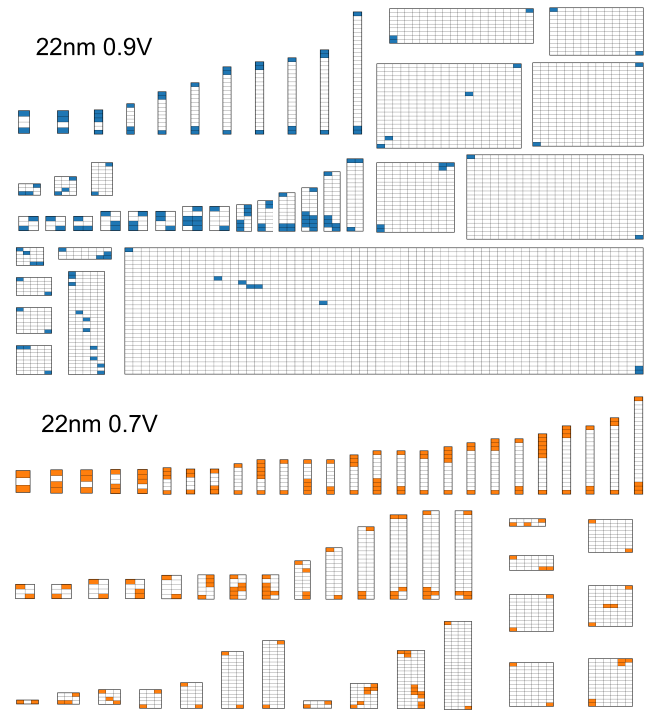


Fig. 10. Bit-flip patterns of distant MCUs observed in the 22-nm device at 0.9 and 0.7 V. All observed distant MCU events are shown, with colored cells indicating flipped bits.

and $1 \times 2(2)$, each group includes all patterns that become equivalent when rotated or mirrored.

For the 55 nm device, patterns aligned along the BL direction (2×1 and 3×1) dominate, indicating the stronger influence of PBA. In contrast, the 22 nm device exhibits a higher fraction of patterns including WL-direction flips, indicating that charge sharing has a greater impact than PBA in this technology node. These trends are consistent with the flip-pattern ratios reported for 20 nm devices analyzed using a static test in [31], suggesting similar underlying physical mechanisms.

4) *Patterns of Distant MCUs*: Figs. 10 and 11 show the bit-flip patterns of Distant MCUs observed in the 22- and 55-nm devices. Colored cells represent flipped bits, and each

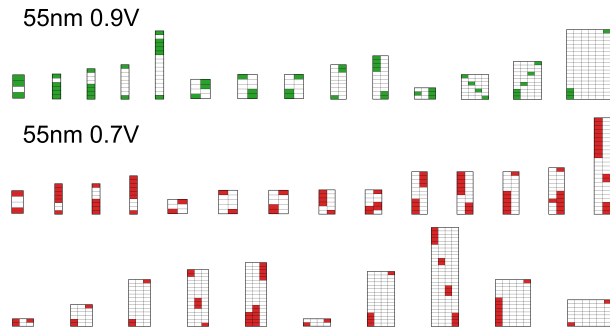


Fig. 11. Bit-flip patterns of Distant MCUs observed in the 55-nm device at 0.9 and 0.7 V. All observed Distant MCU events are shown, with colored cells indicating flipped bits.

figure includes all Distant MCU events observed under the corresponding supply voltage condition.

The secondary particles that cause Distant MCUs can be considered as follows: 1) a combination of a heavy ion and secondary light particles; 2) a single light particle; and 3) multiple light particles. In case 1), a heavy ion deposits a large amount of charge locally, producing a large MCU, while secondary light particles may induce isolated SBUs, resulting in combined patterns. In case 2), a single light particle leaves a straight track, leading to bit flips aligned along a line. In case 3), multiple light particles act simultaneously, which may result in patterns containing several SBUs.

Across all configurations, Distant MCU events were found to include patterns corresponding to cases 1)–3). For the 22-nm device at 0.9 V, very large-scale Distant MCUs were observed, which can be attributed to the tracks of light particles. In particular, the largest Distant MCU pattern of 64×31.8 was observed, corresponding to an MCU cluster length of $37.15 \mu\text{m}$. At 0.7 V, although such large-scale events were less frequent, a large number of patterns were still recorded, with about half of them consisting of single-column flips. In the 55-nm device, the number of observed events was limited due to statistics, yet Distant MCUs extending over as many as six columns were observed.

D. Comparison With Conventional Static Methods

Conventional static measurement methods accumulate all SEUs observed during an irradiation run onto a single bitmap and classify spatially adjacent bit flips as MCUs. Whereas “adjacency” is often interpreted as immediate neighboring cells, the actual spatial extent that should be treated as an MCU has not been quantitatively established. Restricting the grouping to physically adjacent cells corresponds to a Chebyshev distance of 1, whereas detecting non-adjacent or Distant MCUs requires expanding this distance to larger values. Thus, the Chebyshev distance used for grouping is the key parameter, and the choice of Chebyshev distance implicitly determines the balance between capturing true MCUs and introducing Pseudo MCUs due to excessive spatial merging.

To clarify this trade-off, we systematically evaluate the static bitmap method as a function of the Chebyshev distance

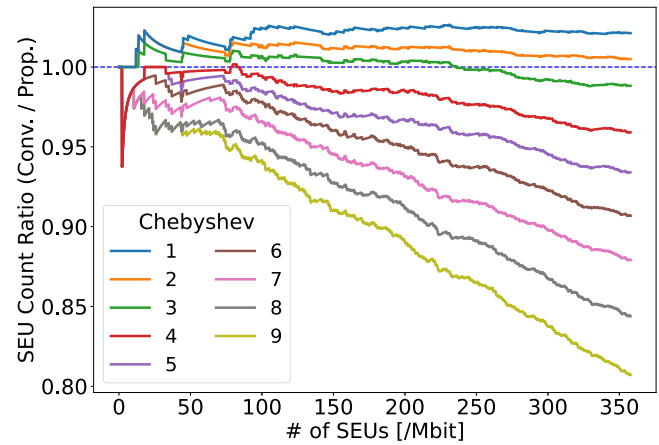


Fig. 12. Ratio of SEUs from the conventional static measurement method to those from the proposed quasi event-wise dynamic method as a function of total SEUs for the 22 nm device at 0.7 V. The legend shows the Chebyshev distance for grouping bit flips (distance 1 includes the eight neighboring cells).

and compare its output with the per-event SEU information obtained by the proposed quasi event-wise dynamic method. To reproduce the static method in this evaluation, we map the observed SEUs onto a bitmap in the order of detection and regroup them according to the Chebyshev distance used for clustering bit flips into MCUs. This enables a consistent comparison between the two methods.

This evaluation allows us to quantify: 1) the SEU counting error induced by different distance settings directly affecting the FIT estimation and 2) the fidelity with which the static method reconstructs the true SEU spatial patterns required for validating simulation-based SEU estimation. Furthermore, by analyzing how the identification probability of Distant MCUs evolves with increasing Chebyshev distance, we reveal how attempts to include Distant MCUs inevitably increase the misclassification of SBUs as MCUs, thereby exposing a fundamental limitation of conventional static analysis. As a result, we demonstrate that the SEU patterns obtained using the conventional bitmap method are not suitable for validating SEU simulations.

Fig. 12 shows the ratio of SEUs obtained by the conventional static measurement method to those from the proposed quasi event-wise dynamic method, for the 22 nm device operating at 0.7 V. The horizontal axis indicates the total number of SEUs per Mbit, and the vertical axis represents the ratio of SEU counts obtained by the conventional method to those from the proposed method. Here, the SEU counts of the proposed method are considered the ground truth. In the legend, each curve corresponds to the Chebyshev distance used for grouping bit flips into MCUs. When the Chebyshev distance is large, the SEU count ratio decreases rapidly with increasing total SEU count, because SBUs are more likely to be recognized as MCUs, leading to an underestimation relative to the actual number of SEUs. Conversely, when the Chebyshev distance is small, the ratio tends to be overestimated at low total SEU counts.

Fig. 13 demonstrates the ratio of SEUs from the conventional static method to those from the proposed dynamic

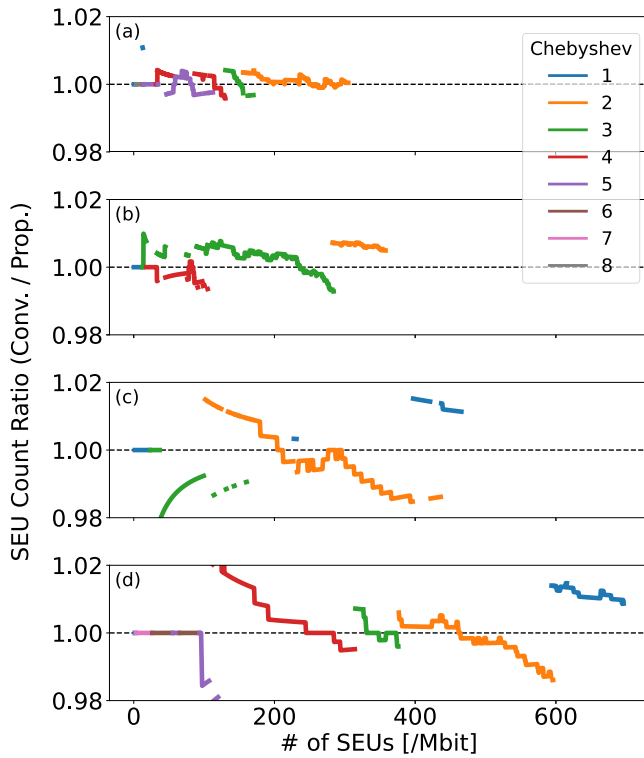


Fig. 13. Ratio of SEUs from the conventional static measurement method to the proposed quasi event-wise dynamic method for four configurations. (a) 22 nm, 0.9 V, (b) 22 nm, 0.7 V, (c) 55 nm, 0.9 V, and (d) 55 nm, 0.7 V. The legend shows the Chebyshev distance, and the highlighted curves indicate the distance with a ratio closest to 1.

method for four configurations: (a) 22 nm, 0.9 V; (b) 22 nm, 0.7 V; (c) 55 nm, 0.9 V; and (d) 55 nm, 0.7 V. In each case, only the portions of the curves corresponding to the Chebyshev distance that yield a ratio closest to 1 at each SEU count on the x -axis are shown. As the total number of SEUs increases, the optimal Chebyshev distance gradually shifts toward 1 for all processes. Furthermore, for the same total SEU count, a higher supply voltage tends to require smaller Chebyshev distances compared with a lower voltage.

Fig. 14 shows the accuracy of the SEU patterns obtained by the conventional static measurement method as a function of the total number of SEUs, assuming the proposed quasi event-wise dynamic method provides the true SEU pattern for the 22 nm device operating at 0.7 V. Here, the accuracy is defined as the proportion of SEU events that, when mapped onto a bitmap and regrouped using the bitmap method, exactly match the true SEU events observed in this experiment. Similar to Fig. 12, smaller Chebyshev distances yield higher accuracy as the total SEU count increases, whereas larger Chebyshev distances cause the accuracy to decline more rapidly.

Fig. 15 presents the SEU pattern accuracy across four configurations, and in all of them, the optimal Chebyshev distance gradually shifts toward 1. For SBUs, the highest accuracy is consistently achieved at a Chebyshev distance of 1, regardless of the total number of SEUs. In the case of MCUs, as more SEUs accumulate on the bitmap, larger Chebyshev distances can cause independent SEUs to be merged into the same MCU. Therefore, at high SEU counts, a Chebyshev

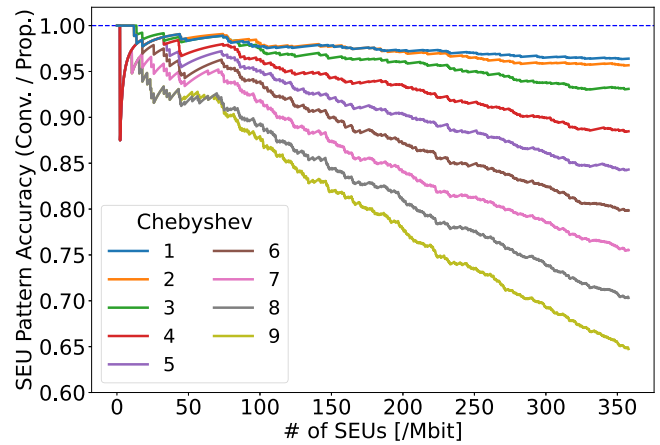


Fig. 14. Accuracy of SEU patterns by the conventional bitmap method relative to the proposed dynamic method for the 22 nm device at 0.7 V. The legend shows the Chebyshev distance for grouping bit flips (distance 1 includes the eight neighboring cells).

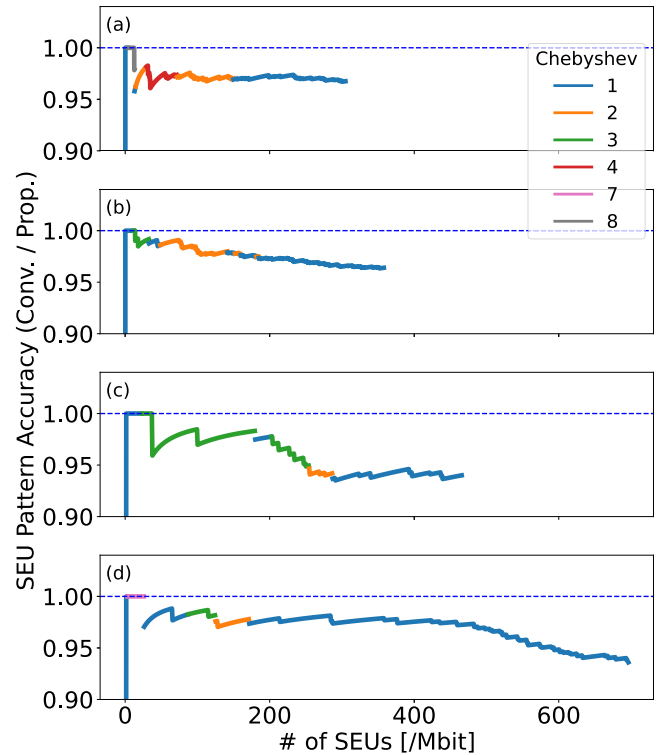


Fig. 15. Accuracy of SEU patterns by the conventional static method relative to the proposed dynamic method for four configurations. (a) 22 nm, 0.9 V, (b) 22 nm, 0.7 V, (c) 55 nm, 0.9 V, and (d) 55 nm, 0.7 V. The legend shows the Chebyshev distance for grouping bit flips; highlighted curves indicate the distance yielding an accuracy closest to 1.

distance of 1 is most appropriate, but in this case, any Distant MCUs cannot be counted.

Fig. 16 illustrates the cumulative probability of successfully identifying Distant MCUs as a function of Chebyshev distance when mapping them using the bitmap method, for four configurations: 22 nm at 0.9 and 0.7 V, and 55 nm at 0.9 and 0.7 V. Although the total number of SEUs is smaller for the 55 nm devices, the results indicate that Distant MCUs in 22 nm devices are more likely to occur at larger distances

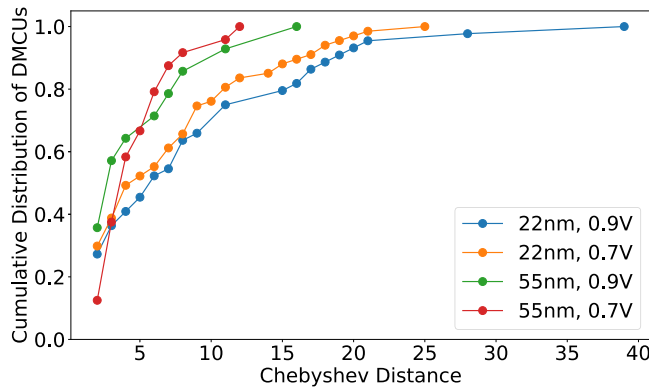


Fig. 16. Cumulative probability of successfully identifying Distant MCUs as a function of the Chebyshev distance when categorizing them via the bitmap method, for four configurations: 22 nm at 0.9 and 0.7 V; 55 nm at 0.9 and 0.7 V.

compared to the 55 nm devices. At a Chebyshev distance of 11, approximately 80% of Distant MCUs are correctly identified for 22 nm, 0.7 V.

These results highlight both the potential and the fundamental limitations of the bitmap-based static method. In principle, increasing the Chebyshev distance improves the likelihood of capturing the full spatial footprint of Distant MCUs; however, doing so also increases the probability of grouping independent SEUs into Pseudo MCUs. Conversely, setting the Chebyshev distance too low reduces the risk of misclassification but fails to identify Distant MCUs that extend over large separations. Thus, while the static method can provide partial insight into the spatial distribution of Distant MCUs, the inherent trade-off between capturing long-range events and suppressing Pseudo MCUs prevents it from reliably recovering the true physical event structure. This limitation demonstrates that static bitmap analysis cannot quantitatively determine the true Distant MCU distribution, thereby underscoring the necessity of event-wise dynamic measurements for accurate and reliable MCU characterization and for validating MCU simulation.

V. SIMULATION OF NEUTRON-INDUCED SEUS

We performed event-wise neutron irradiation simulations for the 22- and 55-nm devices using PHITS ver. 3.26 with event generator mode ver. 2. Neutron transport employed the evaluated nuclear-data library JENDL-4.0 below 20 MeV and the INCL4.6 intranuclear cascade model coupled with the GEM evaporation model for higher-energy neutrons. For neutron energies below 20 MeV, neutron-induced nuclear reactions and the resulting recoil nuclei and secondary particles in the sensitive volumes (SVs) were generated using the event generator mode based on JENDL-4.0 [32]. In this mode, all reaction products from a single nuclear event are stochastically generated on an event-by-event basis under energy and momentum conservation using evaluated nuclear data. This mode enables nuclear reactions in constituent materials of the device stack within the SVs, for which evaluated nuclear data are available, to be explicitly modeled.

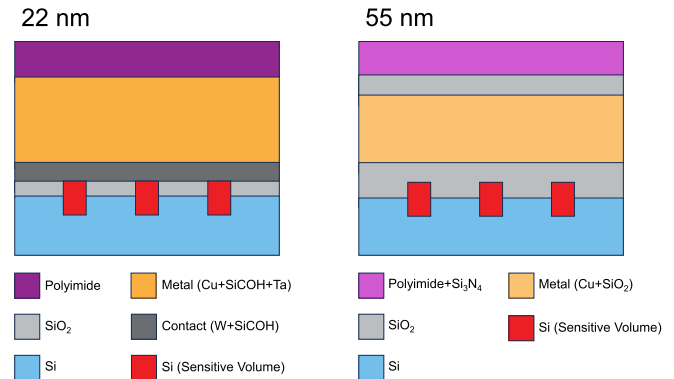


Fig. 17. Cross-sectional layer structures of the 22- and 55-nm SRAM devices used in the simulation.

A key objective of the simulation is to provide a physics-based interpretation of the experimentally observed Distant MCUs. Because PHITS generates full secondary-particle spectra and reaction channels on an event-by-event basis, it enables the identification of which secondary particles are responsible for the long-range charge deposition that produces Distant MCUs. The simulations are first validated by comparing the simulated events with the event-wise measurements, and are then used to analyze the particle species contributing to Distant MCU formation.

In the simulations, the SVs were modeled using the widely adopted rectangular parallelepiped (RPP) approximation, and SEUs were evaluated based on particle transport Monte Carlo simulations.

A. Simulation Method

We constructed 3-D PHITS models of the 22 and 55 nm devices, as shown in Fig. 17, and irradiated them with neutrons. The neutron energy spectrum obtained from a PHITS simulation reproducing the RCNP experimental setup was used as one irradiation condition, as shown in Fig. 2, and a total of 10^{10} neutrons were simulated for each device configuration.

The simulation included four chips, each containing 152.3 Mbit of SRAM for 22 nm or 29.4 Mbit for 55 nm, mounted together with packaging and printed circuit board (PCB). Each SRAM macro consists of a 72×128 -bit array. In our simulation model, each chip contains 16 530 ($= 570 \times 29$) macros for the 22-nm device and 3190 ($= 290 \times 11$) macros for the 55-nm device, respectively. While the number of SRAM macros in the model was larger than in the actual devices, the dimensions within each macro matched the real devices. Events in which bit flips occurred simultaneously in multiple macros were excluded from the analysis, as such events were not observed in our irradiation experiments due to the spacing between macros in the fabricated chips. To better reproduce experimental conditions, PHITS options for multiple scattering and delta-ray generation were enabled, and then electron transport was tracked. Delta-ray production was enabled when charged particles traversed the SV or the layers adjacent to the SV. Delta rays were

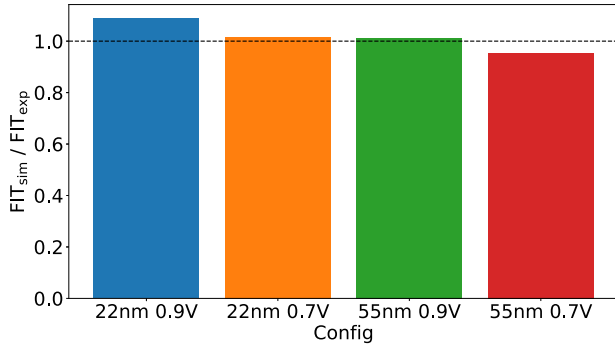


Fig. 18. Ratio of FIT rates obtained from simulation to those measured in experiments for four configurations: 22 nm at 0.9 V, 0.7 V, and 55 nm at 0.9 and 0.7 V, where the Q_c values used in the simulations are 0.7, 0.6, 0.8, and 0.7 fC, respectively.

generated for particle kinetic energies above 1 keV, and their transport was terminated at a kinetic energy cutoff of 1 keV.

Fig. 17 illustrates the cross-sectional layer structures of the 22- and 55-nm SRAM devices used in the simulation. Both devices share a similar overall structure, consisting of a polyimide-based layer on top, followed by stacked metal and contact layers, with the silicon substrate and SVs located at the bottom. The BEOL thicknesses were estimated from publicly available technology-node information. For the 22- and 55-nm devices, the BEOL structures were modeled as stacks of eight and eleven metal layers, respectively.

An SV is assigned around the OFF-state nMOS drain [33], with a depth of 0.5 μm for each SRAM cell [34]. An SEU is assumed to occur when the deposited charge exceeds a predefined threshold, called the critical charge Q_c . The value of Q_c depends on the device technology and supply voltage. In this study, Q_c values were selected such that the simulated failure in time (FIT) rates reproduce the experimental measurements for each device and voltage condition. In this work, an MCU is defined as multiple bit flips occurring within the same SRAM macro and induced by a single primary neutron event.

B. Simulation Results

In this section, we first follow the conventional simulation approach by determining the critical charge Q_c values that reproduce the experimental FIT rates and evaluating the resulting SEU distributions.

Fig. 18 shows the ratio of FIT rates obtained from simulations to those measured in experiments, for four configurations (22 nm at 0.9 and 0.7 V, and 55 nm at 0.9 and 0.7 V). Here, the critical charge Q_c was swept in steps of 0.1 fC so that the simulations reproduce the experimental FIT rates. The resulting Q_c values are 0.8 fC for 22 nm at 0.9 V, 0.7 fC for 22 nm at 0.7 V, 1.2 fC for 55 nm at 0.9 V, and 1.0 fC for 55 nm at 0.7 V.

Fig. 19 illustrates the ratios of SBUs, MCUs, and Distant MCUs obtained from simulations, together with the experimental results, which are identical to those in Fig. 5. In both simulation and experiment, SBUs are the most dominant, followed by MCUs and then Distant MCUs, indicating

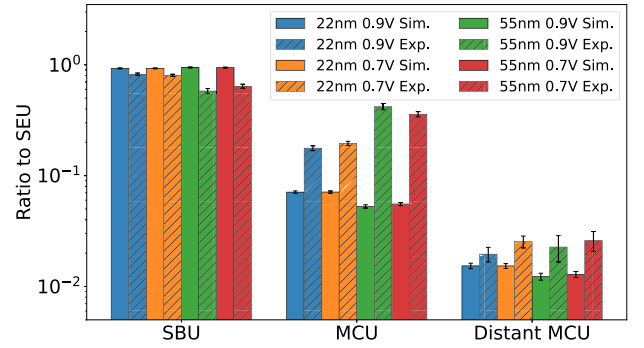


Fig. 19. Ratios of SBUs, MCUs, and Distant MCUs to the total SEUs obtained from the event-based neutron irradiation simulations for four configurations: 22 nm at 0.9 and 0.7 V, and 55 nm at 0.9 and 0.7 V.

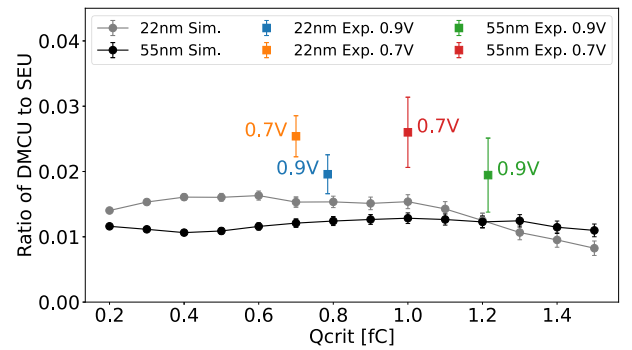


Fig. 20. Ratio of Distant MCUs to SEUs as a function of the critical charge Q_c for 22 and 55 nm devices at 0.9 and 0.7 V, comparing simulations (lines) with experiments (markers).

that the overall hierarchy of soft-error modes is reproduced. However, the simulated MCU ratios are lower than the experimental values, particularly for the 55 nm device. When only direct charge collection is considered, the simulations naturally predict a higher MCU probability for the 22 nm device due to its smaller critical charge. The fact that the experimental MCU fraction is instead higher for the 55 nm device strongly suggests that PBA-induced charge transport dominates MCU generation in the 55 nm SRAM, whereas its influence is reduced for the 22 nm technology. The PHITS-based model used in this work does not incorporate PBA and therefore cannot reproduce PBA-induced MCUs. While PBA-induced charge transport is likely the primary cause of the discrepancy, we also acknowledge that additional factors, such as uncertainties in SV geometry and cell-to-cell variation, may contribute to the remaining differences.

Fig. 20 shows the ratio of Distant MCUs to SEUs as a function of Q_c for the 22 and 55 nm devices at 0.9 and 0.7 V. In the experiments, the ratio may exhibit a weak dependence on supply voltage, but this trend is not statistically meaningful. Overall, the simulated ratio of Distant MCUs to SEUs agrees with the experimental results within a factor of two.

Fig. 21 compares the complementary cumulative probability distributions of MCU cluster sizes obtained from experiments and simulations for 22 and 55 nm devices at 0.9 and 0.7 V.

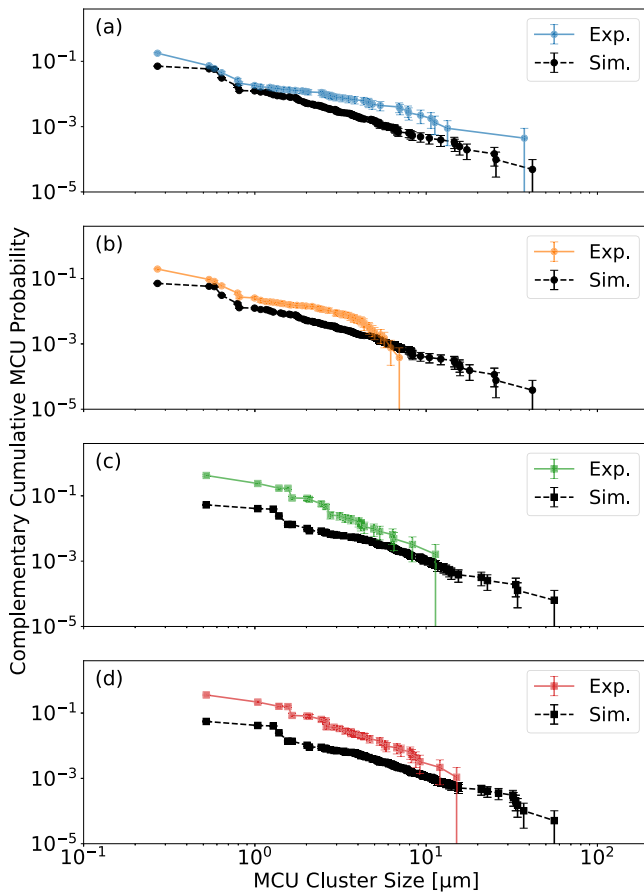


Fig. 21. Complementary cumulative MCU probability as a function of MCU cluster size for 22 and 55 nm devices at 0.9 and 0.7 V. The cumulative values are computed starting from the largest MCU cluster size. Experimental results are compared with simulations. Note that the complementary cumulative probabilities do not reach 1, since MCU events are only a fraction of the total SEUs. Error bars indicate standard errors in both measurements and simulations. (a) 22 nm, 0.9 V. (b) 22 nm, 0.7 V. (c) 55 nm, 0.9 V. (d) 55 nm, 0.7 V.

It should be noted that the complementary cumulative probabilities do not reach 1, since MCU events constitute only a fraction of the total SEUs. For the 22 nm device, the discrepancy is primarily caused by the smallest cluster sizes, where simulations significantly underestimate their occurrence compared with experiments. In contrast, for the 55 nm device, in addition to the smallest clusters, MCUs composed of several flipped cells also contribute to the discrepancy, leading to larger differences between experiments and simulations across a wider range of cluster sizes. The discrepancy in the small clusters, particularly for the 55-nm device, is likely attributable to PBA, which is not considered in the current simulation setup.

Fig. 22 shows the results after applying a clustering process to the experimental data to virtually mitigate PBA-induced MCUs. In this process, multiple flipped bits aligned along the BL direction, which are often attributed to PBA, are merged into one MCU cluster, with the representative bit defined as the cell closest to the well tap. This method eliminates BL-aligned two-bit MCUs and substantially improves the agreement between experiment and simulation. For all configurations,

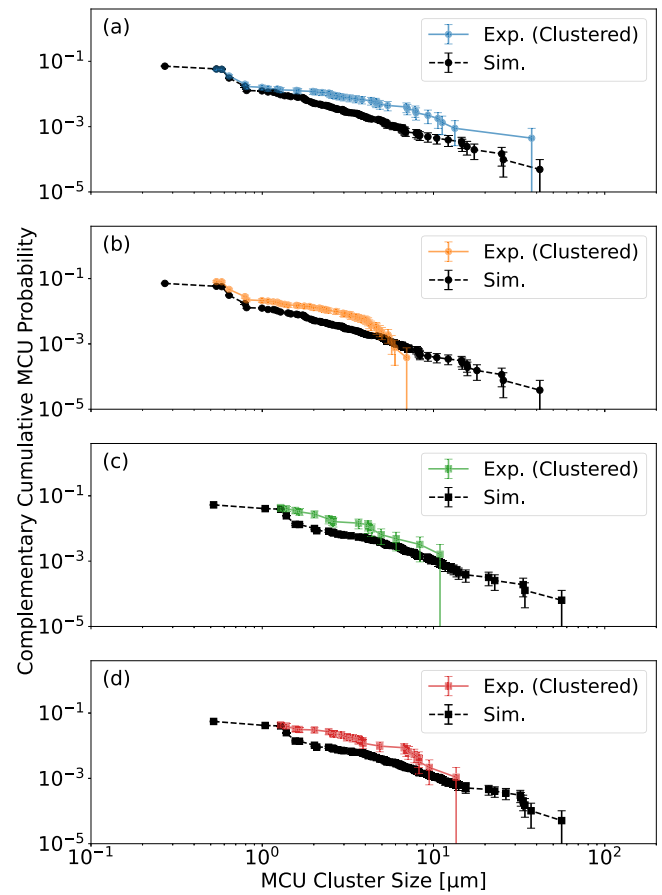


Fig. 22. Complementary cumulative MCU probability after applying the clustering process to the experimental data. In this process, all continuous bit upsets along the BL direction are merged into a single representative bit, where the bit closest to the well tap is chosen as the representative. (a) 22 nm, 0.9 V. (b) 22 nm, 0.7 V. (c) 55 nm, 0.9 V. (d) 55 nm, 0.7 V.

the cumulative MCU probability shows strong consistency between simulation and experimental results. Although the simulations still tend to slightly overestimate the probability, the discrepancy observed in Fig. 21 can be reasonably attributed to the PBA effect.

By suppressing the influence of PBA, we confirmed that the simulations can successfully reproduce the MCU behavior observed in the experiments. To further investigate the physical mechanisms responsible for the experimentally observed Distant MCUs, we performed a particle-level analysis of the simulated events.

Fig. 23 shows the ratio of dominant secondary particle species to all Distant MCUs for both event-based and bit-based classifications for the 22-nm device at 0.9 V with a critical charge of 0.8 fC. The figure also presents the maximum MCU cluster size associated with each dominant secondary particle species, as indicated on the right axis. In bit-based classification, each bit flip is attributed to the particle that generated it—more precisely, the particle that deposited the largest amount of charge—and this particle species is counted for each bit flip. In the event-based classification, the dominant species of an event is defined as the particle producing the largest number of bit flips, and the

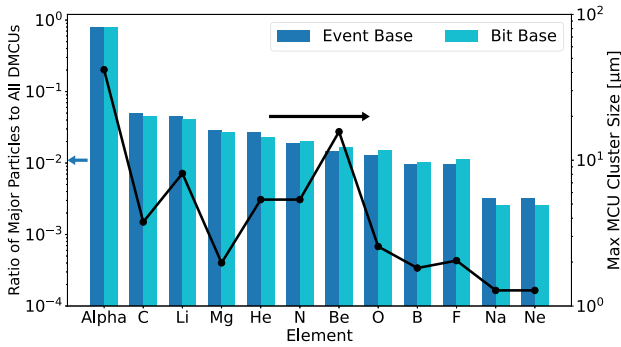


Fig. 23. Ratio of dominant secondary particle species to all Distant MCUs for event-based and bit-based classifications (left axis) and the maximum cluster size for each species (right axis), obtained from PHITS simulations for the 22-nm device at 0.9 V with a critical charge of 0.8 fC.

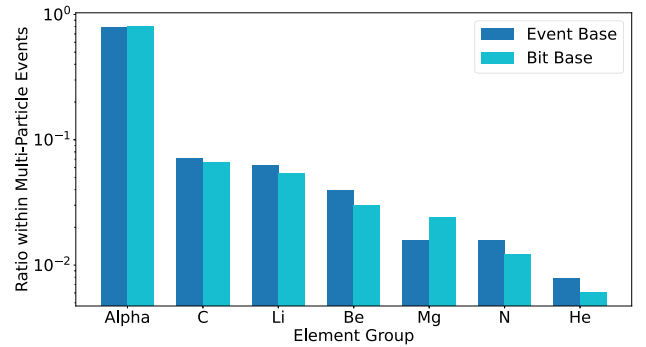


Fig. 24. Ratios of secondary particle species contributing to multi-particle Distant MCUs for event-based and bit-based classifications obtained from PHITS simulations for the 22-nm device at 0.9 V with a critical charge of 0.8 fC.

dominant species is counted for each event. In other words, if an MCU contains contributions from multiple secondary particles, the cluster size is assigned to the dominant particle of that MCU, as defined in the event-based classification.

As seen in the figure, alpha particles overwhelmingly dominate the population of dominant species in both event-based and bit-based evaluations. Nevertheless, when excluding delta-ray electrons, the maximum MCU cluster sizes associated with all particle species exceed $1.28 \mu\text{m}$, indicating that every species is capable of producing multi-cell-scale clusters beyond nearest-neighbor distances. Beryllium (Be) shows a notably large maximum cluster size; however, this event also includes a bit flip induced by an accompanying alpha particle, confirming that the extended spatial distribution originates from the alpha track rather than Be itself. Delta-ray electrons frequently deposit charge together with other particles and contribute to many bit flips, but no bit flip was observed to be caused solely by an electron. When considering neutron-silicon reactions such as those reported in [35], SEUs induced by silicon recoil nuclei were frequently observed; however, they were predominantly SBUs, and even when MCUs occurred, they were limited to adjacent cell flips and did not satisfy the definition of Distant MCUs. In contrast, magnesium (Mg) nuclei produced together with alpha particles through neutron-induced reactions possess sufficiently high LET to deposit charge over a wider spatial extent, thereby giving rise to Distant MCUs. Aluminum-related reactions can, in principle, generate Distant MCUs via proton emission; however, the charge deposited by protons was too small under the present simulation conditions, and no proton-induced Distant MCUs were observed.

Most Distant MCUs are generated by a small number of secondary particles, indicating that spatially extended clusters are typically produced by a limited set of energetic ions rather than by coincident interactions from many particles. In the present analysis, approximately 80% of Distant MCUs are associated with a single secondary particle, while about 20% involve two secondary particles, and contributions from three particles are rare (<1%). Focusing on the rarer cases that include two particles, Fig. 24 presents the ratios of secondary particle species contributing to such multi-particle Distant MCUs for

both event-based and bit-based classifications, obtained from PHITS simulations for the 22-nm device at 0.9 V. In the bit-based classification, alpha particles account for 81% of all bit flips within these events, demonstrating their strong dominance even when other species are present. A similar trend is observed in the event-based classification, where alpha particles also contribute 79% of the events containing multiple secondary particles, highlighting their leading role in generating multi-species Distant MCUs.

Taken together, these results show that neutron-induced Distant MCUs are predominantly governed by alpha particles, which serve as the primary contributors to long-range charge deposition. At the same time, the analysis clearly indicates that other heavy particle species also produce Distant MCUs, as evidenced by their maximum cluster sizes exceeding $1.28 \mu\text{m}$. These non-alpha species, therefore, play a non-negligible role in forming extended upset clusters, even though their occurrence probability is smaller. The combination of event-wise dynamic measurements and Monte Carlo transport simulations thus enables a particle-resolved understanding of Distant MCU formation and clarifies both the dominant role of alpha-induced tracks and the measurable contributions of other secondary particles in shaping large upset clusters.

VI. CONCLUSION

We performed a quasi event-wise SEU measurement that continuously monitored bit flips during neutron irradiation in 22- and 55-nm bulk planar SRAMs. This method achieved a Pseudo MCU probability ratio on the order of 10^{-11} , serving as a reliable ground truth. Using this data, we evaluated the limitations of conventional bitmap-based SEU analysis. We quantitatively demonstrated an inherent trade-off: for the 22-nm device at 0.7 V, a Chebyshev distance of 11 was required to capture 80% of Distant MCUs, yet such expansion of the grouping distance to detect the remaining events erroneously merged independent SEUs into Pseudo MCUs, making accurate event identification difficult.

Our results show that about 2% of events are classified as Distant MCUs, with maximum MCU cluster sizes of $7.0 \mu\text{m}$ for 22-nm devices and $15 \mu\text{m}$ for 55-nm devices,

and Pseudo MCU probabilities on the order of 10^{-11} . Using the measurement data, we evaluated the accuracy and limitations of conventional bitmap-based SEU analysis, which revealed fundamental limitations in identifying MCU events.

In addition, we performed PHITS-based simulations to reproduce the event-wise experimental results and to analyze the detailed physical mechanisms of Distant MCUs. While the ratio of Distant MCUs showed no significant difference, the PHITS model could not reproduce PBA, resulting in a large discrepancy in the overall MCU ratio. However, once the influence of PBA was approximately removed from the measurement data, the simulated MCU probability agreed well with the experimental results. Based on this validated simulation, particle-level analysis identified that approximately 78% of the observed Distant MCUs are attributed to secondary alpha particles.

Our results clarify that static bitmap-based testing is sufficient for estimating overall FIT rates but is fundamentally limited in identifying true MCU events, especially long-range Distant MCUs, due to the unavoidable mixing of independent SEUs. In contrast, quasi event-wise dynamic measurement provides ground-truth SEU sequences with negligible Pseudo MCU contamination, enabling accurate characterization of Distant MCUs and reliable validation of particle-transport simulations. Thus, the static method remains practical for FIT evaluation, whereas the dynamic method is essential for studies requiring event-level physical fidelity.

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