

22.4 A Radiation-Hardened Self-Healing CMOS Imager with Online Pixel/Logic Annealing and Tile-Adaptive Compression for Space Applications

Quan Cheng^{*1,2}, Zhengke Yang^{*1}, Haoyuan Li², Qiufeng Li¹, Zhen Kong¹, Gaoqiang Niu¹, Yuan Liang¹, Jiamin Li¹, Jerald Yoo³, Masanori Hashimoto², Longyang Lin¹

¹Southern University of Science and Technology, Shenzhen, China, ²Kyoto University, Kyoto, Japan, ³Seoul National University, Seoul, Korea

*Equally Credited Authors (ECAs)

Abstract

CMOS imagers in space suffer radiation-induced faults and downlink bandwidth limits. This work presents an 180nm self-healing imager with localized online thermal annealing for both pixels and logic, as well as adaptive ROI-lossless compression for 75.5% data

reduction. Measurements show 4.82×/3.97× reductions in pixel/logic leakage and nearly full image recovery after 20kGy X-ray exposure, enabling continuous, robust space imaging.

CMOS imagers are indispensable in space missions for Earth observation, planetary exploration, and autonomous navigation [1-4]. However, long-duration deployment exposes them to harsh radiation, inducing transient and permanent faults in pixel arrays and logic, which manifest as hot pixels, leakage, and timing errors [3-8], ultimately degrading image quality and mission reliability. At the same time, massive onboard image data often exceeds available satellite downlink bandwidth [9], demanding imagers with both radiation tolerance and efficient in-sensor compression (Fig. 22.4.1).

is temporarily suspended when the readout reaches the annealed row, yielding an effective annealing window of 127 out of 128 row periods per readout cycle.

Figure 22.4.3 (bottom) shows the principle of localized thermal annealing in digital logic using scan-assisted faulty-path detection and selection. Razor-based flip-flops [12], which support error detection, are augmented with a triple-modular redundancy (TMR) structure for immediate error correction and an additional latch ($L1$ in Fig. 22.4.3) to store error flags, enabling asynchronous readout via a scan chain (SC) without interrupting normal logic operation. Within the TMR, intentional delays are inserted in both the clock and data paths, introducing slight temporal skew among the three flip-flops to enhance single event transient (SET) tolerance and enable sensing of delay-induced timing violations by cumulative radiation effects (e.g., TID). A persistent error flag observed on the same path therefore serves as an indicator of a hard error, and the SC is reused to select this faulty path for annealing (e.g., via SC flip-flop $F1$ in Fig. 22.4.3). When annealing is enabled (HE=1), the selected path (SQ=1) is toggled at high frequency (>1.5GHz) by a digital annealer, inducing localized Joule heating (Fig. 22.4.3, bottom-right). The annealer generates a local clock with a compact ring oscillator (delay cell, inverter, and multiplexer) and maximizes switching activity on the faulty path by inverting the flip-flop input each cycle. To accommodate intermittent logic annealing, a short healing phase is inserted after normal operations (image readout, novelty detection, and image compression), resulting in only a slight frame-rate reduction (~5%). Meanwhile, the Razor-TMR flip-flops, designed with intentional delay skew, sustain normal operation under radiation-induced errors, as any error in one flip-flop can be detected and corrected by the majority voter leveraging the other two.

Prior radiation-hardened techniques such as enclosed layout transistors (ELTs) [4-6], wide-bandgap photodiodes [7], and voltage compensation [8] improve radiation tolerance but cannot repair accumulated damage (i.e., hard errors). Redundancy-based self-healing [10] can replace damaged circuits with spares but introduces large area overhead. In contrast, thermal annealing can restore device performance by releasing trapped charges caused by Total Ionizing Dose (TID) and repairing lattice defects induced by Displacement Damage Dose (DDD). A prior space imager [3] employed spike-based architecture with on-chip thermal annealing for pixel recovery. However, this approach interrupts imaging during annealing, does not address degradation in logic circuits, and lacks scalability due to its spike-based processing. Therefore, there is no scalable, continuous-operation space imager that can heal both pixels and logic while also mitigating the downlink bottleneck.

This work presents a radiation-hardened self-healing imager that integrates localized online thermal annealing for both pixels and processing logic, enabling autonomous recovery from radiation-induced degradation. Unlike prior designs, the proposed architecture supports online annealing without interrupting imaging, allowing continuous operation during self-healing. In addition, a tile-based adaptive compression engine applies per-tile variable compression ratios, dynamically allocating bandwidth according to local image complexity. A 180nm test chip demonstrates successful online self-healing for nearly full image quality recovery, with a 4.82× reduction in pixel dark current and a 3.97× reduction in logic leakage after 20kGy X-ray exposure. The proposed compression reduces transmitted data volume by 75.5% without loss of information in regions of interest (ROI), while consuming 26.48mW at 100fps.

Figure 22.4.4 (right) shows the proposed tile-based adaptive image compression. Each frame is partitioned into tiles, where edge magnitudes are extracted using a Sobel operator and inter-frame edge differences set compression levels from 0 (lossless) to 15 (highly compressed). These levels control an adaptive blurrer that attenuates high-frequency content in less critical regions, with blur strength N mapped from the tile values. A lightweight pre-quantization then aligns pixels to coarse gray-level grids to reduce symbol diversity. The processed image is passed to a LOCO-I-based predictor and context modeler [13], with configurable near-lossless tolerance, and prediction errors are encoded via a Golomb encoder. This approach preserves key scene details while enabling efficient transmission under tight bandwidth and compute constraints.

Illustrated in Fig. 22.4.2, the proposed imager integrates a 128×128 PWM-based pixel array with localized thermal annealing, column-parallel time-to-digital converters for pixel readout with support for online annealing via pixel masking, scan-assisted faulty-path detection and logic annealing, and a tile-based adaptive image compression engine. During normal imaging, the compression pipeline applies tile-based adaptive compression guided by edge complexity, preserving key scene content while reducing bandwidth. Radiation damage detection is performed intermittently: hot pixels are identified by shuttered readout compared to a threshold, while logic faults are detected by monitoring error flags from Razor flip-flops. Localized thermal annealing is then applied on individual damaged pixels, while faulty logic paths are healed by an internally generated high-frequency clock applied only to the selected path (Fig. 22.4.2, bottom).

Test-chip temperature maps captured by an infrared thermal camera confirm localized thermal annealing in both the pixel array (~167μW/μm² at 1.8V) and digital logic (~13μW/μm² at 1.8V), as shown in Fig. 22.4.5 (top-left). After exposure to 20kGy X-ray irradiation, the dark current in the pixel array and the leakage current in the digital logic increase by 181.13× and 4.13×, respectively, and the captured image quality degrades severely, indicating radiation-induced damage. After four annealing rounds (10 min/round for pixel; 1 hr/round for logic), leakage currents across 8 chips are reduced by 4.82× and 3.97×, respectively, with image quality progressively restored to nearly full recovery (Fig. 22.4.5, middle). The digital logic exhibits no timing errors under X-ray irradiation up to 20kGy, attributed to the relatively low operating frequency (≤80MHz) that provides ample timing margin. Hence, the healing effect in digital logic is primarily evidenced by reduced leakage currents. Shown in Fig. 22.4.5 (right), the adaptive image compression processes 128×128 frames (8-bit, 16 kB) via Sobel edge detection and tile-based object detection on 64 tiles, where tile values determine compression ratios. Detail-critical tiles (e.g., around objects) use low or lossless compression as required, while background tiles are heavily compressed. After LOCO-I prediction, context modeling, and Golomb encoding, the bitstream is reduced to 3.92kB (75.5%) while preserving full detail in the regions of interest.

Figure 22.4.3 (top) shows the proposed 6T PWM-based self-healing pixel design, where the photodiode (PD) operates in reverse bias for readout or forward bias for localized thermal annealing. During normal operation, the pixel is first reset by turning on $M2$ ($RSTN=0$) and $M1$ ($V_{RAMP}=V_{RST}$) for threshold variation cancellation (TV), similar to [11]. After reset, $M2$ is turned off and a ramp signal is applied to V_{RAMP} , while the in-pixel comparator ($M1$ and $M3$) with gain stage $M4$ generates a pulse whose width is proportional to light intensity. Unlike [11], which omits the row selection transistor, the proposed design includes $M5$ to suppress leakage currents from unselected rows on the column lines. Radiation-damaged pixels are detected by temporarily closing the shutter to capture a dark frame; if any pixel value exceeds a predefined threshold, it is flagged as damaged. The healing process is then triggered by switching the corresponding pixel into forward bias through $M6$ and activating a column-shared annealing driver (1.5-to-2.0V) [3], which initiates localized thermal annealing. This selective activation minimizes power overhead while enabling per-pixel recovery. Continuous imaging with online pixel annealing is achieved through pixel masking (Fig. 22.4.4, left). During annealing, the driver occupies the selected column, making its pixel readouts unavailable. These missing values are interpolated from the average of the adjacent horizontal neighbors. Furthermore, annealing

Comparison with prior radiation-hardened imagers (Fig. 22.4.6) shows that the 180nm test chip (Fig. 22.4.7) uniquely supports both pixel and logic localized online thermal annealing together with ROI-lossless compression at up to 400fps, enabling continuous and robust operation for long-duration space missions. Unlike [3], which employs a spiking-pixel, fully parallel architecture with poor scalability and no logic healing, the proposed PWM-based architecture scales efficiently to large arrays while providing continuous self-healing and compression, retaining full radiation-hardening capability.

Acknowledgement:

This work is partially supported by the National Natural Science Foundation of China under Grant 62274081, Guangdong Projects (Grant 2023QN10X177, Grant 2025B0101180002), and the Grant-in-Aid for Scientific Research (S) from the Japan Society for the Promotion of Science (JSPS) under Grant 24H00073.

References:

[1] A. A. Omar, M. M. Farag and R. A. Alhamad, "Artificial Intelligence: New Paradigm in Deep Space Exploration," *14th International Conference on Developments in eSystems Engineering (DeSE)*, Sharjah, United Arab Emirates, 2021, pp. 438-442. <http://doi.org/10.1109/DeSE54285.2021.9719425>

[2] I. Kostavelis, L. Nalpantidis, E. Boukas *et al.*, "Spartan: Developing a vision system for future autonomous space exploration robots". *Journal of Field Robotics*, 2014, 31(1): 107-140. <http://doi.org/10.1002/rob.21484>

[3] Q. Cheng *et al.*, "A Radiation-Hardened Neuromorphic Imager with Self-Healing Spiking Pixels and Unified Spiking Neural Network for Space Robotics," *Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2025, pp. 1-3. <http://doi.org/10.23919/VLSITechnologyandCir65189.2025.11075180>

[4] V. Goiffon *et al.*, "Total Ionizing Dose Effects on a Radiation-Hardened CMOS Image Sensor Demonstrator for ITER Remote Handling," *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 101-110, Jan. 2018. <http://doi.org/10.1109/TNS.2017.2765481>

[5] C. Virrmonois *et al.*, "Total Ionizing Dose Versus Displacement Damage Dose Induced Dark Current Random Telegraph Signals in CMOS Image Sensors," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 3085-3094, Dec. 2011. <http://doi.org/10.1109/TNS.2011.2171005>

[6] J. Bogaerts, B. Dierickx, G. Meynants and D. Uwaerts, "Total dose and displacement damage effects in a radiation-hardened CMOS APS," *IEEE Transactions on Electron Devices*, vol. 50, no. 1, pp. 84-90, Jan. 2003. <http://doi.org/10.1109/TED.2002.807251>

[7] M. Tsutsumi, T. Meguro, A. Takeyama, T. Ohshima, Y. Tanaka and S. -I. Kuroki, "Integrated 4H-SiC Photosensors With Active Pixel Sensor-Type Circuits for MGy-Class Radiation Hardened CMOS UV Image Sensor," *IEEE Electron Device Letters*, vol. 44, no. 1, pp. 100-103, Jan. 2023. <http://doi.org/10.1109/LED.2022.3226494>

[8] B. R. Dean *et al.*, "Back-Biasing Strategy to Mitigate TID-Induced Threshold Voltage Shift in 22nm FDSOI Transistors," *IEEE Transactions on Nuclear Science*. <http://doi.org/10.1109/TNS.2025.3613463>

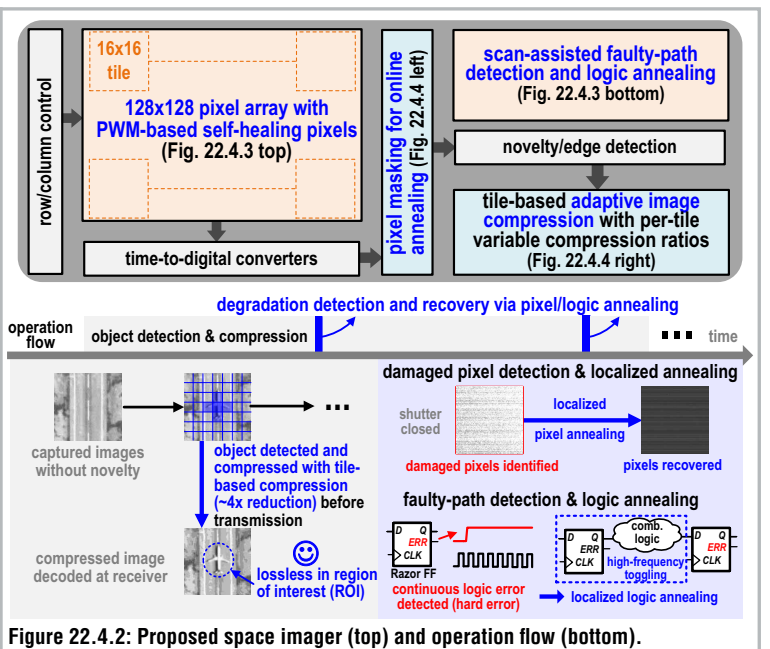
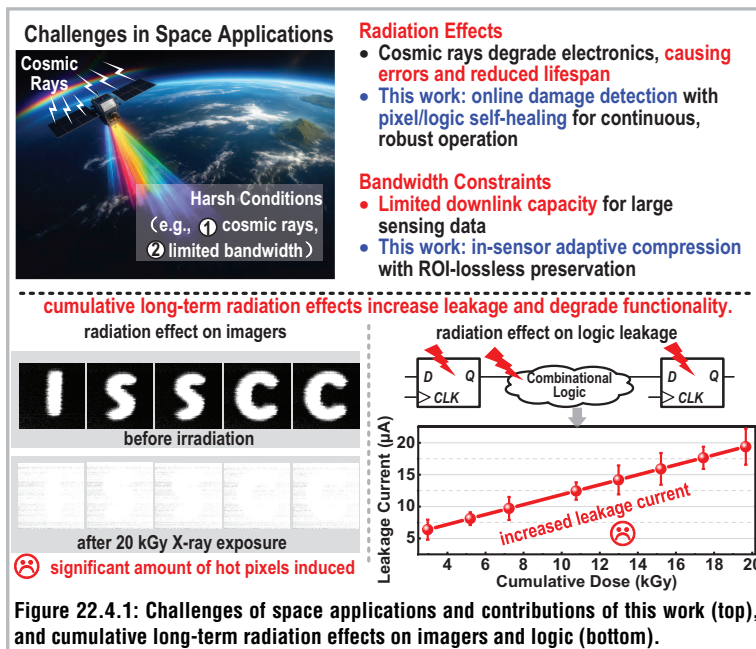
[9] O. Kodheli *et al.*, "Satellite Communications in the New Space Era: A Survey and Future Challenges," *IEEE Communications Surveys & Tutorials*, vol. 23, no. 1, pp. 70-109, Firstquarter 2021. <http://doi.org/10.1109/COMST.2020.3028247>

[10] P. Balasubramanian and D. L. Maskell, "A Self-Healing Redundancy Scheme for Mission/Safety-Critical Applications," *IEEE Access*, vol. 6, pp. 69640-69649, 2018. <http://doi.org/10.1109/ACCESS.2018.2880763>

[11] A. Y. -C. Chiou and C. -C. Hsieh, "An ULV PWM CMOS Imager With Adaptive-Multiple-Sampling Linear Response, HDR Imaging, and Energy Harvesting," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 298-306, Jan. 2019. <http://doi.org/10.1109/JSSC.2018.2870559>

[12] M. Fojtik *et al.*, "Bubble Razor: An architecture-independent approach to timing-error detection and correction," *IEEE International Solid-State Circuits Conference*, San Francisco, Feb. 2012, pp. 488-490. <http://doi.org/10.1109/ISSCC.2012.6177103>

[13] M. J. Weinberger, G. Seroussi and G. Sapiro, "The LOCO-I lossless image compression algorithm: principles and standardization into JPEG-LS," *IEEE Transactions on Image Processing*, vol. 9, no. 8, pp. 1309-1324, Aug. 2000. <http://doi.org/10.1109/83.855427>



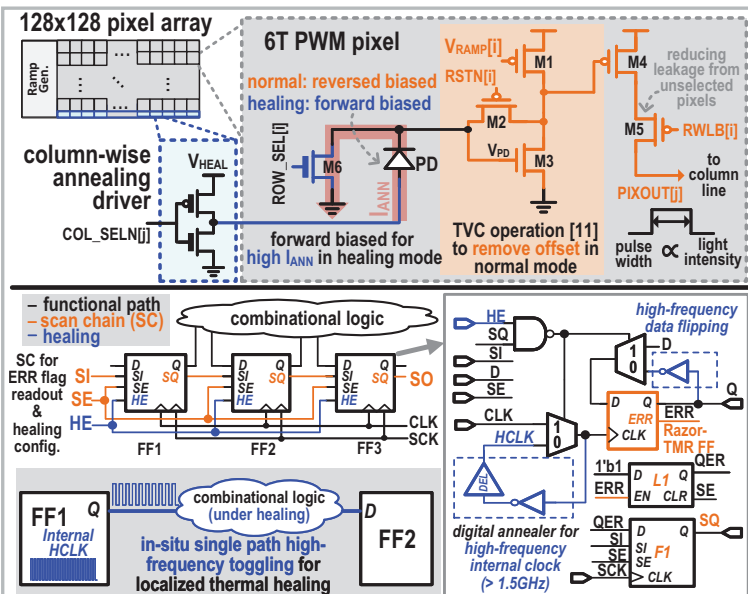


Figure 22.4.3: Proposed 6T PWM-based self-healing pixel (top) and localized thermal annealing of digital logic using scan-assisted path selection (bottom).

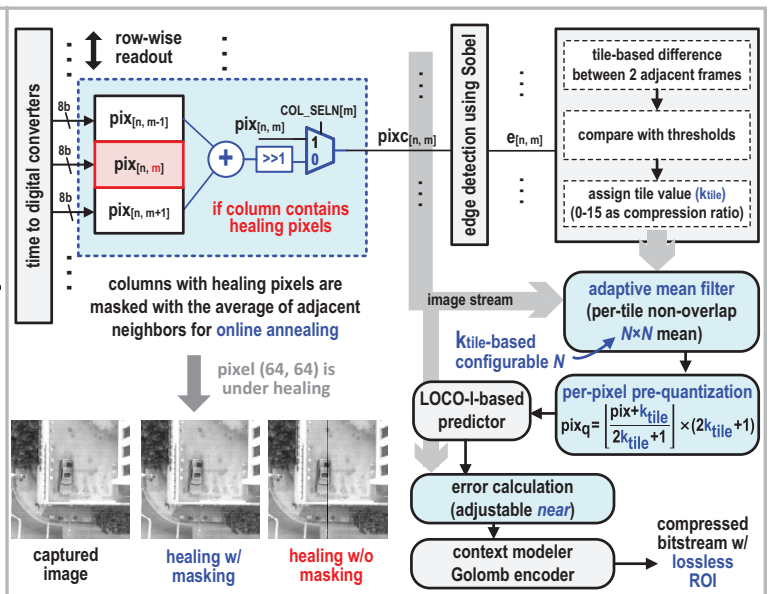


Figure 22.4.4: Proposed pixel masking for online annealing (left) and tile-based adaptive image compression (right).

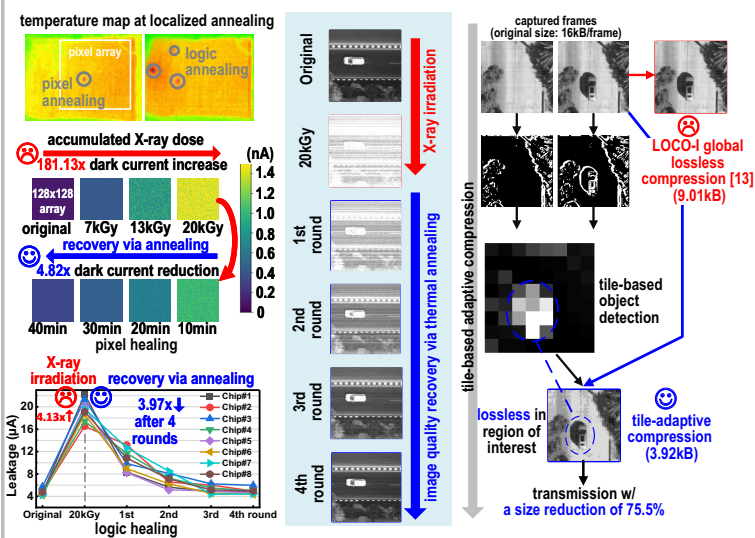


Figure 22.4.5: Measurement results of X-ray irradiation and self-healing with near full image quality recovery, and tile-based adaptive image compression.

	[4] TNS'18	[3] VLSI'25	This work
Technology	180nm CIS	180nm CMOS	180nm CMOS
Architecture	imager only	imager, SNN	imager, novelty/edge detection, adaptive data compression
Supply voltage (V)	analog: 3.3 digital: 1.8	0.6-0.8 (normal) 1.5-2.5 (healing)	0.6-1.0 (analog), 1.3-1.8 (digital) 1.5-2.0 (healing)
Area (mm ²)	not reported	28.275	18.243
Pixel array	256x256	73x73	128x128
Pixel size (μm ²)	10x10	22x21	20x20
Pixel structure	3T	14T spike	6T PWM
Frame/event rate	25 fps	1-5000 event/s	100-400 fps
Image compression ratio	no compression	no compression	~ 4x (2.3x higher compared to LOCO-I)
Power consumption	not reported	76.3 μW @ 0.6V	31.80 μW @ 0.6V, 100fps (analog) 26.48 mW @ 1.3V, 100fps (digital)
Radiation hardening	ELT, gate-overlap PD	pixel annealing, NW-guarded PD	pixel/logic online annealing, Razor-TMR FF, NW-guarded PD
Online healing	no	no	yes
*Dark current increase	>100x @20kGy X-ray	~20x (after healing) @14kGy Alpha Am-241	~38x (after healing) @ 20kGy X-ray
Power density for thermal annealing	N/A	114 - 465 μW/μm ² (pixel only)	93 - 221 μW/μm ² (pixel) 7 - 18 μW/μm ² (logic)
Dark/leakage current reduction after healing	N/A	6.25x (pixel only) @ 14kGy Alpha Am-241	4.82x @ 20kGy X-ray (pixel) 3.97x @ 20kGy X-ray (logic)

*the rise in pixel dark current after irradiation compared to that of the non-irradiated reference device. Figure 22.4.6: Comparison with state-of-the-art radiation-hardened imagers.

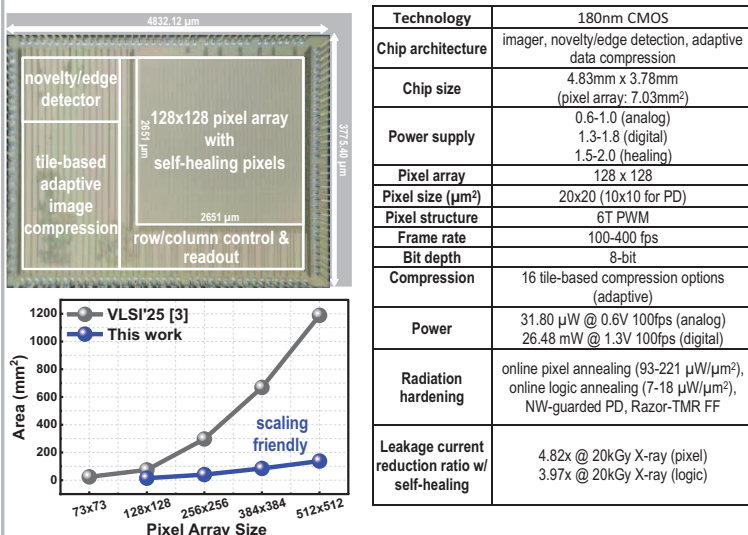


Figure 22.4.7: Die micrograph and chip summary.