# Ramen: Radiation-Aware Modeling Framework for PDK-Enabled Design and Library Characterization

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***Abstract*—Radiation-induced degradation poses a critical challenge to the reliability of space-grade integrated circuits (ICs). Existing radiation-aware models largely remain at the device level and lack direct integration with circuit or system design flows, limiting their practical use in radiation-aware IC design. To address this, this work proposes Ramen, a non-invasive radiation-aware device modeling framework that is fully compatible with commercial Process Design Kits (PDKs). Ramen accurately captures total ionizing dose (TID) and displacement damage dose (DDD), enabling early-stage evaluation at both circuit and system levels without requiring modifications to existing PDK structures. By seamlessly integrating with standard analog, mixed-signal, and digital flows, the radiation-aware models not only support SPICE-based circuit simulation but also feed into standard library characterization tools to generate radiation-aware Liberty libraries. These libraries encode dose-dependent timing, leakage, and power information, allowing radiation effects to be captured in synthesis, timing analysis, and back-end implementation. Experimental validation on a 180 nm CMOS imager under radiation stress shows that the proposed framework achieves $<15\%$ simulation errors for both analog and logic circuit, confirming the reliability of Ramen for radiation-aware IC design.**

***Index Terms*—radiation effects, compact modeling, PDK, library characterization, radiation-aware IC design**

## I. Introduction

The design of space-grade integrated circuits (ICs) faces unique challenges due to harsh radiation environments [1]–[4]. Devices across the entire chip (e.g., analog sensors, standard CMOS transistors, and logic) are susceptible to cumulative degradation from both total ionizing dose (TID) and displacement damage dose (DDD) [5]–[7]. TID leads to trapped charge buildup and interface-state generation in oxides, which induce threshold-voltage shifts and increased leakage currents [8], while DDD creates bulk defects that degrade carrier mobility and carrier lifetime [9]. Acting together, these mechanisms result in timing drifts, higher static power, and reduced signal integrity, ultimately compromising overall circuit reliability. These combined effects have been widely documented in radiation studies on advanced CMOS and imaging devices, underscoring the necessity of radiation-aware modeling and design methodologies for reliable space electronics [10], [11].

Despite extensive studies of radiation mechanisms at the device-physics level, current commercial Process Design Kits (PDKs) and standard library characterization flows still assume ideal, radiation-free devices. Existing research on radiation modeling has largely remained isolated, focusing on standalone compact models without integrating them into mainstream design flows [12]–[14]. As a result, pre-silicon simulations lack comprehensive radiation-aware support, preventing early reliability analysis of the entire design and limiting opportunities to optimize ICs for radiation-tolerant applications. Consequently, designers often encounter unexpected failures after fabrication or are forced to adopt overly conservative margins, leading to unnecessary penalties in area, power, and cost.

To address these challenges, we propose Ramen (**R**adiation-**A**ware **M**odeling for PDK-**En**abled Design and Library Characterization), a comprehensive framework that introduces radiation awareness throughout the IC design flow. Ramen performs a two-step process. First, device models (analog components such as photodiodes and standard CMOS transistors) are reconstructed by incorporating radiation-dependent parameters into existing PDK and BSIM models, enabling accurate simulation of device behavior under varying radiation conditions with minimal modifications. Second, for digital design, the reconstructed models are processed through standard library characterization EDA tools to generate radiation-aware Liberty models. Radiation parameters are treated as design variables, allowing the creation of "radiation corners" corresponding to different radiation levels and producing digital libraries that support radiation-resilient timing, power, and reliability analysis in the back-end design.

By integrating radiation effects into both device-level modeling and library characterization, Ramen provides a non-invasive, PDK-compatible solution for radiation-aware design. Unlike prior approaches that remain limited to standalone models, Ramen enables seamless adoption across analog, mixed-signal, and digital design flows, effectively bridging the gap between radiation physics and practical IC implementation workflows. This holistic integration allows designers to evaluate, optimize, and sign off radiation-tolerant circuits using their existing EDA toolchains without disruption.

## II. Related Work

Radiation-induced degradation in silicon devices has been studied for decades, with many compact models proposed to capture the effects of TID/DDD, typically focusing on threshold

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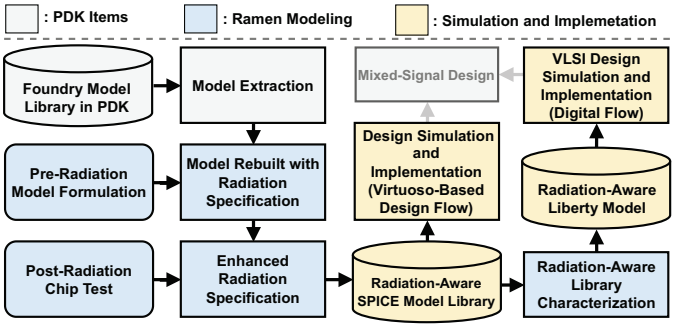



Fig. 1. Ramen framework for radiation-aware design.

voltage shifts, leakage increases, and carrier mobility degradation [13]–[17]. While informative for understanding device-level mechanisms, these works remain limited to isolated device characterization or computationally expensive TCAD simulations, making them difficult to apply in real design flows.

Simoen et al. examined multiple-gate and SOI transistors, showing how geometry influences TID sensitivity through $V_{th}$ shifts, mobility loss, and subthreshold swing degradation [13]. Despite its value for device physics, this study is confined to experimental characterization without a path to PDK integration. Antonsanti et al. investigated DDD-induced dark current in p-type deep-trench photogates, introducing a damage-factor leakage model [15], but the results remain sensor-specific and not extendable to circuit or system design. Srour and Palko developed a framework for DDD, formulating analytical expressions for defect generation and leakage scaling [16], yet this work emphasizes fundamental mechanisms rather than practical implementation. Sanchez Esqueda et al. proposed a physics-based compact model combining oxide-trapped charge and interface traps in the MOS surface potential, validated with TCAD and measurements under TID and aging [17]. While rigorous, it is device-centric, TCAD-dependent, and lacks compatibility with commercial PDKs or library characterization.

In summary, prior studies provide valuable compact models of TID and DDD effects but remain restricted to device-level use or technology-specific cases, without seamless integration into analog and digital flows. Our proposed framework, Ramen, addresses this gap by introducing a non-invasive, radiation-aware modeling methodology that augments PDK models with dose-dependent parameters and extends naturally to library characterization. This bridges radiation physics with practical design workflows, enabling pre-silicon reliability evaluation and robust implementation of space-grade ICs across analog, mixed-signal, and digital domains.

## III. Ramen Framework

As mentioned, we propose Ramen, a non-invasive framework that bridges radiation physics, compact modeling, and CMOS design flows. Ramen embeds radiation effects directly into PDK-compatible compact models, ensuring that no modification to existing foundry kits is required and preserving seamless integration with commercial EDA tools. Moreover, the generated radiation-aware models not only support accurate SPICE-level simulation for analog circuits, but can also be fed into standard library characterization tools to produce radiation-aware Liberty libraries, thereby extending radiation considerations into the digital flow. This unified capability enables both analog and digital designers to evaluate and optimize circuit reliability against radiation effects from the early design stages.

As illustrated in Fig. 1, Ramen consists of three tightly connected components (PDK items, Ramen modeling flow, and simulation and implementation flow) that form a unified radiation-aware design framework. The process begins with the foundry model library in the PDK, where all device models are based on the standard BSIM model, providing a reliable foundation for both analog and digital design. Ramen then reconstructs compact, radiation-aware models by combining empirical formulation based on radiation physics models mentioned in Section III-B with post-radiation calibration using experimental data from chip-level radiation tests in Section V-B. This integration produces precise radiation-aware SPICE models for accurate circuit-level simulations and supports iterative refinement through both simulation and measurement-based enhancement. Finally, the radiation-aware models are seamlessly incorporated into mainstream design flows. Analog design flows in Virtuoso are supported by the radiation-aware SPICE model library, enabling accurate radiation simulation at the circuit level. For digital design, the radiation-aware SPICE netlists generated by Ramen can be fed into library characterization tools to construct radiation-aware Liberty libraries, allowing VLSI designers to capture radiation-induced variations at both standard-cell and macro levels.

By enriching both analog and digital design flows with radiation-aware compact models, Ramen enables designers to co-simulate, implement, and verify radiation-tolerant circuits and systems from the early stages of design. This integration ensures that radiation effects are consistently accounted for across circuit simulation, timing analysis, and digital implementation, facilitating end-to-end design of reliable ICs.

### A. Radiation-Aware Parameter Integration

In this work, we implement a comprehensive radiation-aware parameter integration workflow using SKILL scripts, as summarized in Algorithm 1. The process begins by extracting transistor and device models from the commercial PDK and creating corresponding Ramen models, ensuring a one-to-one mapping between the original PDK models and the reconstructed models. Each Ramen model initially inherits all baseline parameters from its PDK counterpart. Radiation-specific parameters, such as radiation dose, are then introduced through Cadence Virtuoso's Component Description Format (CDF) functionality. Callback functions, constructed by combining native PDK functions with Ramen-defined extensions, process these radiation parameters and translate them into device-level effects, including threshold voltage shifts and leakage current increases. The updated parameters are subsequently propagated into the Ramen models, yielding radiation-aware BSIM models that faithfully reflect radiation-induced degradations while remaining fully compatible with SPICE simulation and standard library characterization flows.

**Algorithm 1** Radiation-Aware Parameter Integration in Ramen

**Require:** Device type $T$; Radiation condition $R$ (e.g., total ionizing dose $D$ [Gy])

**Ensure:** Radiation-aware BSIM4v5 model $M_{rad}$ with compact model parameters $P_{rad}$

**Model Extraction:**

  Extract baseline compact model parameters $P_{pdk}$ from the commercial PDK (e.g., the values/initial values of $V_{th}$, $I_{leak}$, $\mu$, etc. from PDK models).

**Radiation Parameter** $P_{pdk} \rightarrow P_{rad}$ **Mapping:**

  Based on dose $D$, compute radiation-induced parameter shifts:

    Threshold voltage shift:

      $V_{th,rad} \leftarrow V_{th} + f_{\mathrm{rad}}(D)$ ▷ $f(\cdot)$: models dose-dependent $V_{th}$ shift due to oxide-trapped charge and interface traps

    Leakage current increase:

      $I_{leak,rad} \leftarrow I_{leak} \times g_{\mathrm{rad}}(D)$ ▷ $g(\cdot)$: captures dose-dependent enhancement of junction or STI leakage

**Model Reconstruction:**

  Use Virtuoso CDF callback functions to dynamically update $P_{pdk}$ with $P_{rad}$.

  Store updated parameters into Ramen-enhanced BSIM model $M_{rad}$.

  Ensure $M_{rad}$ remains SPICE-compatible for circuit simulation and Liberty library characterization.

**return** $M_{rad}$

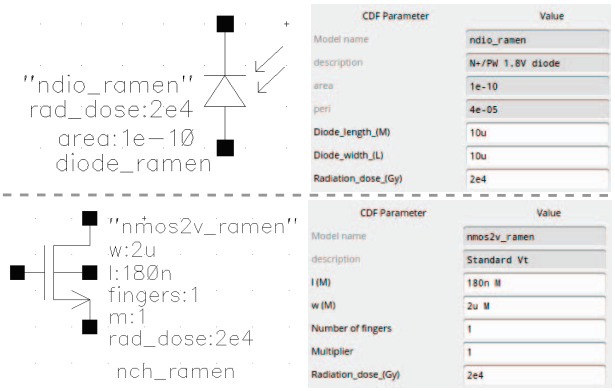



Fig. 2. Examples of Ramen models.

Two typical devices (a diode and an NMOS) are shown as examples in Fig. 2. Based on the original PDK, we extend the radiation dose attribute through CDF, and its value is converted via CDF-based callback functions into electrical parameter shifts such as increased leakage current or threshold voltage variation. The detailed formulations are presented in Section III-B. Therefore, this framework allows seamless integration of radiation effects into PDK-compatible models, forming a complete radiation-aware modeling environment suitable for robust circuit simulations under radiation exposure.

### *B. Compact Model Formulation*

To establish the relationship between radiation dose and specific parameters in BSIM models, we denote total radiation dose by $D$ (Gy or krad($SiO_2$), 1 krad = 10 Gy). The CDF callback maps $D$ into compact-model parameter shifts that are written back to the PDK BSIM/SPICE cards. Under TID stress, the dominant leakage mechanism in CMOS photodiodes arises from Shockley–Read–Hall (SRH) generation at the STI/Si sidewall depletion region [18]. According to Goiffon et al. [19], the TID-induced dark current in photodiode can be modeled as:

$$I_{\mathrm{dark}} = q\, W_{\mathrm{STI}}(V_R, D)\, P_j\, \sigma_{\mathrm{eff}}\, v_{\mathrm{th}}\, k\pi\, T\, D_{\mathrm{it}}(D)\, n_i(T), \quad (1)$$

where $q$ is the elementary charge, $W_{\mathrm{STI}}$ is the depletion width at the STI/Si interface (increasing with both reverse bias $V_R$ and dose $D$), $P_j$ is the diode perimeter, $\sigma_{\mathrm{eff}}$ is the effective capture cross-section, $v_{\mathrm{th}}$ is the thermal velocity, $k$ is Boltzmann's constant, $D_{\mathrm{it}}(D)$ is the interface trap density (proportional to $D$), $n_i(T)$ is the intrinsic carrier concentration, and $T$ is temperature. In practice, the radiation-induced dark current in Eq. (1) is mapped to the sidewall junction reverse saturation current density parameter (`JSW`) of the BSIM body-diode model. The measured dose-dependent dark current is normalized to the junction perimeter to obtain an equivalent increment $\Delta$`JSW`, which is directly written into the model card without modifying BSIM equations. This approach consistently captures irradiation-induced edge leakage within the existing PDK framework. The dose-aware update is embedded in CDF callback functions, allowing parameter shifts to be dynamically evaluated and injected into BSIM model, thus yielding a fully radiation-aware device for circuit-level simulation.

Regarding MOSFET, under TID, oxide-trapped (ot) charge and interface traps (it) jointly shift the threshold voltage. Following the rebound compact law in [12], the shift is

$$\begin{aligned}\Delta V_{th}(D) &= \Delta V_{\mathrm{ot}}(D) + \Delta V_{\mathrm{it}}(D) \\ &\approx \frac{\lambda}{\ell}\, F_{\mathrm{ot}}\, A_d\, D\, \ln\!\left(\frac{D}{D_R}\right) \Big/ C_{ox},\end{aligned} \quad (2)$$

where $C_{ox}$ is the gate-oxide capacitance per unit area, $F_{\mathrm{ot}}$ the deep-oxide trap efficiency, $A_d = K_g\, t_{ox}\, \eta(E_{ox})$ (with $K_g$ the $e$–$h$ pair generation constant, $t_{ox}$ the oxide thickness, and $\eta$ the field-dependent yield), $\lambda/\ell$ the tunneling parameter ratio, and $D_R = P t_{\min} \exp[\ell(1-\beta)/\lambda]$ the rebound dose set by dose rate $P$, minimum tunneling time $t_{\min}$, and a dimensionless factor $\beta$. Equation (2) captures the initial oxide-charge–driven shift and its later compensation by interface traps (rebound).

The OFF-state leakage current is obtained by inserting $V_{th}(D) = V_{th0} + \Delta V_{th}(D)$ into the diffusion–drift compact model. $V_{th0}$ denotes the baseline threshold voltage from the original PDK model (i.e., the pre-radiation value). An useful asymptote is subthreshold diffusion ($V_{th}(D) > 0$)

$$I_{\mathrm{OFF}}(D) \;\approx\; \frac{W}{L}\, q\, \mu_0\, C_D\, \varphi_T^2 \left(\frac{T_0}{T}\right)^{3/2} \exp\!\left[-\frac{V_{th}(D)}{m(D)\, \varphi_T}\right], \quad (3)$$

where $W/L$ is device geometry, $\mu_0$ the low-field mobility, $C_D$ the depletion capacitance density, $\varphi_T = kT/q$, and $m(D) = 1 + \big(C_{it}(D) + C_D\big)/C_{ox}$ is the subthreshold factor ($C_{it} = q^2 D_{it}$).

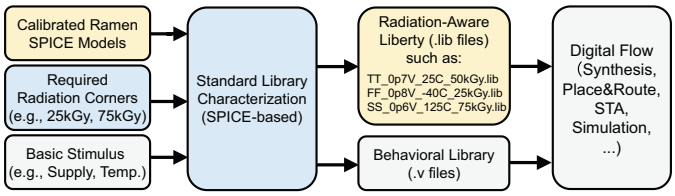



Fig. 3. Library characterization flow with Ramen for VLSI design.

Equations (2)–(3) provide a direct dose-to-parameter mapping. $\Delta V_{th}(D)$ governs the exponential OFF leakage in subthreshold, while Eq. (3) serves as the analytical basis showing how temperature and dose jointly affect leakage scaling. In implementation, the CDF callback evaluates $\Delta V_{th}(D)$ from Eq. (2) and updates the BSIM entry `VTH0`, so that threshold-voltage shifts are directly embedded in the model card. Subthreshold degradation, expressed via $m(D)$, is reflected as an effective adjustment of `NFACTOR`-related parameters to reproduce the degraded swing behavior.

With this mapping strategy, radiation-induced shifts in parameters such as `VTH0`, `NFACTOR`, and `JSW` are systematically evaluated and updated via the CDF callback, allowing the compact model to accurately capture dose-dependent leakage behaviors of both MOSFETs and diodes, all while preserving the original BSIM equation framework.

### C. Library Characterization Flow with Ramen

From the calibrated radiation-aware SPICE models, Ramen extends the standard library characterization flow to include radiation-defined corners via original standard cell library. For each cell, SKILL/CDF scripts export SPICE-compatible radiation-aware netlists at selected doses (e.g., 25kGy, 75kGy). Only a few parameters in the model card are modified, while the netlist remains unchanged. These dose points are treated as radiation corners, augmenting conventional PVT conditions and producing composite corners such as `TT_0p7V_25C_50kGy`, `SS_0p6V_125C_25kGy`, and `FF_0p8V_-40C_75kGy`.

Standard characterization tools (e.g., Cadence Liberate, Synopsys Primelib) then perform SPICE-level analyses at each corner, generating delay/transition tables, leakage power, and internal power metrics. The outputs are radiation-aware Liberty libraries, where dose-induced variations are directly encoded in cell_rise/fall, transition, leakage, and power tables. Because Ramen SPICE models preserves native BSIM syntax, these models can be inserted into the characterization flow without modifying either the foundry PDK or EDA tools, thus radiation parameters are simply passed through the SPICE netlists.

The resulting Liberty libraries integrate seamlessly into digital flows for synthesis, timing sign-off, and place-and-route (PnR). Designers can analyze and optimize circuits across both PVT and radiation corners. In practice, shifts in `VTH0` and `NFACTOR` manifest as increased delay and degraded transitions; diode and NMOS leakage appear in leakage power; and variations in `JSW` directly alter junction edge leakage, which in turn impacts photocurrent behavior in sensor front-ends. This enables end-to-end dose-aware design closure using existing industrial EDA toolchains.

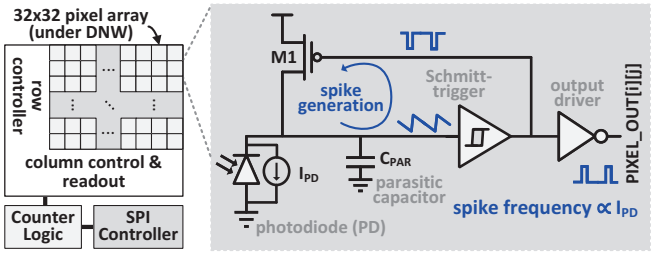



Fig. 4. Imager with spike-based pixel for Ramen verification.

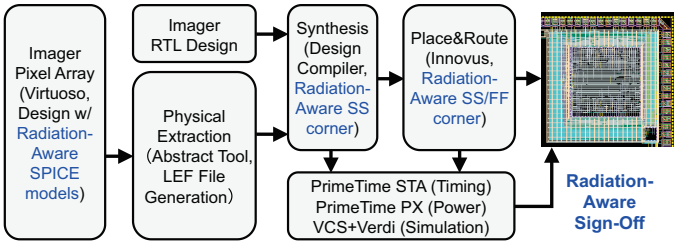



Fig. 5. Ramen-based radiation-aware imager implementation.

## IV. A Custom CMOS Imager for Ramen Validation

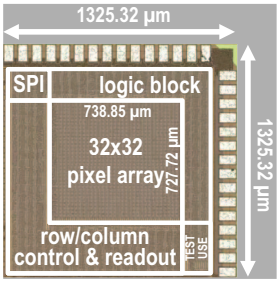
### A. CMOS Imager Architecture

To validate Ramen, we implement a spike-based imager (Fig. 4). In this architecture, the photodiodes and associated front-end circuits are intentionally left without upper-layer metal coverage, making them directly exposed to radiation. This layout facilitates controlled irradiation experiments, where the impact of radiation on device characteristics can be readily observed. Another advantage of this architecture is its spike-based signaling. Instead of generating continuous analog outputs, each pixel produces spikes whose frequency is proportional to the photocurrent. These spikes can be directly accumulated by simple counter logic, enabling efficient data collection and statistical evaluation.

At the system level, the prototype consists of a 32×32 pixel array controlled by row and column drivers, with column readout circuits, counter logic, and an SPI controller for data transfer. Within each pixel, the photodiode generates a photocurrent ($I_{PD}$) that charges the parasitic capacitor ($C_{PAR}$). Once the capacitor voltage reaches the threshold of the Schmitt trigger, a pulse is generated, which is further buffered by an output driver. The output spike frequency is therefore linearly proportional to $I_{PD}$, and hence to the incident light intensity. This compact, event-driven pixel architecture provides an efficient platform for radiation testing and serves as a practical vehicle for verifying radiation-aware modeling and simulation enabled by Ramen.

### B. Ramen-based Radiation-Aware Imager Implementation

Based on the Ramen framework, we implement the imager as mentioned in Section IV-A. The pixel array is directly simulated and designed in Virtuoso using the radiation-aware SPICE models generated by Ramen, while the EDA tool, Cadence Abstract, is employed to extract LEF and other physical views for digital PnR. Subsequently, Ramen, together with commercial characterization tools (Synopsys PrimeLib), is used to generate radiation-aware TT, SS, and FF -corner libraries.




| Specification | Value |
|---|---|
| Process | 180nm CMOS |
| Supply Voltage [V] | 0.6–0.8 |
| Frequency [MHz] | 1MHz @ SPI<br>1-10MHz @ Others |
| Chip Area [mm$^2$] | 1.756 |
| Core Area [mm$^2$] | 1.312 |
| Pixel Array Area [mm$^2$] | 0.538 |
| Power [mW] | 0.1-2.6 |
| Pixel Array | 32×32 |
| Pixel Structure | Spike |
| Pixel Size [µm$^2$] | 20×20 |
| Photodiode [µm$^2$] | 10×10 |
| Bit-depth | 32-bit (counter) |

Fig. 6. Die micrograph and summary.

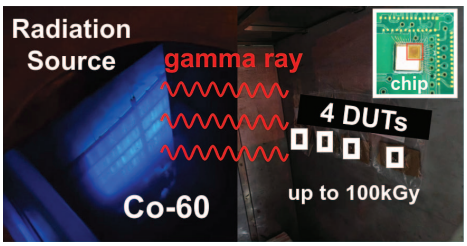



Fig. 7. Experimental setup for Co-60 $\gamma$ ray irradiation.

Specifically, the SS corner (0.6 V, 125°C, and 100 kGy) is adopted for logic synthesis using Synopsys Design Compiler, whereas both this SS corner and an FF corner (0.8 V, 0°C, and 25 kGy) are employed for PnR using Cadence Innovus. In this flow, the SS corner is applied to constrain setup timing, while the FF corner is used for hold timing constraints. Final timing verification is performed with Synopsys PrimeTime, where the relatively low operating frequency (below 10 MHz) ensured timing closure with sufficient margin. Power estimation is conducted with Synopsys PrimeTime PX to complete the digital sign-off process. In addition, functional pre- and post-simulation are performed using Synopsys VCS, with waveform analysis and debugging supported by Synopsys Verdi.

### C. Imager Specification

Based on the implementation flow described in Section IV-B, an imager is designed and fabricated in a 180-nm CMOS technology node, as illustrated in Fig. 6. The resulting chip features a total die area of 1.756 mm$^2$ with an active core area of 1.312 mm$^2$. The 32×32 spike-based pixel array (0.538 mm$^2$) is surrounded by row/column control, readout, logic, and SPI blocks. Each pixel measures $20 \times 20\,\mu$m$^2$ with a $10 \times 10\,\mu$m$^2$ photodiode. The chip operates at 0.6–0.8 V, supports 1–10 MHz frequency (1 MHz at SPI), consumes 0.1–2.6 mW, and integrates a 32-bit counter for digital readout.

## V. Experiment and Evaluation

### A. Experimental Setup

To evaluate the effectiveness of Ramen, four DUTs are subjected to continuous Co-60 gamma-ray irradiation up to a total dose of approximately 100 kGy, as illustrated in Fig. 7. Co-60 is selected because it provides a well-established and standardized radiation source that closely emulates the cumulative ionizing effects. Throughout the irradiation process, key device parameters (the pixel spike frequencies and leakage currents in digital and analog parts) are periodically measured at four monitoring points to capture the degradation behavior under increasing radiation stress, as summarized in Table I.

TABLE I
Dose Monitoring During Co-60 Irradiation for Four DUTs.

| Stage | Accumulated Dose (kGy) | Time (s) | Average Rate (Gy/s) |
|---|---|---|---|
| 1 | 33.0 | 21,780 | 1.515 |
| 2 | 68.2 | 41,580 | 1.640 |
| 3 | 81.3 | 51,480 | 1.579 |
| 4 | 102.1 | 61,380 | 1.663 |

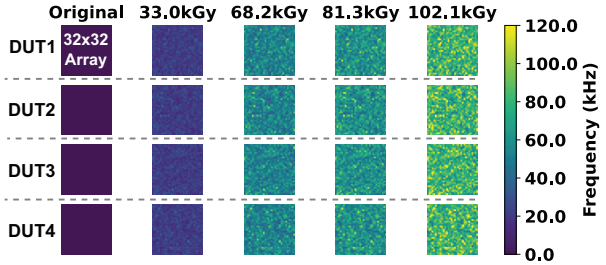



Fig. 8. Spike frequency of 4 DUTs under different gamma-ray dose.

TABLE II
Analysis of Spike Frequency under Different Total Doses.

| Dose (kGy) | Spike Frequency (kHz) | | Relative Error |
|---|---|---|---|
| | Simulation | Measurement* (4 DUTs) | |
| 33.0 | 22.32 | 24.29/24.05/20.38/21.84 | 2.15-8.83% |
| 68.2 | 54.08 | 55.73/55.05/49.66/53.31 | 1.42-8.17% |
| 81.3 | 62.09 | 69.15/59.90/65.72/61.88 | 0.34-11.37% |
| 102.1 | 77.01 | 79.83/77.68/88.17/81.74 | 0.87-14.49% |

*Mean spike frequency of pixel array.

TABLE III
Leakage Current Comparison of Digital and Analog Circuits under Different Total Doses @ 0.7V 25°C.

| Dose (kGy) | Analog Leakage (uA) | | Digital Leakage (uA) | |
|---|---|---|---|---|
| | Simulation | Measurement Error | Simulation | Measurement Error |
| 33.0 | 34.98 | 8.41-8.52% | 22.68 | 2.15-11.35% |
| 68.2 | 82.79 | 3.00-8.07% | 34.32 | 1.62-7.45% |
| 81.3 | 93.84 | 0.36-11.22% | 45.40 | 0.72-9.83% |
| 102.1 | 114.73 | 0.85-14.34% | 59.63 | 4.56-13.03% |

### B. Ramen Validation and Analysis

Fig. 8 illustrates the measured spike frequency distributions of 4 DUTs under different $\gamma$-ray doses ranging up to 100 kGy. Each subplot corresponds to a 32×32 pixel array, showing the progressive degradation in spike activity as dose increases. As dose accumulates, the spike frequency is increased due to radiation-induced leakage increase and threshold-voltage shifts. This validates the sensitivity of the pixel array to radiation and provides a baseline for simulation-to-measurement correlation.

Table II compares the measured spike frequencies of the four DUTs against Ramen-based simulation results at nominal operating conditions (0.7 V, 25°C). The results show that the proposed framework accurately predicts frequency degradation across the full irradiation range. At lower doses (33–68 kGy),

TABLE IV
COMPARISON OF RADIATION-AWARE MODELING APPROACHES.

| Item | Li et al. [14] | Antonsanti et al. [15] | Srour et al. [16] | Esqueda et al. [17] | This work (Ramen) |
|---|---|---|---|---|---|
| **Target Device** | General CMOS | p-type deep-trench photogate | Bulk Si devices | Bulk/SOI MOS | General CMOS (MOS, diodes, sensors) |
| **Radiation Mechanism** | TID | DDD | DDD | TID + aging | TID + DDD (extensible) |
| **Modeling Level** | Physics-based model (analytical + Verilog-A) | Experimental + empirical model | Physics/mechanism model (no SPICE) | Physics-based compact model | Compact model reconstruction in PDK |
| **Need for TCAD** | No | No | No | Yes | No (CDF + calibration) |
| **PDK Compatibility** | Yes (Verilog-A add-on) | No | No | No | Yes (SPICE reconstruction) |
| **EDA Flow Integration** | Partial (SPICE-level only) | No | No | No | Yes (Analog + Digital flows) |
| **Library Characterization** | No | No | No | No | Yes (Radiation-aware Liberty files) |
| **Scope of Applicability** | Device-level + SPICE simulation | Sensor-specific (dark current, RTS) | Fundamental mechanism studies | Device-level TCAD | Full-chip design (analog, mixed-signal, digital) |

the deviation between simulation and measurement is modest (2–8%), while even at the highest evaluated dose (102 kGy), the maximum error remains below 14.5%. Such accuracy confirms that Ramen effectively captures radiation-induced circuit-level behavior while keeping prediction errors within acceptable limits for pre-silicon evaluation.

Since the system operates at low frequency (10 MHz), only the leakage current can be readily observed. Table III summarizes the leakage current of both analog and digital circuits under different dose conditions at 0.7 V and 25°C. The simulation data for the analog domain are obtained directly from Cadence Virtuoso, while the digital domain results are derived from radiation-aware Liberty files generated through library characterization and subsequently analyzed via Synopsys PrimeTime. Importantly, Ramen framework is calibrated through parameter fitting using post-radiation measurement data from the fabricated imager, ensuring that dose-dependent effects are incorporated into the compact models as faithfully as possible. As a result, across all radiation levels, the Ramen-based simulation results remain in close agreement with measurements, with deviations typically within 2–14%. Such bounded errors demonstrate that the proposed framework can reliably capture dose-dependent leakage variations for both analog and digital circuits. On the other hand, this variation may also arise from PVT variations and experimental errors. By measuring basic diodes and transistors as test structures in advance, similar accuracy is expected for pre-silicon designs.

### C. Comparison with Radiation-Aware Modeling Approaches

Compared to prior radiation-aware modeling approaches summarized in Table IV, our proposed Ramen framework offers clear advantages in terms of practicality and compatibility with IC design flows. Li et al. [14] introduced physics-based models with Verilog-A extensions that can be added to commercial PDKs, but their applicability is limited to SPICE-level simulations and does not extend to full EDA flows. Antonsanti et al. [15] developed sensor-specific models of displacement-damage effects (e.g., dark current, random telegraph signal (RTS) degradation), yet the approach remains experimental and cannot be generalized to broader circuit applications. Srour et al. [16] provided a comprehensive analytical framework for displacement-damage mechanisms, but the results are restricted to device-level studies without compact-model or library integration. Esqueda et al. [17] advanced a TCAD-dependent compact model that incorporates oxide-trapped charge and interface traps, though this method lacks compatibility with commercial PDKs and practical EDA toolchains. In contrast, Ramen reconstructs compact models directly within existing PDKs, incorporates both TID and DDD effects (with extensibility for other mechanisms), and produces radiation-aware Liberty libraries. This integration enables seamless use in analog, digital, and mixed-signal flows, ensuring end-to-end radiation-aware design that previous approaches cannot provide.

## VI. CONCLUSION

In this work, a radiation-aware modeling framework, Ramen, is proposed that augments commercial PDKs with compact models incorporating cumulative radiation effects. Ramen provides a non-invasive methodology that preserves the native BSIM syntax and integrates seamlessly into standard EDA workflows. Through SKILL-based extraction and CDF callbacks, radiation dose is translated into parameter perturbations such as threshold-voltage shifts, and leakage-current increase, enabling the construction of radiation-aware SPICE models. Beyond circuit-level analysis, Ramen supports full-flow digital implementation by generating radiation-aware Liberty libraries via standard characterization tools. This capability extends radiation modeling from individual devices to system-level VLSI design, allowing radiation corners to be incorporated naturally into VLSI design flow. In this way, Ramen bridges radiation physics and practical design flows across analog, mixed-signal, and digital domains. Experimental validation on a 180nm CMOS spike-based imager under Co-60 irradiation confirmed that Ramen accurately predicts radiation-induced degradation trends, with modeling errors kept within 15%. Ultimately, Ramen enables designers to build radiation-aware circuits without modifying foundry PDKs, offering an effective and practical path toward end-to-end radiation-aware IC design.

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