A 292.2-to-321.4-GHz Synchronized Source Generator With −58.7-dBc Spurious Tone and 136.7-fs_{rms} Integrated Jitter in 22-nm CMOS Technology

Yuan Liang, *Member, IEEE*, Shiqi Chen, Huizi Zhang, Longyang Lin, *Senior Member, IEEE*, Quan Cheng, *Member, IEEE*, and Masanori Hashimoto, *Senior Member, IEEE*

***Abstract*—This article introduces a synchronized source generator operating from 292.2 to 321.4 GHz. It involves a millimeter-wave (mmW) phase-locked loop (PLL) cascaded with an 8× frequency multiplier chain. A complementary ripple-neutralized phase detector (CRN-PD) is introduced in the PLL for ripple compensation during phase alignment, aiming to reduce the PLL spurious tone level. A calibration scheme enhances the robustness of ripple neutralization. The CRN-PD is further developed to support frequency and lock detection (LD). Another calibration scheme is introduced to capture the optimal locking point of the dynamic-latch-based prescaler, eliminating the need for external tuning. The source generator was implemented in a 22-nm CMOS technology, achieving −110.6- and −86.1-dBc/Hz phase noise at a 1-MHz offset, respectively, at 39.8 and 307.7 GHz, indicating the integrated jitter of 63.0 and 136.7 fs_{rms} (10 kHz–100 MHz). The spurious tone level is −58.7 dBc, normalized to 320 GHz. The signal source generates a peak output power of −8.6 dBm, and it consumes 216.2 ~ 249.5 mW of power from 0.9-/1.8-V power supplies.**

***Index Terms*—Calibration, CMOS phase-locked loop (PLL), phase detector (PD), source generation, terahertz (THz).**

I. Introduction

RECENT endeavors regarding integrated components and circuits working in the terahertz (THz) frequency range have enabled applications such as rotational spectroscopy imaging [1], [2], 300-GHz broadband wireless links [3], [4], and THz radar and sensing [5], [6]. In these systems, a wide frequency tuning range (FTR), low phase noise, and low-spurious-tone synchronized source generator are essential to enhance data rates to hundreds of gigabits per second or to boost detection sensitivity to < −100 dBm [7], [8]. Traditionally, THz source generators have been implemented using compound semiconductors [9], [10], [11] or SiGe BiCMOS technologies [12], [13], [14]. With the continuous scaling of CMOS transistors, CMOS technology has been considered the ultimate low-power, low-cost, and digital-intensive solution for supporting versatile THz applications.

Phase-locked loop (PLL)–based synchronized THz source generators have been examined. A 283-GHz synchronized signal source utilizing a triple-push voltage-controlled oscillator (VCO) measured −53.5 dBc/Hz at a 100-kHz offset [15]. A triple-push VCO was also employed in a 300-GHz frequency synthesizer [16], achieving a 7.9% locking range, but it consumed 376 mW of power with a peak dc-to-RF efficiency of 0.01%. A cascaded frequency synthesizer operating at 560 GHz has achieved a locking range of 3.75% [17], but it required a pair of triple-push Colpitts VCOs for decoupling the parasitic loading. By adopting harmonic mixing topology, a frequency synthesizer attained a wide FTR from 208 to 255 GHz [18]. Yet, it consumed 1.3 W of power. A subsampling PLL (SS-PLL) achieved sub-100-fs_{rms} integrated jitter at 270.72 GHz [19], but its spurious tone level was −26.8 dBc. By optimizing the output power efficiency of the VCO, an SS-PLL achieved −6-dBm output power at 110 GHz [20], but its FTR was limited to ~2 GHz. A 300-GHz SiGe BiCMOS source generator integrating an 80-GHz VCO was utilized, achieving 122-fs_{rms} integrated jitter and a normalized −50-dBc/Hz spurious tone [13], but it consumed more than 370 mW of power. A cascaded injection-locked PLL attained ~355 fs_{rms} jitter at 307 GHz [21], but it required cumbersome frequency adjustment for the injection-locked frequency multiplier.

In light of previous work, a THz source generator architecture is illustrated in Fig. 1, to balance integrated jitter, spurious tone level, FTR, and power consumption. Such an architecture raises several design challenges. As the frequency

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Yuan Liang and Shiqi Chen are with the School of Electronics and Communication Engineering, Guangzhou University, Guangzhou 510006, China (e-mail: yliang017@e.ntu.edu.sg; sqchen@e.gzhu.edu.cn).

Huizi Zhang and Longyang Lin are with the School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China.

Quan Cheng and Masanori Hashimoto are with the Department of Informatics, Kyoto University, Kyoto 606-8501, Japan (e-mail: ivin.chengquan@gmail.com; hashimoto@i.kyoto-u.ac.jp).

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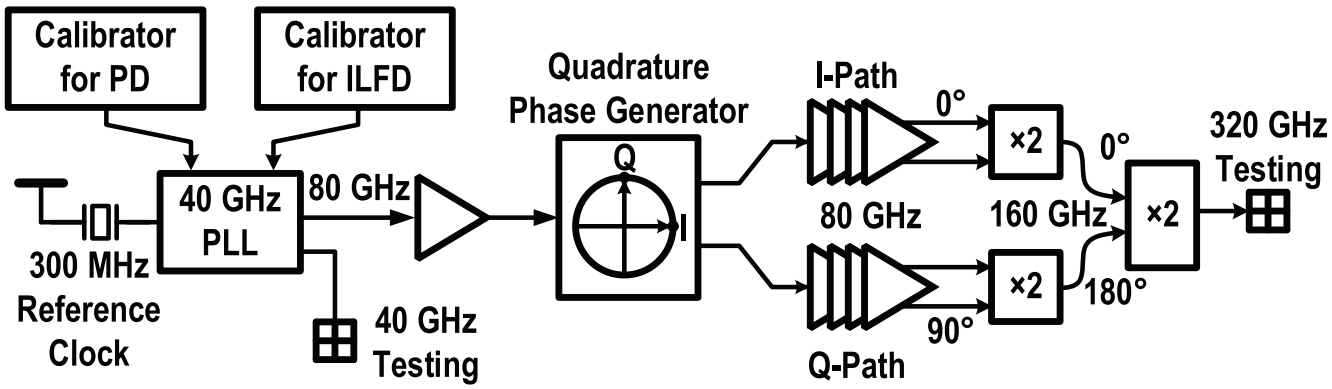

Fig. 1. Architecture of the 320-GHz synchronized source generator realized in CMOS technology.

multiplication factor is 8, the PLL spurious tone must be amplified by a factor of 20log (8) =18 dB. If the desired spurious tone is below −55 dBc at the 320-GHz output, it must be −73 dBc or lower at the PLL output while maintaining low-jitter performance. Moreover, since the oscillation frequency of 40 GHz is still high for the process, the millimeter-wave (mmW) prescaler, based on low-power dynamic-latch topology, necessitates frequency alignment and therefore calibration.

This article describes an energy-efficient, low-spurious-tone, and low-jitter 320-GHz source generator implemented in a 22-nm CMOS process. A complementary ripple-neutralized phase detector (CRN-PD) is introduced for mutual spurious tone cancellation without consuming additional power. Considering inherent device mismatch and process, voltage, and temperature (PVT) variations, a calibration scheme is introduced to enhance the effectiveness of ripple neutralization. The CRN-PD is further developed to support frequency alignment and VCO lock detection (LD). Furthermore, to achieve low-power and robust operation, an additional calibration scheme is introduced specifically for capturing the optimal injection-locked point of the mmW injection-locked frequency divider (ILFD), thereby eliminating the need for external fine-tuning.

This article is organized as follows. Section II introduces the concept of ripple neutralization, and its circuit realization and calibration are elaborated in Section III. Section IV discusses the calibration for the prescaler, followed by a discussion on PLL implementation and the frequency multiplier. Measurement results are provided in Section V. Finally, Section VI concludes this article.

II. Concept of Ripple Neutralization

A. PD in mmW PLLs

As the quality factor (Q-factor) of inductor coils is low (i.e., ~15) at mmW frequencies, a wide PLL loop bandwidth (f_{BW}) is preferred for dampening more VCO phase noise. However, raising the PLL corner frequency diminishes the level of attenuation to spurious tones. Thus, obtaining low PLL phase noise naturally contradicts the requirement for a small spurious tone. Since the spurious tone level is highly associated with PD topology, a PD capable of decoupling spurious tone suppression and f_{BW} is desired. With this achievement, f_{BW} can be extended to suppress more VCO phase noise without raising the spurious tone level.

B. State-of-the-Art PD Topologies

Low-noise and low-spurious-tone PLLs have been reported recently. The SS-PLL has been recognized as achieving the best figure of merit (FoM) among all PLL architectures. It benefits from high PD gain (K_{PD}) and low power consumption since the subsampling operation does not need a divider chain. Random jitter associated with the PD is described in the following equation [22]:

$$\text{Noise}_{PD} = 20\log\left(\frac{2\cdot\pi\cdot I_{N.PD}\cdot N}{K_{PD}}\right) \quad (1)$$

where $I_{N.PD}$ denotes the PD output noise current and N denotes the PLL division ratio. A high K_{PD} allows the reference phase noise to become dominating, leading to low jitter in the PLL. However, SS-PLLs are prone to binary frequency shift keying (BFSK) modulation, clock feedthrough, as well as charge injection [22]. The mmW SS-PLLs commonly exhibit a high spurious tone level of ~ −40 dBc. Furthermore, since the acquisition range of an SSPD is small, a frequency-tracking loop (FTL) is mandatory.

On the other hand, a sampling PLL (S-PLL) amplifies the divider noise by N^2, but it is more robust than SS-PLLs since its PD acquisition range is N times larger, possibly obviating the need for an FTL. By sampling the steep clock edge of the divider output, K_{PD} of an SS-PLL is also high enough to render the PD noise negligible. The BFSK modulation effect is negligible since the PD has no direct path to modulate the VCO tank. However, S-PLLs heavily rely on loop filters (LFs) for dampening spurious tones. For example, the main/secondary sampling filter (MSSF) adopts a harmonic trap after the PD to attain ~20-dB attenuation, but this degrades the loop margin [23]. Moreover, external calibration is required. First-order RC filters have been adopted in [24], [25], and [26]. Since these PLLs are Type-I PLLs, the RC corner also determines their f_{BW}, phase margin, and PD acquisition range. Other PLLs utilizing low-intrinsic-noise PDs, such as mixer PD [27], AND-gate PD [28], and XOR-gate PD [29], also rely on small RC

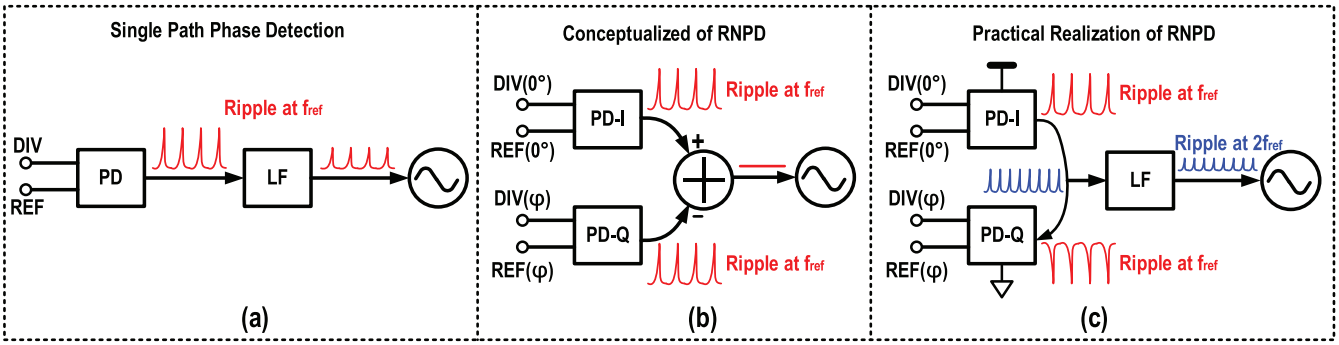

Fig. 2. (a) Single-path PD, (b) concept of ripple neutralization, and (c) practical implementation ripple neutralization with current circulation.

corner frequencies and therefore suffer from the same issues as S-PLLs.

C. Concept of Ripple Neutralization

The effort to suppress spurious tone levels in traditional PDs is coupled with PLL phase noise, loop stability, and PD acquisition range. Consequently, it is desirable not to rely on a small f_{BW} for spurious tone suppression and to instead rely on the PD itself to attenuate it. Considering this, a PD capable of spurious tone neutralization is introduced.

PLL spurious tones mainly stem from the ripple at the VCO control line voltage (V_{ctrl}) and voltage ringing at the power lines. The latter can be mitigated by regulating voltage (Section III-C) and separating power lines among each circuit block, whereas the former is determined by the PD characteristics. Fig. 2(a) illustrates spurious tone generation due to voltage ripple at the PD output, which periodically modulates V_{ctrl}. The LF afterward aims to attenuate the ripple voltage to some extent, but, as mentioned, its corner frequency couples ripple suppression with PLL phase noise. To relax this tradeoff, a redundant path for phase detection [Fig. 2(b)] is introduced. If the two PDs are fully symmetrical, the ripple produced by the original PD (i.e., PD-I) can be effectively neutralized by the redundant PD (i.e., PD-Q). Since ripple suppression now relies on mutual cancellation rather than traditional filtering, the spurious tone level becomes independent of f_{BW} and is therefore decoupled from the PLL phase noise performance.

As ripple neutralization should not impede normal PLL operation, the input phase for each PD must be unequal. In a heterodyne receiver, mixing images are eliminated by adopting a pair of mixers driven by a quadrature signal source, leaving only the intermediate frequency term. Inspired by this concept, a phase offset $\varphi = 90^\circ$ is adopted in Fig. 2(b) for performing ripple neutralization. Meanwhile, the PD in each path functions the same way as a mixer. Mixer PDs are widely used in low-jitter frequency synthesizers [14], [27]. However, as explained in Section III-A, using a single mixer for phase detection generates a large ripple. In [27], the spurious tone was −37 dBc.

The architecture in Fig. 2(b) has to involve two PDs, which doubles the power consumption. It is therefore transformed as shown in Fig. 2(c), where the current drawn by PD-I is reused by PD-Q, maintaining the same current as the single-path version. This arrangement calls for a complementary implementation of Fig. 2(b), resulting in the CRN-PD. Unlike mixer PDs, where the ripple voltage is suppressed by the subsequent LF, the CRN-PD suppresses the ripple in the current domain by neutralizing each ripple current produced by the respective PD.

D. Mismatch Effect

Like other complementary circuits, the CRN-PD suffers from worse device mismatch compared with Fig. 2(b), weakening the effectiveness of ripple neutralization. In this regard, an LF is still required to dampen the leakage current. Since phase comparison occurs twice within one reference cycle (i.e., $1/f_{ref}$) due to quadrature operation, as opposed to once in traditional mixer PDs, the ripple frequency undergoes an inherent frequency doubling. This characteristic alleviates the dilemma of LF, as the corner frequency can be allocated at $\sim 2f_{ref}$, which is orders of magnitude higher than f_{BW}, thereby imposing lesser impact on phase margin.

Both amplitude and phase mismatches exacerbate ripple neutralization, raising the spurious tone level. By applying a pair of square pulses, denoting the reference clock and the divider output, spurious tones associated with amplitude mismatch (ΔA) and phase mismatch ($\Delta\theta$) can be evaluated by the following:

$$\text{Spurious Tone}\Big|_{2f_{ref}} \approx 20\log\left[\frac{\frac{K_{VCO}K_{PD}}{2f_{ref}/f_{PD}}\frac{A_2}{2f_{ref}/f_{LF}}}{2\pi\times f_{ref}}\sqrt{\left(\frac{\Delta A}{A_2}\right)^2+\frac{\Delta\theta^2}{2}}\right] \quad (2)$$

where K_{VCO} represents the VCO gain; f_{PD} and f_{LF} denote the corner frequencies of the PD and LF, respectively; and A_2 is the ripple amplitude of the second harmonic. As observed, the second tone suffers from 12-dB more attenuation than the fundamental tone. f_{ref} and K_{VCO} are predefined systematic parameters, and K_{PD} cannot be arbitrarily small considering the PD acquisition range and phase noise. Meanwhile, f_{PD} and f_{LF} cannot be too small, for maintaining loop stability. The remaining effort hereby lies in minimizing device mismatches.

III. CRN-PD and Calibration

A. Circuit Realization of CRN-PD

Fig. 3(a) and (b), respectively, depicts an all-pMOS and an all-nMOS realization of the differential PD performing

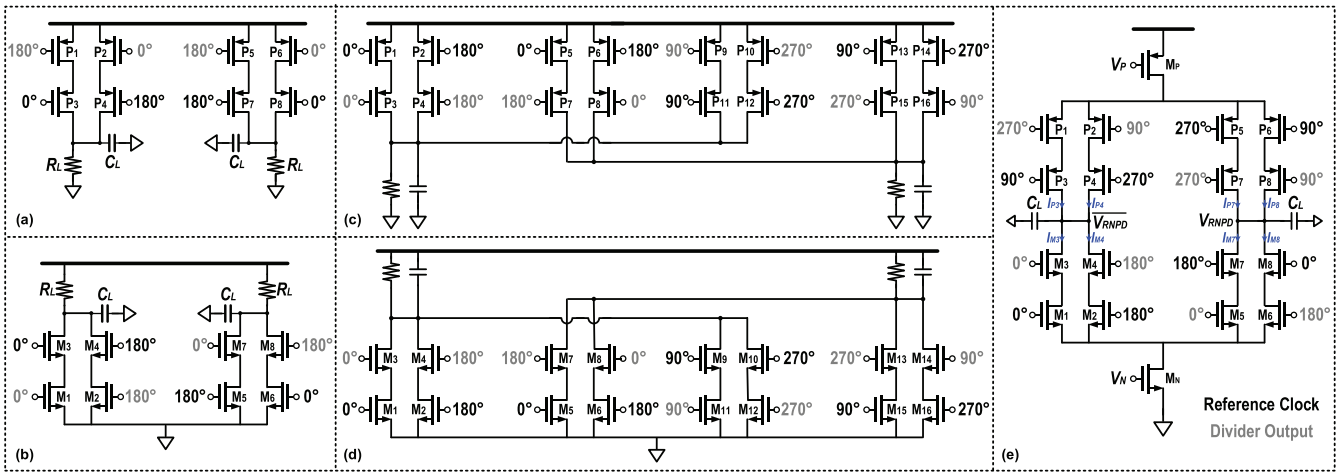

Fig. 3. Single-path PD performing dual-tone mixing for phase detection: (a) all pMOS realization and (b) all nMOS realization. Realization of ripple neutralization technique corresponding to Fig. 2(b): (c) all pMOS realization and (d) all nMOS realization. (e) Complementary implementation of ripple neutralization.

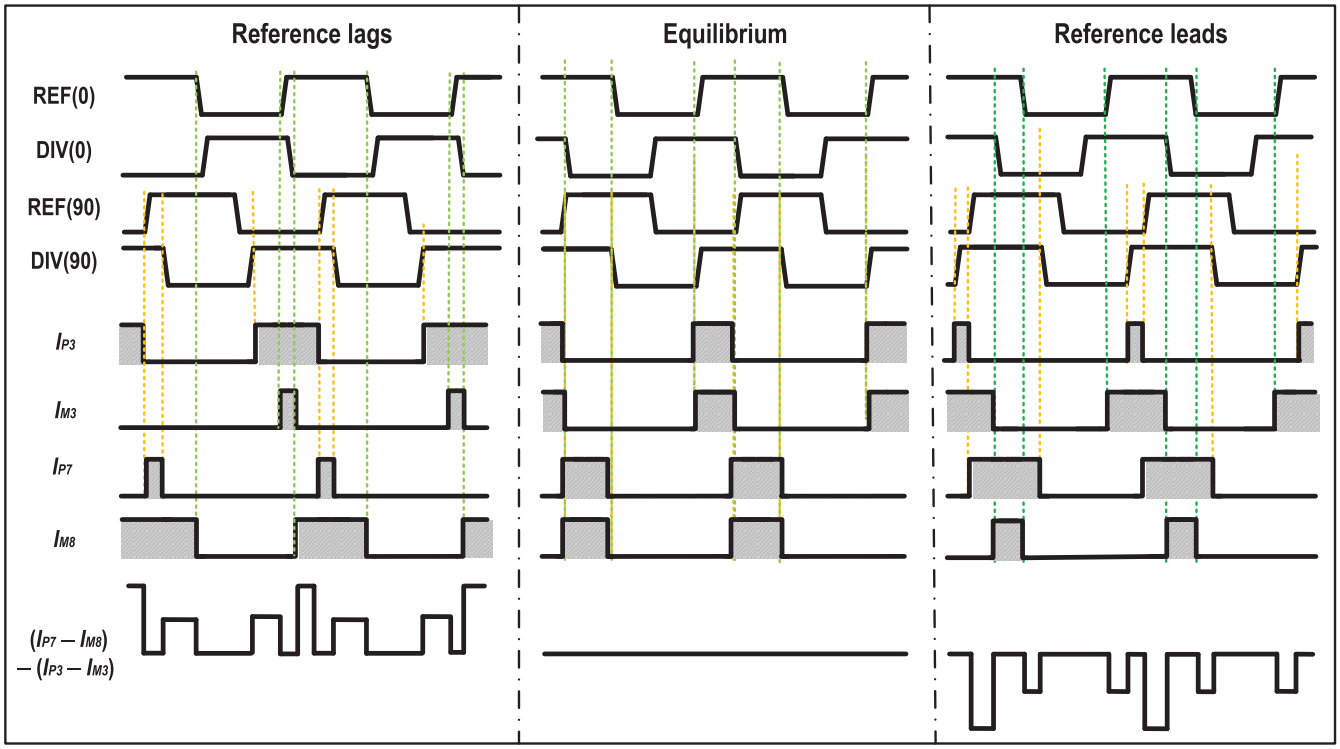

Fig. 4. Timing diagram illustrating ripple neutralization.

mixing, achieved by stacking two identical transistors. The load resistor R_L defines the downconversion gain and also contributes to f_{PD} in (2). These two PDs compare the input phases and generate a near-dc output, driving V_{ctrl} toward phase locking. Unfortunately, the mixing also produces spurious tones dominant at $2f_{\mathrm{ref}}$. In the time domain, the ripple generated in the quarter reference cycle must be neutralized in the next quarter cycle. Although a subsequent LF can attenuate the ripple to some extent, it, however, sacrifices loop stability and acquisition range, both of which could potentially lead to locking failure.

The ripple neutralization, in essence, neutralizes the ripple over a full reference cycle. The aforementioned two PDs are developed into Fig. 3(c) and (d) to perform ripple neutralization. In Fig. 3(c), for example, the ripple currents generated by P_1–P_8 are neutralized by those from P_9 to P_{16}. The same principle applies to Fig. 3(d), although its power consumption must be doubled. Since ripple neutralization operates in the current domain, a complementary version is introduced [Fig. 3(c)] by folding the all-pMOS PD onto the all-nMOS PD, forming the CRN-PD. Such a topology eliminates the need for R_L. Its operating principle is illustrated in Fig. 4. When the reference clock lags, the net current $I_{\mathrm{net}} = (I_{P7} - I_{M8}) - (I_{P3} - I_{M4})$ remains positive, driving V_{ctrl} toward a lower voltage and therefore smaller VCO frequency. A similar process applies when the reference clock is leading. In the equilibrium state, I_{P3} is well neutralized by I_{M4}, and I_{P7} is well neutralized by I_{M8}, nulling I_{net}. From this perspective, the CRN-PD tends

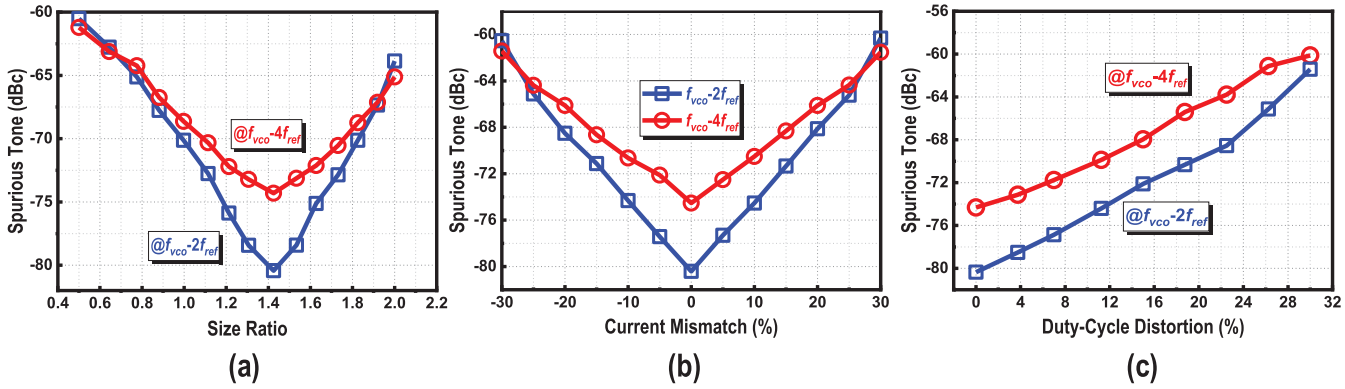

Fig. 5. Simulated spurious tone against (a) size ratio between PDs, (b) current mismatch between PDs, and (c) duty-cycle distortion of the PD input clock.

to guide phase alignment rather than impede it. In Fig. 3(a) and (b), however, if only I_{P3} (I_{M4}) and I_{P7} (I_{M8}) exist, the charge injected into C_L due to I_{P3} (I_{M4}) must be neutralized by I_{P7} (I_{M8}) in the next quarter reference cycle, producing a high level of spurious tone at $2f_{\text{ref}}$.

The effectiveness of ripple neutralization by the CRN-PD heavily relies on device matching between the two PDs. By choosing the minimal gate length for all transistors, the optimal size ratio from the all-pMOS PD to the all-nMOS PD is ~1.42, as observed in Fig. 5(a). Furthermore, the dominating spurious tone is at $2 \times 2f_{\text{ref}}$, where the first factor of 2 is due to differential operation, and the second one stems from ripple compensation. The rise of the $2f_{\text{ref}}$ tone is due to nonzero I_{net}, a result of device mismatch. Spurious tone degradation due to current mismatch is depicted in Fig. 5(b). Current tuning for each PD is achieved by biasing the tail current transistors M_N and M_p in Fig. 3(e). Since ripple neutralization relies on the ripple waveforms being identical, the duty cycle distortion of the input clock raises the spurious tone, as evaluated in Fig. 5(c).

The above simulation results indicate the need for dedicated calibration for practical use. Spurious tones associated with the ripple amplitude at the PD output can be evaluated by the following equation:

$$\text{Spurious Tone}\Big|_{4f_{\text{ref}}} \approx 20\log\left[\frac{\frac{H_{V/I}\times 2\pi f_{\text{BW}}\times N}{\sqrt{1+(2\pi\times 4f_{\text{ref}}\times R_2C_2)^2}}V_{\text{ripple}}}{2K_{\text{PD}}\times 4\times 2\pi f_{\text{ref}}}\right] \quad (3)$$

where $H_{V/I}$ denotes the voltage gain of the V–I converter (VIC), R_2C_2 is the filter preceding V_{ctrl}, and N represents the PLL divide ratio. With f_{ref} = 300 MHz, N = 128, f_{BW} = 10 MHz, K_{PD} = 12 V/rad, $H_{V/I}$ = 30 dB, C_2 = 1 pF, and R_2 = 1 kΩ, V_{ripple} must be smaller than 1 mV to attain < −74-dBc spurious tone at the PLL output. In Fig. 5, the simulated V_{ripple} is ~ 682 μV to realize a spurious tone of −75.1 dBc at $4f_{\text{ref}}$ offset. The spurious tone would rise to −55.3 dBc (simulated) and −57.0 dBc (calculated) if both R_2 and C_2 are missing. These results imply a direct method for CRN-PD calibration by tracing V_{ripple}.

B. Calibration for CRN-PD

Fig. 6(a) depicts the calibration scheme, comprising two paths. Path-I includes a shift register and a thermometer-code converter, while Path-II involves an envelope detector (ED), a 4-bit flash analog-to-digital converter (ADC), and a register array, followed by a finite-state machine (FSM).

The calibration timing diagram is illustrated in Fig. 6(b). Clocked by signal CK_{FC}, Path-I generates a series of time frames from ⟨0000⟩ to ⟨1111⟩, each with a period of ~ 5 μs. Moreover, as shown in Fig. 6(c), Path-I gradually activates the 4-bit current digital-to-analog converter (DAC) feeding the all-pMOS PD, with the current amplitude scaled from the smallest (at ⟨0000⟩) to the largest (at ⟨1111⟩). During each time frame, Path-II first amplifies the weak signal through the ED and then generates a voltage level (V_{ED}) that represents the envelope amplitude level. V_{ED} is sensed by the flash ADC and recoded digitally into the register array. A signal D_{min} remains asserted as long as the existing V_{ED} is smaller than all its previous values. In this manner, V_{ED} undergoes an overall of 16 comparisons. In Fig. 6(a), as an example, the ADC quantizer output decreases as V_{ED} becomes smaller, until the state ⟨1100⟩ at t_1. D_{min} is deasserted at t_2 and remains so until the end since all remaining quantizer outputs are no longer smaller than that at t_1. At the end, the FSM selects the state at ⟨1100⟩, which corresponds to producing the minimal V_{ED} and, therefore, the smallest PLL spurious tone level. The D_{DEC} signal switches the selector output from Path-I to Path-II afterward, maintaining this state for subsequent PLL operation.

C. Design of VIC

Besides device mismatches, the CRN-PD has another drawback: low K_{PD}. By observing the waveform shown in Fig. 4, the CRN-PD output voltage, which is $\Delta V_{\text{PD}} = V_{\text{RNPD}} - V_{\overline{\text{RNPD}}}$, exhibits a linear relationship with the PD input phase error $\Delta\theta$ (i.e., the phase error between the reference clock and the divider output). ΔV_{PD} is maximized when $\Delta\theta = 90°$ and nulled when $\Delta\theta = 0°$. From this perspective, K_{PD} is $2V_{\text{DD}}/\pi$, indicating that K_{PD} is only 0.57 V/rad for a 1-V power supply. This results in a large input-referred noise and therefore a poor PD phase noise. This dilemma can be alleviated by allowing a VIC to follow the PD and significantly sharpen the

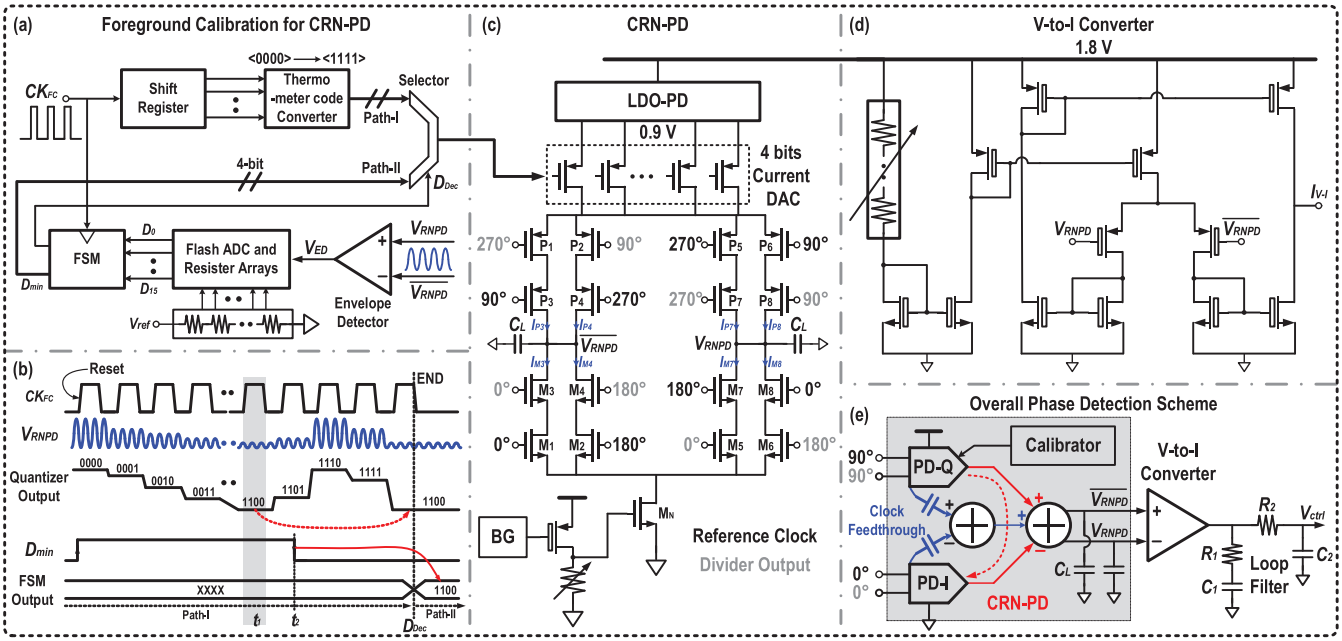

Fig. 6. (a) Calibration scheme for CRN-PD, (b) timing diagram showing the calibration, (c) full version of the CRN-PD, (d) schematic of the VIC, and (e) overall phase detection scheme including LF.

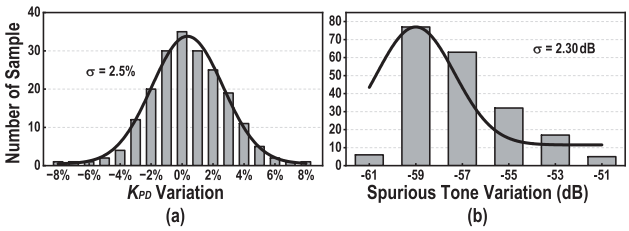

Fig. 7. Monte Carlo statistics of PD + VIC in terms of (a) K_{PD} variation and (b) spurious tone variation (normalized to 320 GHz).

voltage-to-phase transition, as shown in Fig. 6(d), effectively boosting K_{PD}. The VIC is inherently a high-gain transimpedance amplifier. Upon phase locking, ΔV_{PD} would converge to a near-dc voltage. Consequently, the VIC, supplied by 1.8 V, can be constructed using thick-oxide transistors without relying on a level shifter. This approach not only boosts K_{PD} but also increases the effective tuning voltage for V_{ctrl}.

Notably, a voltage level shifter is necessary in CP-PLLs [30], which are power-hungry and noisy for $f_{ref} > 250$ MHz. In that case, since the PFD dead-zone mitigation pulses are difficult to generate, it fails to completely steer the CP current.

The overall phase detection scheme is illustrated in Fig. 6(e). As indicated by (3), R_2C_2 serves to attenuate the spurious tone at $4f_{ref}$, imposing negligible impact on PLL phase margin. The complementary topology of the CRN-PD partially neutralizes clock feedthrough and charge injection, as is the case in the current-steering CP.

Monte Carlo statistics of the CRN-PD + VIC are summarized in Fig. 7(a) and (b), with 200 samples for each. As the VIC amplifies near-dc output voltage of the CRN-PD, its transistors can be sized large enough to reduce process variation, as long as the pole it introduces imposes negligible impact on the PLL loop dynamics. The PD gain variation exhibits a standard variation of 2.5%, which can be compensated by tuning the VIC static current. To evaluate how the spurious tone is degraded, in the simulation, only the CRN-PD and the VIC adopt transistor models, whereas other blocks are Verilog-A models or ideal components. The statistical results indicate a standard variation of 2.3 dB and an extreme case of −50.2 dB (all normalized to 320 GHz). This result indicates the impact of VIC mismatch, demanding another calibration in future implementations.

D. Comparison With Prior Arts

The complementary mixing PD (CMPD), composed of two pairs of harmonic-rejection mixers, was adopted in [31] to perform spurious tone rejection in a push-pull manner. The CMPD also neutralizes clock feedthrough and charge injection directly at its output. However, this PD requires eight phases for harmonic rejection, and the actual reference frequency must be four times the PD input clock frequency. In [31], the PD input frequency is 320 MHz, while the reference frequency is approximately 1.28 GHz. The ripple compensation PD (RCPD) introduced in [32] employs four pairs of sampling switches combined with a differential current summer to achieve ripple compensation through mutual current compensation. Similar to the CMPD, the RCPD enhances spurious tone rejection without introducing extra LF. Although the charge injection and clock feedthrough stemming from the current summer can be effectively compensated by the complementary configuration, the clock feedthrough from all sampling switches cannot be mitigated. Consequently, a smaller f_{BW} (<6 MHz) is allocated to achieve a spurious tone level of −75 dBc, resulting in a higher integrated jitter of 88.5 fs_{rms}.

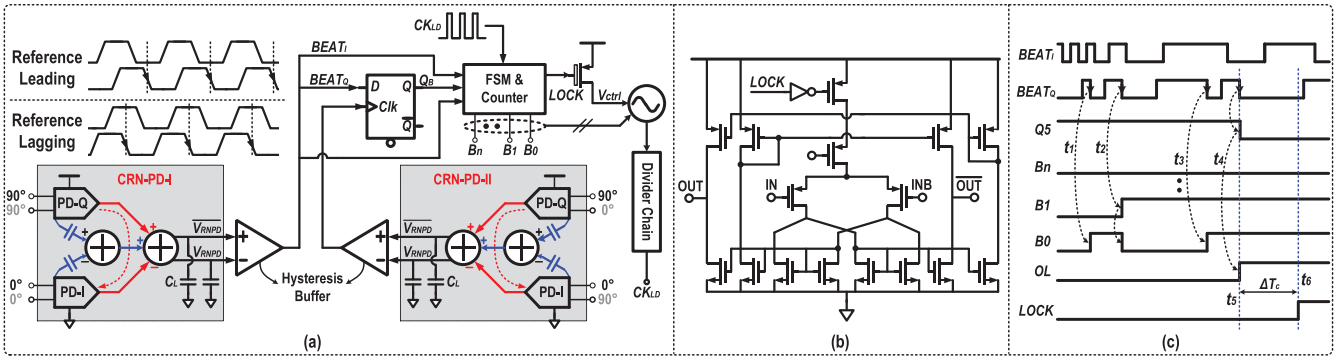

Fig. 8. (a) Block diagram of LD for VCO band searching, (b) hysteresis buffer, and (c) timing diagram of VCO LD.

The CRN-PD combines the advantages of both the CMPD and the RCPD. First, the switches and the current summer have been merged, allowing the ripple current, charge injection, and clock feedthrough, to be mutually neutralized at the PD output. This integration eliminates the need to narrow $f_{\rm BW}$ to suppress spurious tones caused by clock feedthrough. Moreover, since ripple neutralization can be performed with quadrature phase, the reference frequency needs not be multiplied by a factor of 4. Consequently, the CRN-PD achieves mutual ripple compensation without multiplying the reference frequency, enabling an $f_{\rm BW}$ greater than 10 MHz for enhanced attenuation of VCO phase noise (Section IV-E).

IV. PLL Implementation and Frequency Quadrupler

A. LD by CRN-PD

LD is preferred for a wide FTR VCO. In CP-PLLs, LD is performed by tracing $V_{\rm ctrl}$ [33]. This approach, however, couples the required time for LD ($T_{\rm LD}$) with the PLL loop dynamics. In a small $f_{\rm BW}$ PLL, $T_{\rm LD}$ could last for milliseconds.

One way to decouple this relationship relies on determining whether the reference clock leads or lags. According to Fig. 4, the CRN-PD fulfills this need. It produces a beating signal whose frequency $\Delta f_{1,1} = |f_{\rm div} - f_{\rm ref}|$. In this regard, LD can be realized by sampling one CRN-PD output with another CRN-PD, and the sampled results (Q_B) indicate whether $f_{\rm ref}$ is faster or slower. Fig. 8(a) sketches the LD, composed of a pair of CRN-PDs and hysteresis buffers, a D-flip-flop (DFF), and an FSM. One CRN-PD output $\rm BEAT_I$ is sampled by another, namely $\rm BEAT_Q$. As shown in Fig. 8(b), the hysteresis buffer is inherently a narrow band yet a high-gain amplifier. It serves to further attenuate the harmonic terms, leaving only $\Delta f_{1,1}$, and boosts the amplitude of the beating signal to a logic level.

Fig. 8(c) provides the LD timing diagram. A reset pulse initializes the FSM, and the VCO coarse tuning commences from its lowest band. Once $\rm BEAT_Q$ samples a logic zero, implying that $f_{\rm ref}$ is still faster, the band register rises to a higher band. This operation lasts until the sampled result is a logical one. Thereafter, an indicator OL is asserted to initiate a counter and start counting the time period of $\rm BEAT_Q$. If no transition of $\rm BEAT_Q$ is found during the counting, the counter would eventually overflow, asserting the LOCK signal and finalizing the LD. Otherwise, LD would restart since an error occurs during band searching. The required time period for a successful LD operation is estimated as follows:

$$T_{\rm LD} = T_r + \sum_{i=1}^{k\le L} \left(|f_{{\rm div},i} - f_{\rm ref}|^{-1}\right) + \Delta T_{\rm ct}\Big|_{\substack{f_{\rm ref}-f_{{\rm div},k-1}>0\\ f_{\rm ref}-f_{{\rm div},k}<0}} \tag{4}$$

where L is the total number of VCO bands, T_r is the LD initiation time, and $\Delta T_{\rm ct}$ is the time required for the counter to overflow. Clearly, $T_{\rm LD}$ mainly depends on M rather than PLL loop parameters. M is typically limited to 8 for mmW VCOs. The estimated $T_{\rm LD}$ by (4) is tens of microseconds.

B. Risks of CRN-PD and LD

Two risks could cause locking failure. One is the generation of beating signals in the form of $\Delta f_{\alpha,\beta} = |\alpha f_{\rm div} - \beta f_{\rm ref}|$, where α and β are integers greater than unity. $\Delta f_{\alpha,\beta}$ is all much faster than $\Delta f_{1,1}$. They confuse the LD operation, as incorrect falling edges of $\rm BEAT_Q$ misguide the band register. This can be addressed by utilizing long-channel devices for the hysteresis buffer, allowing it to respond only to slow-varying signals, thereby bypassing $\Delta f_{\alpha,\beta}$ terms inherently.

The other risk is the finite acquisition range of the CRN-PD, possibly necessitating a frequency detector (FD). The PD acquisition range is $\propto\ K_{\rm PD} \times K_{\rm vco}/N$. Fortunately, the LD inherently enables FD since only $\Delta f_{1,1}$ is distilled. Similar to SS-PLLs, a CP, although not shown in Fig. 7(a), can be added and driven by the LD. Whether to sink or source current from the LF is determined by the sampled result Q_B. Upon $\Delta f_{1,1} \rightarrow 0$, the CP is disabled. In fact, in transient simulation, the VIC output can sweep all possible values of $V_{\rm ctrl}$, without the need for the FD. From this perspective, the acquisition range is sufficient to cover the overall FTR of the VCO. This can be attributed to the large $K_{\rm PD}$ boosted by the VIC. However, since a smaller RC corner of the LF is required to attenuate the spurious tone in [32], an auxiliary CP is mandatory to assist with phase locking.

C. Calibration for ILFD

The prescaler is one of the most critical components in mmW PLLs, as it is prone to failure. In [31], a static divider serves as the prescaler but consumes significant power at ~40 GHz. A Miller divider is used in [32], occupying a large

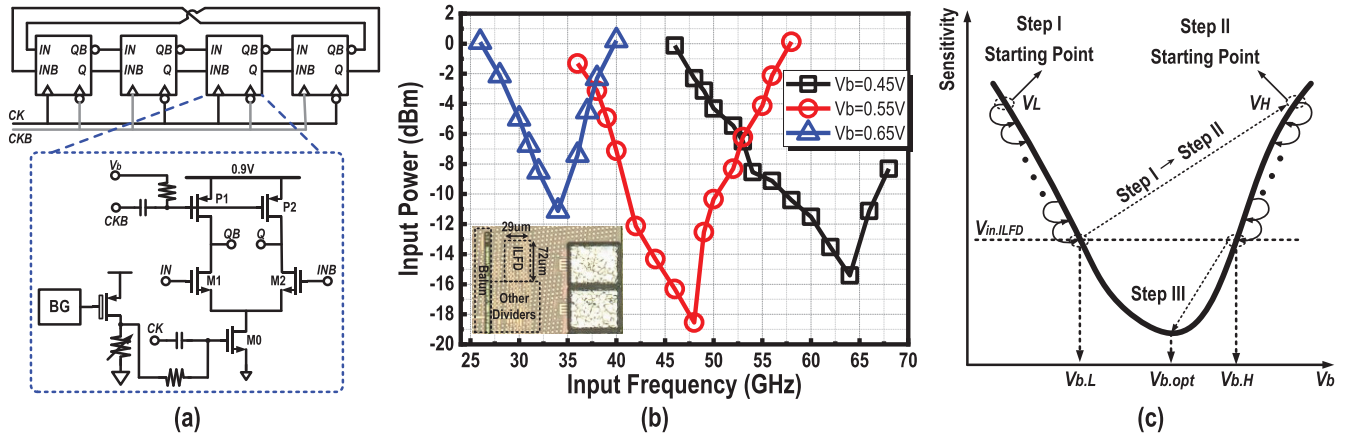

Fig. 9. (a) ILFD based on dynamic latches [34], [35], (b) measured ILFD sensitivity and locking range against the pMOS bias V_b, and its die photograph, and (c) conceptualized calibration scheme for ILFD based on dynamic latches.

area due to the use of an inductor. In contrast, inductorless mmW ILFDs, which involve four-stage cascaded dynamic latches, feature low power consumption, small area, and a wide locking range [34], [35]. Fig. 9(a) illustrates its schematic. Given an external clock injection, the ILFD may lock to the subharmonic of the injected clock. By tuning the gate bias V_b of P_1 and P_2, the overall loop delay would be four times the injected clock period. When the injected clock frequency changes from 4× of the ILFD's natural oscillation frequency (f_{ILFD}), strong injection is required. An ILFD based on dynamic latches has been verified in the same technology, and its measured sensitivity curves against V_b are provided in Fig. 9(b). When not driven by the external clock, the ILFD exhibits a free-running frequency from 8.2 to 21.5 GHz, which can be tuned externally by adjusting V_b.

Such an ILFD raises several concerns in a wide FTR mmW PLL. First, the loading capacitance, layout symmetry, and PVT variations all affect f_{ILFD}, necessitating careful tuning of V_b. Second, although not observed in our measurements, the ILFD may lock to other subharmonics like 5 and 6, as reported in [35]. The tuning window of V_b for divide-by-4 was only ~20 mV. Third, the amplitude of the ILFD input voltage $V_{\text{in.ILFD}}$, which is the VCO output, is unknown. As the VCO tank voltage amplitude is $\propto Q^2$, the degradation of Q, caused by capacitor bank switches, attenuates $V_{\text{in.ILFD}}$. A remedy for this is either inserting a buffer between the VCO and ILFD to compensate for the attenuation or tuning V_b further.

The above discussion suggests that V_b must be well defined for a certain injection frequency f_{osc} and $V_{\text{in.ILFD}}$. A calibration scheme is therefore introduced, as conceptualized in Fig. 9(c). The operation, comprising three steps, is to search for the bias points where the ILFD starts to lock to the input clock. In the first step, V_b is biased to V_L, where V_L is the minimum bias voltage that potentially allows the ILFD to oscillate. Since f_{ILFD} is expected to be far from $f_{\text{osc}}/4$, the ILFD fails to lock. Then, a state machine digitally increases V_b gradually until the ILFD can lock. At this point, V_b is assigned to $V_{b,L}$, which is the minimum bias point allowing the ILFD to lock. In the next step, a higher voltage V_H is assigned to V_b, which corresponds to the maximum possible bias voltage allowing the ILFD to oscillate. The state machine then gradually decreases V_b gradually until $V_{b,H}$ is found. It is the maximum bias voltage allowing the ILFD to lock. As $V_{b,L}$ and $V_{b,H}$ are a pair of extreme bias point, in the final step, V_b is assigned to $V_{b,\text{opt}} = (V_{b,L} + V_{b,H})/k_{\text{ILFD}}$, where where k_{ILFD} is typically 2 or 3. In this manner, the ILFD gains a dynamic range of $V_{b,H} - V_{b,L}$ for a certain $V_{\text{in.ILFD}}$, within which the ILFD can always lock to the input clock. As $V_{b,\text{opt}}$ is close to the bias point where f_{ILFD} aligns with $f_{\text{osc}}/4$, the ILFD achieves nearly the highest sensitivity, making it more robust against PVT and input amplitude variations.

Circuit realization of the above concept is sketched in Fig. 10, composed of multiple frequency dividers, a power detector, an FD discussed in Section III-A, an FSM, and a pair of bias DACs. Three paths jointly involve in the calibration. Upon initiating the FSM, the control logic selects $V_{b.t} = V_L$ to begin with. As V_L is small, the ILFD may fail to oscillate, and its output power is weak. The power detector senses this voltage level and allows MUX S1 and S2 to select Path-II. Then, Path-I and Path-II start frequency comparison. As the division ratio differs for these two paths, the FSM gradually increases $V_{b.t}$ through S3. Once the ILFD starts oscillating, its output power becomes large enough, and the power detector selects Path-III to compare the frequency with Path-I. If the ILFD fails to lock at this state, its output frequency would toggle between two distinct frequencies and would never reach a steady output frequency. In this case, frequency error persists between the two paths. The FSM then continues to increase $V_{b.t}$ until the ILFD can lock. Upon frequency locking, Path-I and Path-III produce the same frequency to the FD, overflowing the counter in the FSM. The control logic assigns the current $V_{b.t}$ to $V_{b,L}$, refreshing the FSM and initiating the next flow, which starts with $V_{b.t} = V_H$. The same process applies to this case through another bias DAC until $V_{b.t} = V_{b.H}$ is found. Finally, the control logic assigns $V_{b.t} = V_{b.\text{opt}}$ through S3 and fixes this value until the FSM receives a new reset signal.

The reference divider is critical, as it serves as the prescaler for Path-I and Path-II. Since it must be able to lock to the

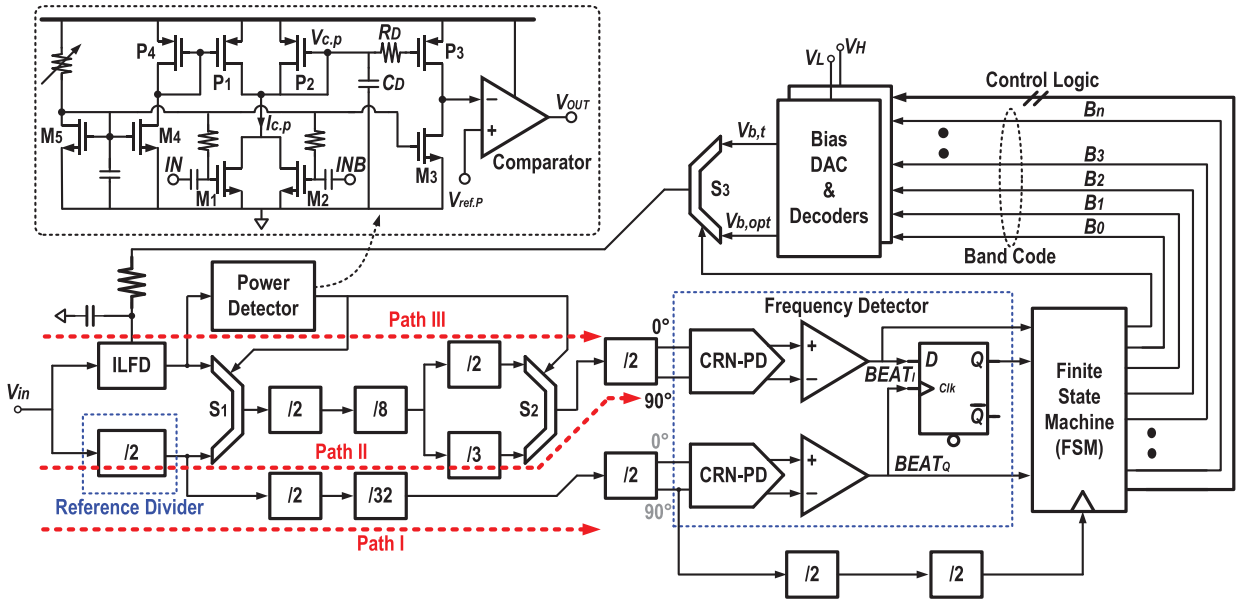

Fig. 10. Circuit realization of calibration for the ILFD based on dynamic latches and the power detector.

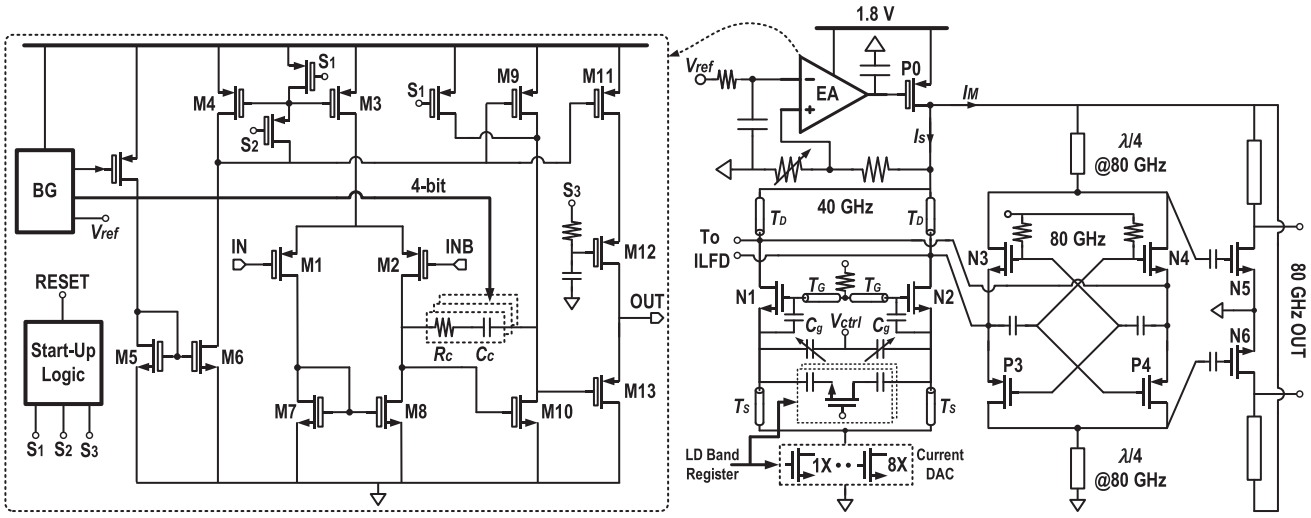

Fig. 11. mmW VCO, the first frequency doubler, and their voltage regulation. BG and bias circuitries are not shown.

input clock throughout all phases of the calibration, a wide locking range, high sensitivity, and small area are preferred design choices. More importantly, the design should avoid dedicated tuning voltage like the ILFD. Miller dividers are feasible for mmW operation, with small power consumption (6.6 mW in simulation), but their locking range is ~5 GHz, and they occupy a large area. Instead, the static divider composed of a pair of DFFs achieves a wide locking range over 20 GHz without using inductors. In this regard, it fulfills the above requirements. CML topology has been applied to maximize the operating frequency. Its power consumption is 45.8 mW, including buffers. However, power consumption is not a concern here since the reference divider will hand over the loop to the ILFD and shut down automatically upon completion of the calibration.

The power detector senses the ILFD output signal using a differential pair $M_{1,2}$, and their combined current $I_{c.p}$ contains a near-dc term and a second harmonic. $I_{c.p}$ is converted to voltage $V_{c.p}$ by a diode-connected pMOS P_2. $V_{c.p}$ then undergoes filtering, and only the near-dc term, which represents the input power level, is distilled and amplified by P_3 and M_3. The subsequent comparator compares this voltage with $V_{\text{ref}.P}$, and the comparison result indicates whether the ILFD is oscillating. The power detector consumes 8.6 mW of power. Likewise, it will be shut down immediately after the calibration is finished.

D. MmW Vco and Frequency Doubler

A Colpitts oscillator is preferred for achieving a wide FTR at mmW frequencies [14]. As shown in Fig. 11, it is mainly composed of nMOS $N_{1,2}$ and coils T_G, T_S, and T_D. T_G must be carefully tuned for the desired oscillating frequency and high Q-factor. The tank involves 3-bit coarse tuning, assigned by the LD band register, which also manipulates the tail current DAC to compensate for Q-factor degradation when more switches

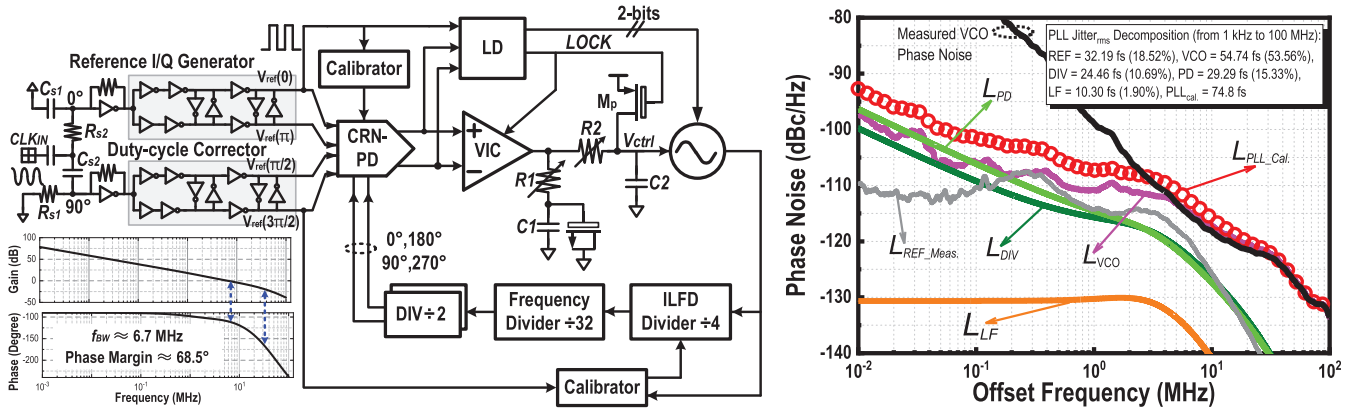

Fig. 12. (Left) mmW PLL architecture and analytical PLL open-loop gain/phase. (Right) Analytical noise decomposition (fit to Fig. 21) including the measured VCO phase noise.

are on. In our simulation, 4-bit coarse tuning imposes a risk of oscillation failure for temperatures over 65 °C in the slow corner.

The VCO supply voltage must be well regulated to: 1) define its value; 2) isolate the supply noise from other blocks [36]; and 3) minimize ground-loop effects circulating between the power and the ground, thereby preventing spurious tones coupled from the external environment. The voltage regulator is shown in Fig. 11 as well, where M_1–M_{13} constitute the error amplifier (EA). Start-up logic ensures its correct operating point. Each transistor is sized large enough to enable the overall VCO phase noise not to be dominated by the EA noise, but instead by the VCO tank Q-factor. However, large transistors render the EA deviated from the one-pole system model, degrading its phase margin. This would result in transient peaking during start-up, stressing the VCO and potentially causing breakdown damage to $N_{1,2}$. A programmable compensator realized by R_c and C_c cancels out the second dominant pole, allowing the EA to become nearly a one-pole system. The bandgap (BG) reference assigns a 4-bit control to ensure that the VCO does not experience over 15% transient peaking from −45 °C to 110 °C for all available current flowing through it. The regulator provides more than 20-dB PSRR.

The frequency doubler, involving $N_{3,4}$ and $P_{3,4}$, is arranged complementarily. The second harmonic is extracted from their respective common node. Simulation reveals that the output amplitude is ~ 1.6× larger than that of the traditional design by $N_{3,4}$ only for the same current. $N_{5,6}$ serves to filter out unwanted harmonics and further amplifies the second harmonic.

E. Pll Implementation and Loop Dynamics

The mmW PLL incorporating the above techniques is shown in Fig. 12. The quadrature reference clock is generated through a polyphase *RC* filter, followed by a duty-cycle corrector (DCC). The DCC not only sharpens the transition of the reference clocks but also suppresses duty-cycle distortion to <0.15%. Monte Carlo statistics indicate a maximum quadrature error of ±2.2°, raising the spurious tone by 2.8 dB. To further attenuate mutual coupling among blocks, the VCO, dividers, and other in-band components adopt respective voltage regulators, and their ground planes are separated.

PLL division ratio is determined by the available reference clock and (1). The goal here is to ensure that the reference phase noise is dominating, which also guides the transistor sizing of the PD and the VIC. Fig. 12 illustrates the noise decomposition of the mmW PLL. The PLL noise profile has been fit to the measured result in Section V. The reference phase noise and the PD + VIC phase noise contribute 18.5% and 15.3%, respectively, to the PLL phase noise, fulfilling the above requirement. The divider chain phase noise, which contributes additional 10.7% noise, may be reduced by utilizing an mmW clock to sample the divider output and reset its accumulated jitter. The VCO measured a phase noise of −99.6 dBc/Hz at a 1-MHz offset, and its overall phase noise contribution is 53.6%, which is hard to reduce for a certain FTR. This can be addressed by allowing a wide f_{BW} to the PLL. The CRN-PD enables this design choice since the spurious tone level now relies on ripple neutralization instead of a narrow f_{BW}.

The PLL exhibits seven poles, located at 1.92×10^9, 1.74×10^9, 3.92×10^8, 2.28×10^8, 5.47×10^7, 1.14×10^7 rad/s, and at the origin, where the two poles 1.92×10^9 and 5.47×10^7 rad/s are neutralized by respective zeros. The remaining zero, located at 1.44×10^7 rad/s, lies between the two dominant poles. Such a zero/pole allocation leads to an f_{BW} of ~6.7 MHz and a phase margin of 68.5°. PLL loop dynamics can be controlled by digitally tuning the loop resistor R_1 and the VIC output current.

F. THz Frequency Quadrupler

With an 80-GHz input, the frequency quadrupler begins with a quadrature generator, followed by I and Q amplification paths; each ends with a frequency doubler, generating the ultimate output frequency at 320 GHz by the third doubler. Fig. 13 illustrates each building block. An mmW quadrature generator can be realized by a hybrid coupler, but it incurs a large area cost for producing differential outputs for I/Q signals with a complex layout. Instead, although it introduces a higher insertion loss, the *RC* polyphase shifter is highly

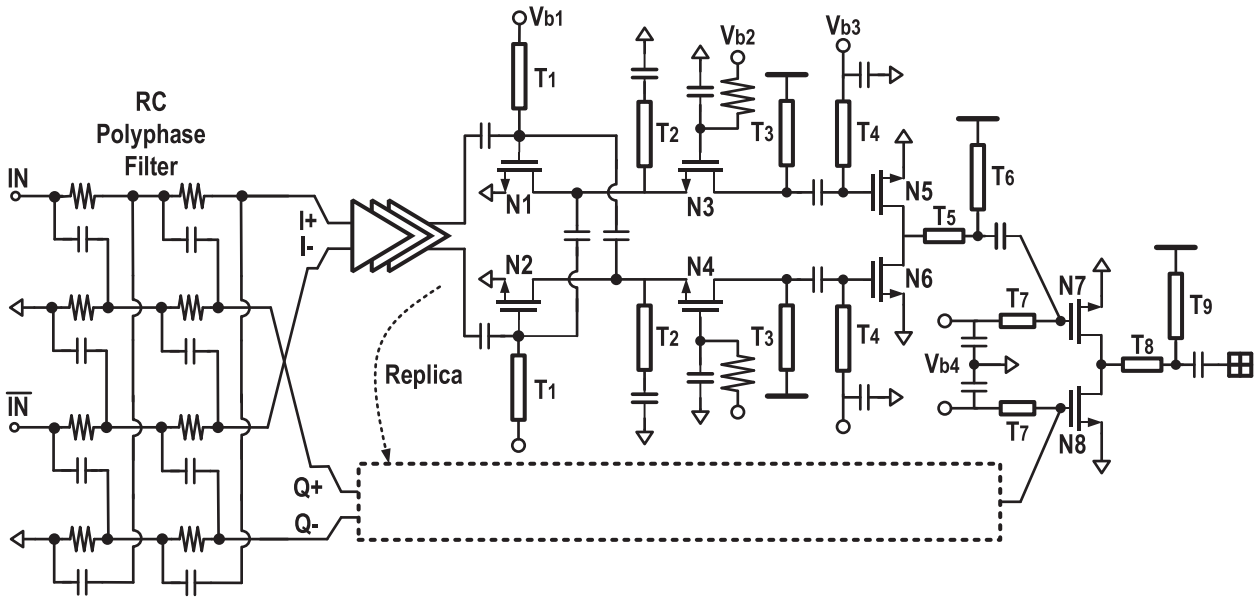

Fig. 13. Frequency quadrupler realized by quadrature-phase combining.

compact and geometrically feasible for short and symmetrical routing. Simulation reveals a ±2.7° I/Q phase error from 72 to 98 GHz, with <0.62-dB amplitude mismatch.

The I and Q paths involve multiple stages of amplifiers for gain boosting, with the final stage adopting cascode topology. Cross-coupled capacitors neutralize the gate-drain capacitance of $N_{1,2}$, while coils T_2 and T_3 resonate with the parasitic capacitance of $N_{3,4}$. Compared with a common-source topology, the cascode amplifier enhances the output power by 2.2 dB. $N_{5,6}$ serves as the first stage of the doubler, and the second harmonic is extracted at their drain terminal. As the two paths have a phase offset of 90°, it becomes 180° at the doubler output, driving the final doubler $N_{7,8}$. The above quadrature phase offset degrades the output power by about 4.7 dB, as it propagates along the amplification path and is likewise boosted by a factor of 4. Such degradation can be partially compensated by tuning the gate voltages V_{b3} and V_{b4} [37], which are typically biased close to the transistor threshold voltage for maximizing harmonic generation.

The 80-GHz preamplifier is constructed by a three-stage common-source amplifier with capacitive neutralization, as illustrated in Fig. 14. As the maximum available gain (MAG) and the stability factor (i.e., K_f) of the differential pair $M_{1,2}$ are rather sensitive to the value of neutralized capacitance, nMOS varactors $C_{n1,2}$ ($Q \approx 7$) exhibit better matching than metal-oxide–metal (MOM) capacitors ($Q \approx 16$), especially for small size of differential pair. With a small gate-drain capacitance of transistor to be neutralized, exploiting MOM capacitor demands accurate electromagnetic modeling. The nMOS varactor, although exhibiting lower Q-factor, leaves sufficient margin to ensure stability over a wide frequency range and bias condition. Postlayout simulated MAG and K_f against various sizing of $M_{1,2}$ and $C_{n1,2}$ are provided in Fig. 14 as well, indicating absolute stability maintained by the differential pair with $C_{n1,2}$. Coil $T_{1,2}$ resonates out the remaining capacitance

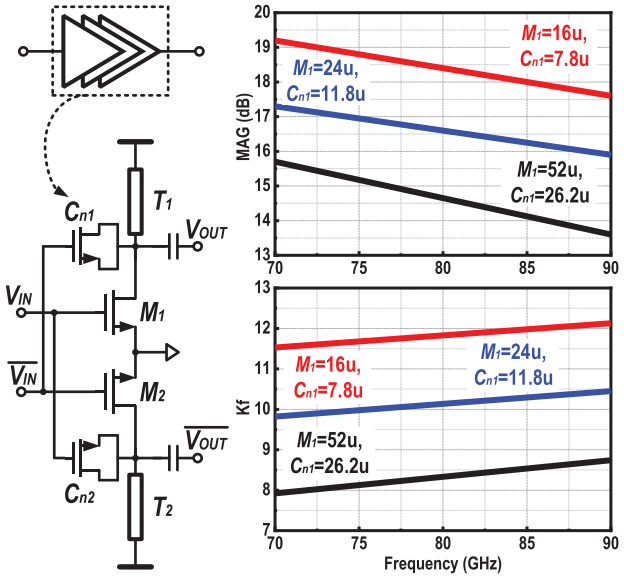

Fig. 14. Preamplifier and its simulated MAG and K_f.

at the differential pair output, creating gain peaking within the operating range and boosting the overall gain inside a small area. To improve the power efficiency, a low-loss directional coupler can be considered to construct the 90° hybrid coupler [37], trading off the chip area. Moreover, wideband techniques for mmW frequency multiplying have been introduced in [38] and [39].

V. Measurement Results

The synchronized THz source generator was implemented using a 22-nm CMOS technology, occupying an active chip area of 0.5 mm^2 (Fig. 15). The chip has been mounted to a board to improve decoupling and power supply. The

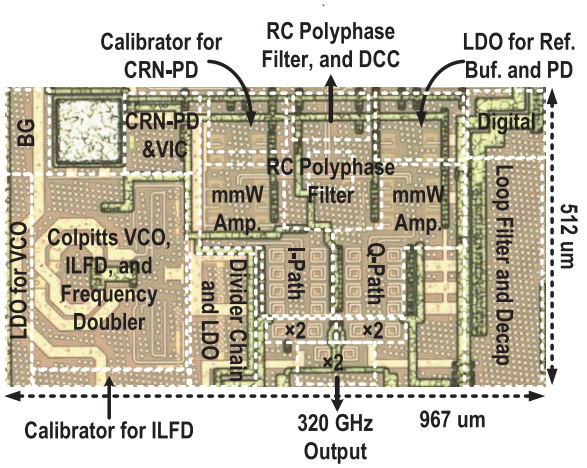

Fig. 15. Die micrograph of the synchronized source generator.

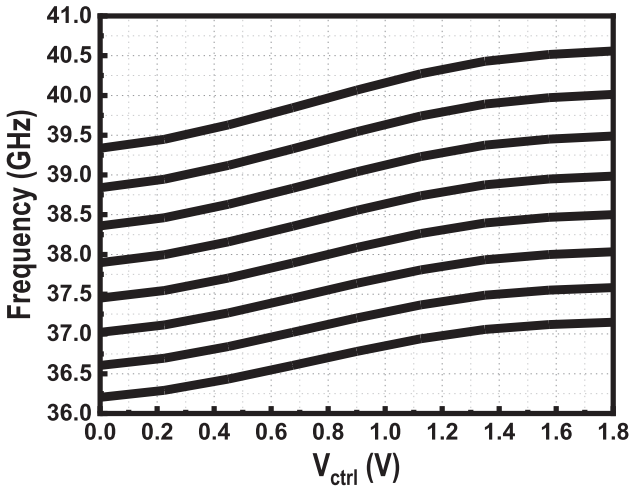

Fig. 16. Measured VCO FTR.

PLL reference was provided by an R&S SMA 100, and the spectrum was measured using a Keysight MXA signal analyzer N9020B. The reference source frequency was tuned in the vicinity of 300 MHz to fully evaluate the signal source performance within the entire operating range. The mmW and THz phase noise was assessed using an R&S FSW-67, which is equipped with a frequency extender up to 0.325 THz. By tuning V_{ctrl} in an open-loop test, the VCO exhibited an FTR from 36.2 to 40.7 GHz, as shown in Fig. 16.

Fig. 17 visualizes the time-domain measurement of the calibration for CRN-PD. The quantizer in the calibrator configured a DAC realized by resistor ladders, and its output is buffered by a unity-gain amplifier, driving the Tektronix mixed-domain oscilloscope for measurement. The calibration took an overall of 16 cycles (i.e., ~ 85 μs) to capture the optimal operating condition, which has been found at the state of ⟨1000⟩. This condition corresponds to the minimal PLL spurious tone that can be achieved for this tested sample.

Due to the weak output power at mmW and THz frequencies, spurious tones cannot be clearly observed from the spectrum analyzer. Consequently, they were measured at the

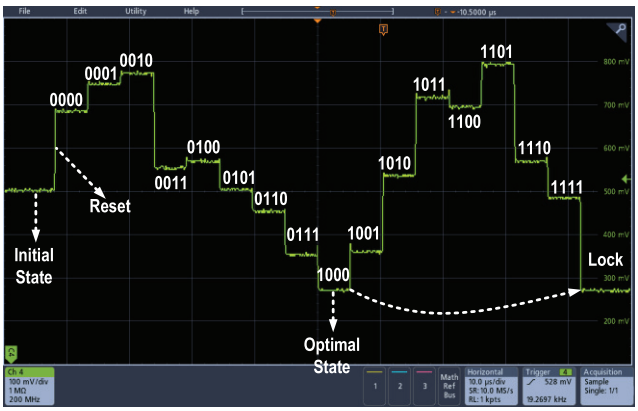

Fig. 17. Time-domain verification of the CRN-PD calibration.

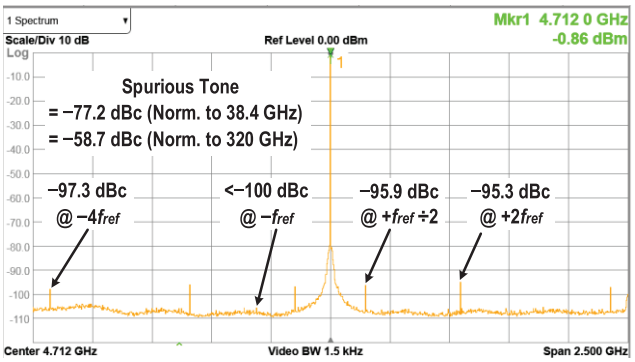

Fig. 18. Measured spurious tone at the divider output.

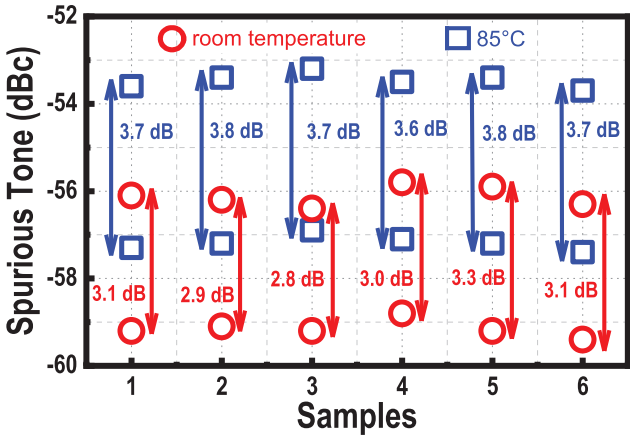

Fig. 19. Summary of measured spurious tone (all normalized to 320 GHz) across the entire PLL locking range for six samples.

5-GHz divider output, as shown in Fig. 18. Measurements were conducted after completing the CRN-PD calibration. The dominant tone was identified at $f_{\text{vco}} \pm 2f_{\text{ref}}$, measured at −95.3 dBc. When normalized to the VCO output frequency of 37.696 GHz and the THz output frequency of 320 GHz, it corresponded to −77.2 and −58.7 dBc, respectively.

An unexpected spurious tone at $f_{\text{vco}} \pm f_{\text{ref}}/2$ revealed a close amplitude level of −95.9 dBc, potentially due to substrate coupling or crosstalk from the calibrators. The spurious tone at $f_{\text{vco}} \pm 4f_{\text{ref}}$ measured −97.3 dBc, due to much stronger

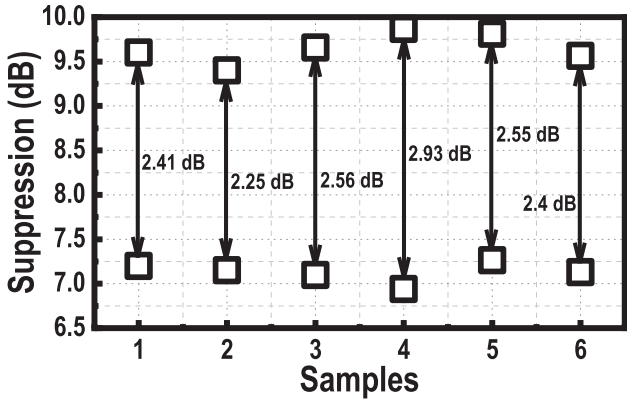

Fig. 20. Measured improvement of spurious tone suppression (all normalized to 320 GHz) by the calibrator compared with the case where the current DAC was fixed to ⟨0000⟩.

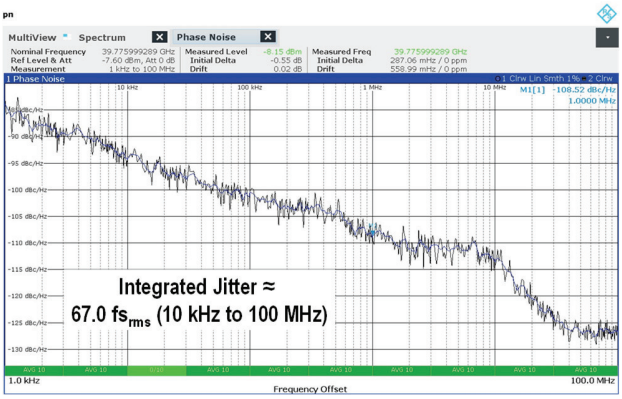

Fig. 21. Measured PLL phase noise at 39.78 GHz.

attenuation by the LF. Levels were below −100 dBc at $f_{vco} \pm f_{ref}$. These results verify the frequency-boosting effect of the CRN-PD. Measurements collected from six samples summarizing the spurious tone across the entire VCO FTR are presented in Fig. 19, all normalized to 320 GHz. At room temperature, spurious tones below −55.8 dBc were achieved, while at 85 °C, they remained below −53.1 dBc. The higher spurious tone levels at higher temperatures may be attributed to increased leakage current through the VCO varactor or LF or worsened device mismatch in the CRN-PD. As indicated in Fig. 20, compared with the case where the calibrator was off and the current DAC was fixed to ⟨0000⟩, the calibrator helped suppress the spurious tone by additional 6.9–9.7 dB across the entire operating range, collected for six samples. The suppression was from 0 to 3.7 dB when compared with the case where the current DAC was fixed to ⟨1000⟩ (not shown in Fig. 20).

The PLL phase noise measured at the VCO output (frequency multiplier was off) is provided in Fig. 21, demonstrating −108.5 dBc/Hz at the 1-MHz offset evaluated at 39.78 GHz. f_{BW} was approximately 6.5 MHz. Extracting the profile from the figure, the corresponding integrated jitter (σ_{rms}) was about 67.0 fs$_{rms}$, with an integration range spanning from 0.01 to 100 MHz. When the frequency multiplier was on, the measured phase noise was shown in Fig. 22, indicating an

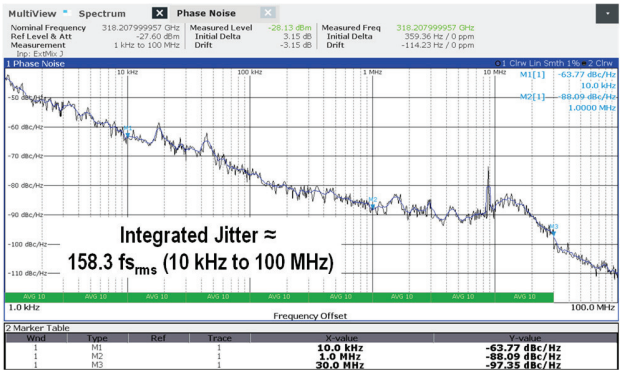

Fig. 22. Measured THz source phase noise at 318.21 GHz.

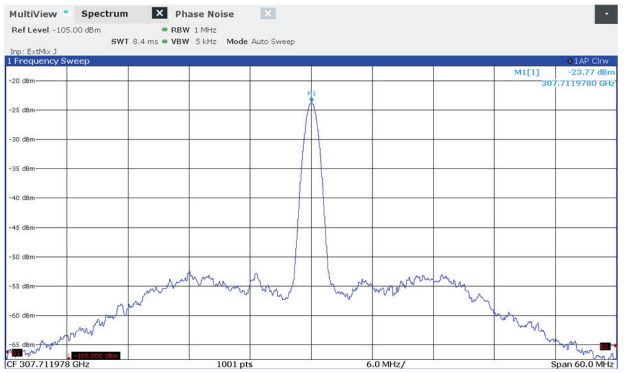

Fig. 23. Measured signal source output spectrum.

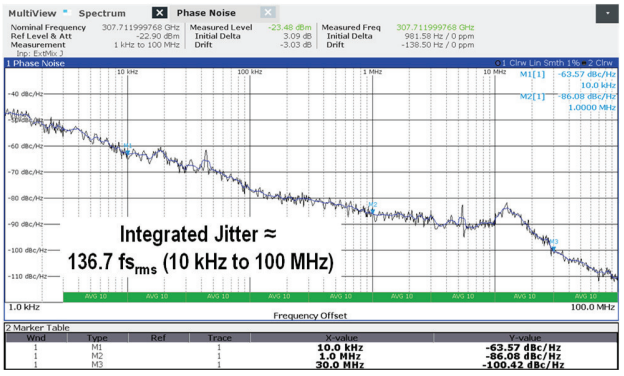

Fig. 24. Measured THz source output phase noise at 307.72 GHz.

integrated jitter of 158.3 fs$_{rms}$ evaluated at 318.21 GHz. The peaking appeared at ∼15 MHz may possibly come from the degradation of VCO tank Q-factor by the frequency multiplier, either through its direct coupling or from noise injection from the regulator, which needs further investigation.

Fig. 23 provides the measured spectrum at which the signal source attained the lowest FoM at THz frequencies, and Fig. 24 displays the corresponding measured phase noise. Found at 307.72 GHz, the phase noise measured −63.6, −86.1, and −100.4 dBc/Hz at offset frequencies of 10 kHz, 1 MHz, and 30 MHz, respectively. σ_{rms} was ∼136.7 fs$_{rms}$ over the same integration range. It corresponds to an FoM of −234.0 dB. The measured σ_{rms} at THz output frequencies is summarized in Fig. 25, remaining below 163.4 fs$_{rms}$ across the entire PLL

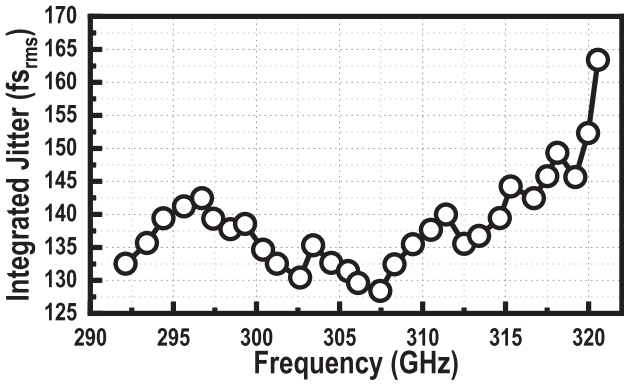

Fig. 25. Summary of THz source generator integrated jitter.

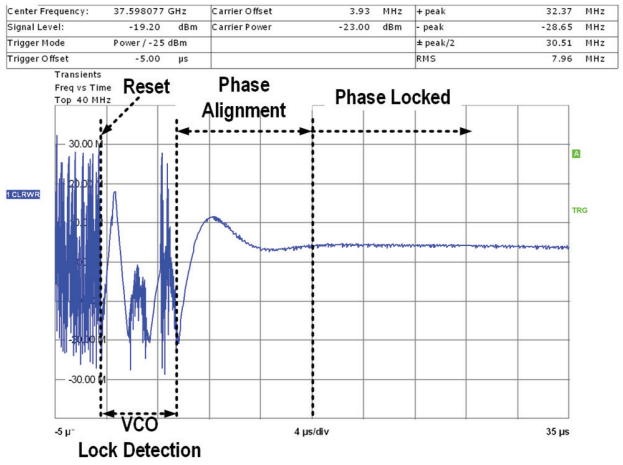

Fig. 26. Transient measurement of VCO LD.

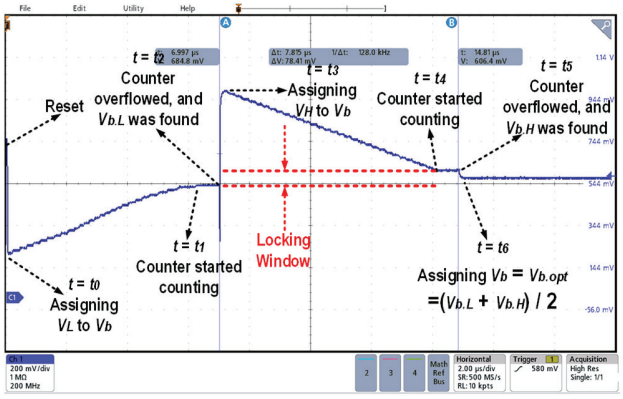

Fig. 27. Time-domain verification of ILFD calibration.

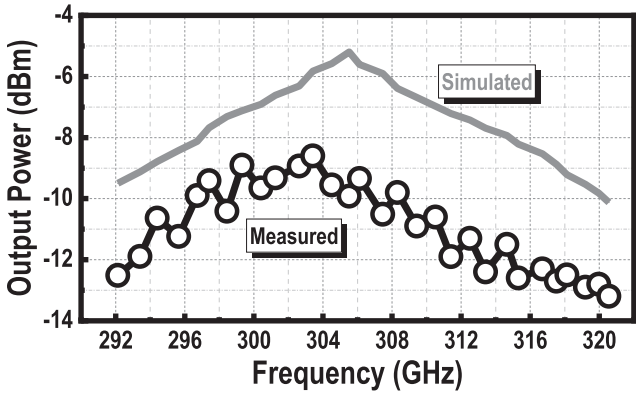

Fig. 28. Simulated/measured THz source generator output power.

TABLE I
THz Source Generator Power Breakdown

Building Block	Power Consumption (mW)
Reference buffer	3.8
VCOs + LDOs + BG	16.2~21.6
VCO buffer + Divider Chain	16.2
CRN-PD	1.8
V/I Converter	3.4~5.2
Frequency Quadrupler	174.8~200.9
Lock detector (off upon lock)	2.7
CRN-PD calibrator (off upon lock)	4.72
ILFD calibrator (off upon lock)	78.5
Drivers for testing	15.8
Total	41.4~48.6 (mmW PLL)
	216.2~249.5 (THz source)

locking range. f_{BW} was well-tuned during testing to achieve the best σ_{rms} at each measured frequency.

VCO LD is verified in Fig. 26. The overall PLL settling time was ~ 16 μs. The time-domain measurement of the ILFD is illustrated in Fig. 27. The tuning voltage V_b is buffered by a unity-gain amplifier, whose output drives the oscilloscope for verification. Calibration for the ILFD was performed after the PLL was well settled. The calibrator was reset at t_0, and V_L was assigned to V_b to initiate calibration. V_b gradually increased until t_1, during which the ILFD failed to lock due to one of the following reasons: 1) the ILFD was not oscillating; 2) its input voltage swing was insufficient to achieve locking; and 3) the ILFD locked to other subharmonic frequencies. At t_1, the ILFD may have begun to lock to $f_{vco}/4$. The counter in the FSM then started counting until it overflowed at t_2, confirming that the ILFD had locked, and this bias voltage $V_{b.L}$. The next step commenced with $V_b = V_H$ at t_3. Similarly, V_b gradually decreased until the ILFD could lock. In the end, the optimal bias voltage was set as $V_{b.opt} = (V_{b.L} + V_{b.H})/2$, finalizing the calibration at t_6. Observed from the same figure, the slot for the ILFD able to lock to $f_{vco}/4$ was approximately 78.4 mV for this tested sample.

A VDI Erickson PM5 power meter was utilized for power measurement. After calibration, the measured output power at THz frequencies is summarized in Fig. 28. The source generator delivered output power ranging from −13.2 to −8.6 dBm from 292.2 to 321.4 GHz, with a peak dc-to-RF efficiency of 0.06%.

The signal source consumed between 216.2 and 249.5 mW from 0.9-/1.8-V power supplies. A power breakdown is listed in Table I. As the two calibrators can be shut down after completing their respective calibrations, their power consumption is not included. Additionally, the output drivers for the divider

TABLE II
SILICON-BASED THz STABILIZED SOURCE GENERATOR PERFORMANCE SUMMARY

	ISSCC'14 [16]	*VLSIC*'16 [18]	*ISSCC*'16 [17]	*ISSCC*'18 [5]	*TMTT*'22 [13]	*JSSC*'22 [21]	*ISSCC*'23 [19]	**This work**
f_{ref} (MHz)	273~296	125	100~110	N/A	600	100	940	**~300**
f_{out} (GHz) FTR	280~303 (7.9%)	208~255 (20.3%)	539~560 (3.8%)	302~332 (9.5%)	306.9~321.3 (4.44%)	198~274 (32.2%)	264~287 (8.3%)	**292.2~321.4 (9.52%)**
Overall division ratio *N*	1024	1664~2040	5390	N/A	512	3020~3320	280~306	**1024**
PN@1 MHz	−82.5	−80	−74	−78.5	−90.3	−85.73	–92	**−86.1**
Normalized PN @1 MHz $\mathcal{L}_{norm}$ (dBc/Hz^2)	–227	–227	–229	N/A	–232	–235	–231	**–231**
Integrated jitter (fs$_{rms}$)	737$^{\Delta}$	N/A	286$^{\Delta}$	192$^{\Delta}$	122$^{\Delta}$	355$^{\Delta}$	87*	**136.7$^{\Delta}$**
Integration Range (MHz)	0.01–100	N/A	0.03–30	0.01–100	0.01–100	0.01–100	0.001–100	**0.01–100**
Spurious Tone (Norm. to 320 GHz, dBc)	N/A	N/A	N/A	N/A	–61.1	–30.2	–46.3	**–58.7**
DC Power (mW)	376	1400	172	51.7	372	49.5	262	**216.2~249.5**
Output Power (dBm)	−14	−11	−27$^{\#}$	−13.9	−3.3	−11	−2.5	**−13.2 to −8.6**
Area (mm^2)	2.56	5.6	2.79	0.85	1.4	0.58	0.99	**0.5**
FoM (dB)	−216.9	N/A	−228.5	−237.2	−232.6	−232.0	−237.0	**−234.0**
FoM$_T$ (dB)	−205.9	N/A	−214.3	N/A	−219.0	−227.1	−226.2	**−223.0**
FoM$_{JRP}$ (dB)	−212.4	N/A	−228.3	N/A	−224.8	−232.0	−227.3	**−229.5**
FoM$_{JIT,N}$ (dB)	−247.0	N/A	−265.8	N/A	−259.7	−267.0	−261.6	**−264.4**
FoM$_p$ (dB)	−202.9	N/A	−201.5	−223.3	−229.3	−229.3	−235.8	**−225.6**
Silicon Technology	90 nm SiGe	65 nm CMOS	65 nm CMOS	130 nm SiGe	130 nm SiGe	65 nm CMOS	65 nm CMOS	**22 nm CMOS**

$\mathcal{L}_{norm} = \mathcal{L}_{in\text{-}band} - 10\log(f_{ref}) - 20\log(N)$ [22] | FoM = $10\log[(\text{DC Power}/1\text{ mW}) \times (\sigma_{rms}/1\text{s})^2]$ [26]

$\text{FoM}_T = 10\log[(\text{DC Power}/1\text{ mW}) \times (\sigma_{rms}/1\text{s})^2 / \text{FTR}]$ [33] | $\text{FoM}_{JIT,N} = 10\log[(\text{DC Power}/1\text{ mW}) \times (\sigma_{rms}/1\text{s})^2] + 10\log(f_{ref}/f_{out})$ [40]

$\text{FoM}_{JRP} = 10\log[(\text{DC Power}/1\text{ mW}) \times (\sigma_{rms}/1\text{s})^2 \times (f_{ref}/100\text{ MHz})]$ [41] | FoM_p = FoM − peak output power [19]

Δ: estimated from figure *: measured at 22.56 GHz #: Radiated power

and mmW VCO are excluded since they were used solely for testing purposes.

State-of-the-art performance of silicon-based synchronized THz source generators is summarized in Table II. Standard metrics for evaluating PLL performance include L_{norm}, FoM, FoM_T, $\text{FoM}_{JIT.N}$, FoM_{JRP}, and FoM_p. Compared to other works, this signal source achieves compelling phase noise and jitter performance while consuming low power. By suppressing more VCO phase noise through a larger f_{BW}, the attained σ_{rms} at mmW frequencies was at least 10 fs$_{rms}$ lower than our prior works [31], [32] while maintaining similar spurious tone level (i.e., −75 dBc). The signal source attains a small normalized spurious tone of −58.7 dBc normalized at 320 GHz. The two introduced calibration schemes enhance the robustness of ripple neutralization and ILFD injection locking while occupying an overall area of ~6.3%. Since both calibration techniques rely on the CRN-PD and a similar FSM, future work could integrate these building blocks to further reduce area and power consumption.

VI. CONCLUSION

This article reports a synchronized 292.2–321.4-GHz CMOS source generator. A CRN-PD is introduced, consuming no additional power, alleviating the tradeoff between spurious tone rejection and VCO phase noise suppression in an mmW PLL.

The CRN-PD has evolved to support VCO LD. A calibration scheme is introduced to enhance the robustness of ripple neutralization. Additionally, another calibration method is implemented for ILFD frequency alignment, improving its robustness. The THz source generator achieves an FoM of −234 dB while consuming 216.2–249.5 mW of power. The attained spurious tone level of −58.7 dBc ranks among the lowest in state-of-the-art works.

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