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# Muon-Induced SEU Cross Sections of 12-nm FinFET and 28-nm Planar SRAMs

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***Abstract*—While muon irradiation experiments have been reported in recent years, negative muon irradiation to FinFETs has not been reported. Negative muons have the unique physical property of muon capture reaction, and generated secondary ions have larger linear energy transfer (LET) than muons themselves. We performed positive and negative muon irradiation experiments on 12-nm FinFET and 28-nm planar SRAMs at MUSE in J-PARC. The negative muon-induced single event upset (SEU) cross section is more than ten times larger than that of the positive muon. The negative muon-induced SEU cross section of FinFETs decreases by the same ratio as neutron-induced one compared to planar SRAMs.**

***Index Terms*—Single event upset (SEU), Soft errors, FinFET, Muons, Neutrons, Static random-access memory (SRAM)**

## I. Introduction

Soft errors are a critical challenge for ensuring the reliability of advanced information systems in contemporary society. In terrestrial environments, soft errors occur when cosmic rays strike electronic devices, causing bit flipping and temporary malfunctions. Traditionally, the nuclear reaction between neutrons and silicon has been thought to be the primary cause of soft errors on the ground. On the other hand, recent semiconductor technology scaling has revealed through irradiation tests that muons, an elementary particle abundant in the terrestrial environment, may also be contributors [1]–[6].

B. D. Sierawski et al. show that positive muon-induced soft errors occur in CMOS SRAM memory at process nodes of 65nm, 45nm, and 40nm and tend to increase with process scaling [1]. N. Seifert et al. report positive muon-induced SEU cross sections of FinFETs [2]. As for negative muons, pioneering works on recent SRAMs [3], [4] report SEU cross sections of 65-nm bulk and SOI SRAMs. They show that negative muons have a much larger SEU cross section than positive muons due to negative muon capture reaction. Following works evaluated the negative muon-induced SEUs of 28-nm SRAM in [5] and 20-nm SRAM in [6]. Meanwhile, negative muon irradiation tests on FinFETs have not been reported in the literature. To clarify the impact of muons on the soft error rate (SER), it is necessary to evaluate the effect of negative muons on FinFETs.

This paper reports the results of positive- and negative-muon irradiation tests of 12-nm FinFET and 28-nm planar SRAMs at the Muon Science Facility (MUSE) in Materials and Life Science Experimental Facility (MLF), Japan Proton Accelerator Research Complex (J-PARC). This paper provides muon, especially negative muon, irradiation data for FinFETs. We also show a comparison with planar SRAMs.

## II. Experimental Setup

We conducted muon irradiation experiments at MUSE using 12-nm FinFETs and 28-nm bulk planar SRAMs. The irradiation target chips, fabricated using a 12-nm process node, are equipped with four types of SRAMs, while two types are at 28 nm. The 12-nm chip has a total bit size of 28.3 Mbits, whereas the 28-nm chip has 18.9 Mbits.

Figure 1 depicts the experimental setup, and Fig. 2 illustrates the setup consisting of a collimator, a plastic scintillator, and chips on a board placed upstream of the muon beam. The experimental board used in this study comprised 36 chips, 30 of which were irradiated, while six chips were used to measure the background effect. The collimator hole had dimensions of 56 mm x 50 mm. A plastic scintillator with a thickness of 500 um was utilized to count the number of irradiated muons. A uniform spatial spread was confirmed by a profiler camera.

The physical mechanism responsible for SEUs involves depositing an electric charge near a transistor, leading to a change in its state. The threshold amount of applied charge that causes bit inversion is called the critical charge ($Q_c$). Some muons are positively charged, and some are negatively charged. There are two distinct mechanisms by which muons induce SEUs: (1) direct ionization by charged positive and negative muons and (2) charge deposition by secondary ions generated through negative muon capture reactions. Therefore, negative muon-induced SEU is more likely to occur than positive muon-induced SEU because protons and alpha particles are generated from negative muon capture.

The critical charge depends on the operation voltage of the SRAMs. Then, we gave operation voltages of 0.30 V, 0.56 V, and 0.69 V to the 12-nm chip and 0.62 V, 0.77 V, and 0.90 V to

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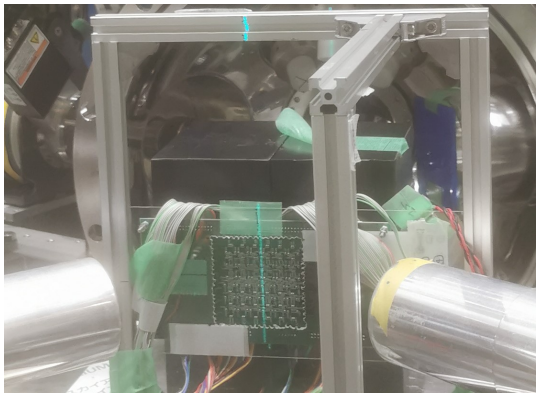

Fig. 1. Experimental system seen from the downstream side.

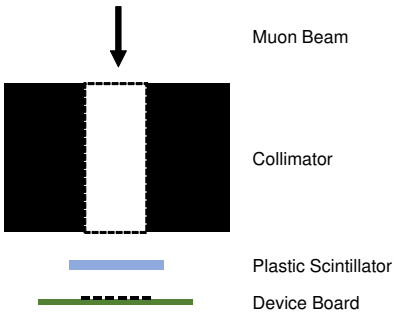


Fig. 2. Experimental setup seen from above.

the 28-nm chip. Note that the voltage difference between 12-nm and 28-nm chips originated from the unexpected voltage drop along the power line from the voltage source. Besides, a 0.30-V measurement of 12-nm SRAM was performed with 0.69 V read/write operations.

Our static test was carried out as follows. All 1 values were written to the SRAM, held for several minutes to a few hours, and compared to the initial values when the values were read back to measure the number of bit flips. Muons are most likely to cause bit flips when they stop near the SRAM transistor, as a large energy loss occurs and negative muon capture reaction occurs just after stopping. Therefore, the change in the SEU cross sections was obtained by sweeping the momentum of irradiation muon. Note that the muons in the beam have a momentum deviation of approximately 5% [3].

SEU can be classified into single bit upset (SBU) with one-bit inversion per event and multiple-cell upset (MCU) with two or more bit upsets per event. In this paper, an MCU is defined as a set of bit inversions in the surrounding eight cells.

## III. Experimental Results and Discussion

### A. SEU Cross Sections

Momentum scans were conducted for both 12 nm and 28 nm to determine the SEU cross sections. Figure 3 illustrates the momentum dependence of 12-nm and 28-nm devices on the SEU cross section for positive and negative muons at a supply voltage of 0.69 V (12 nm) and 0.77 V (28 nm), respectively. Here, there is no plot of 12-nm positive muon since no upset was observed in 1 hour irradiation of 33.9 MeV/c positive muons.

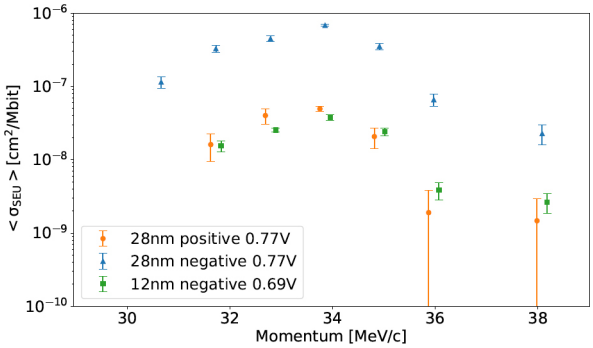


Fig. 3. Positive and negative muon momentum dependence of SEU cross section; 12-nm and 28-nm SRAM chips operated at voltages of 0.69 V and 0.77 V, respectively.

The SEU cross sections peaked at around 33.9 MeV/c for both 12 nm and 28 nm. For both devices, the negative muon-induced SEU cross section is more than ten times larger than the positive muon-induced cross section at the peak momentum. This result indicates that the direct ionization effect is not a dominant contributor to SEUs in both technologies. The critical charges of the 12-nm and 28-nm SRAMs are not small enough for an abundant number of muons passing through the devices to cause upsets.

Figure 4 shows the momentum dependence of 12-nm SRAM SEU cross sections at 0.30 V. Regardless of the supply voltage, the peak momentum is 33.9 MeV/c, similar to Fig. 3.

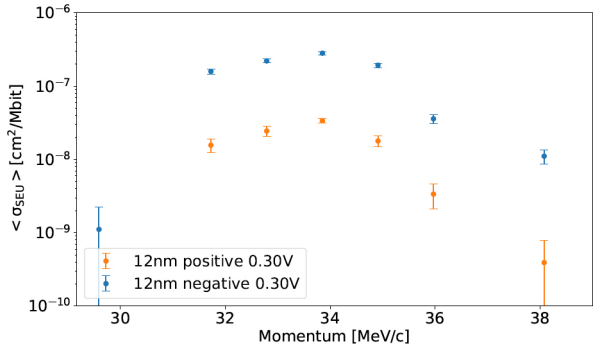


Fig. 4. Muon momentum dependence of SEU cross sections of 12-nm SRAM at 0.30 V.

### B. SEU dependency on operation voltage

Figures 5 and 6 show the SEU cross sections at 33.9 MeV/c of 12-nm and 28-nm SRAMs, respectively, as a function of operating voltage. Note that the 12-nm cross sections at 0.56V are for 32.8 MeV/c due to data missing. We can see the SEU cross section increases as the supply voltage decreases in both 12-nm and 28-nm SRAMs. This tendency is explained by $Q_c$ drop according to supply voltage decrease. On the other hand, the previous negative muon irradiation experiments conducted on 65-nm SRAM show that the SEU cross section is larger at 0.9 V than at 0.5 V [3]. The parasitic bipolar effect is more active in this 65-nm SRAM due to the triple-well structure.

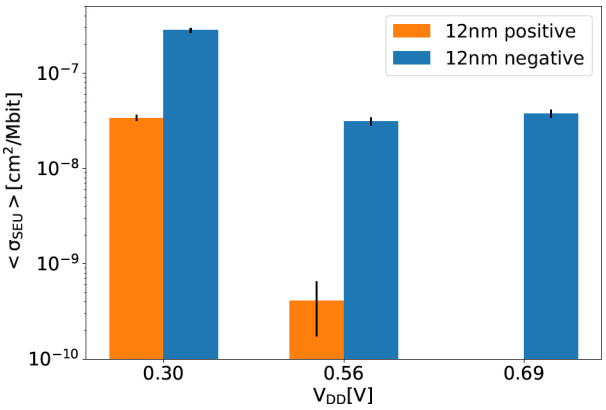


Fig. 5. 12-nm SEU cross sections versus operating voltage under positive and negative muon irradiation at 33.9 MeV/c. At 0.56V, the beam momentum is 32.8 MeV/c.

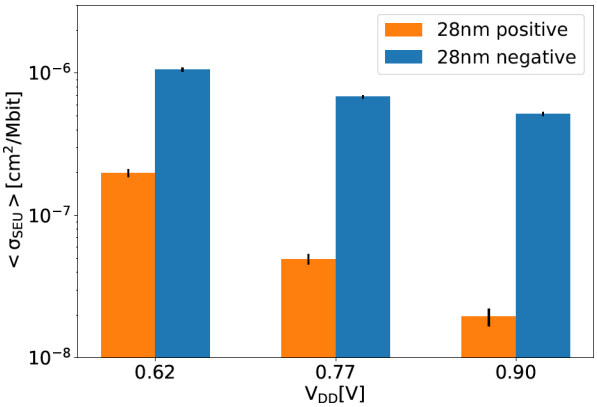


Fig. 6. 28-nm SEU cross section versus operating voltage under positive and negative muon irradiation at 33.9 MeV/c momentum.

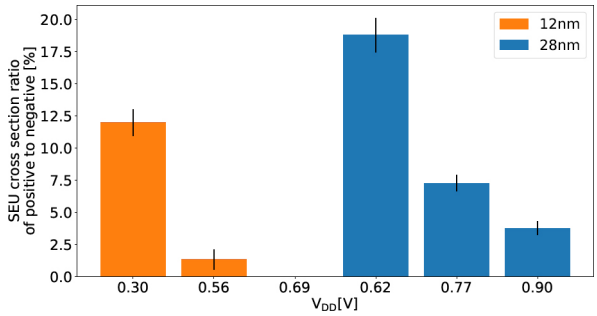


Fig. 7. Ratio of SEU cross section of positive muons to that of negative muons. The muon momentum is 32.8 MeV/C for 12nm SRAM at 0.56V and 33.9 MeV/c for the others.

Figure 7 shows the SEU cross section ratio of positive muons to negative muons. The ratio increases with decreasing voltage, meaning that direct ionization is becoming possible to cause upsets for smaller $Q_c$ values. However, the direct ionization-induced SEU is still insignificant in the 12-nm and 28-nm SRAMs.

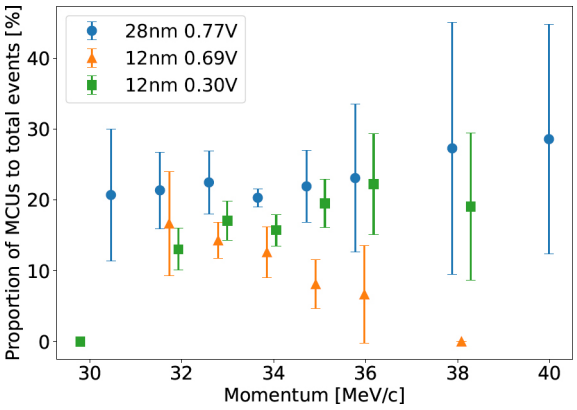


Fig. 8. Proportion of MCUs to total events under negative muon irradiation.

### C. MCU

MCUs are one of the most crucial reliability indicators since they can directly degrade the effectiveness of error-correcting codes. In negative muon irradiation, MCUs are generated more frequently than in positive muon irradiation since the secondary ions generated by negative muon capture have higher linear energy transfer (LET) than muons themself.

Figure 8 shows the ratio of the number of MCUs to that of all events. Compared to the 28-nm SRAM, 12-nm SRAM has a lower MCU ratio at all momenta, which may come from a fact that the process scaling reduces parasitic bipolar action (PBA). An interesting tendency in the figure is that the MCU ratio of 12-nm 0.69-V SRAM becomes lower as the momentum increases. Considering the MCU mechanism that an ion hits multiple sensitive volumes of adjacent SRAM cells, the MCU fraction is expected to peak when the momentum stops near the transistor since the dispersion during secondary ion production is isotropic. This result suggests that the primary mechanism of the 12-nm 0.69-V SRAM could be an ion passing through multiple cells. On the other hand, the 12-nm 0.30-V SRAM does not have a similar tendency. A possible reason might be that charge sharing is more dominant in the 12-nm 0.30-V SRAM. We will perform a simulation-based analysis in our future work.

Figures 9 and 10 show the distributions of the number of MCU bit flips in 12-nm and 28-nm SRAMs, respectively. It is found that PBA is weakened in 12 nm since only two- and three-bit MCUs are observed at 0.69 V. At a lower voltage, large-bit MCUs are observed in both technologies, whereas the opposite trend is found in a 65-nm device [3].

### D. Comparison between 12 nm and 28 nm

It has been reported that neutron-induced SEU cross sections drop significantly across the planar-to-FinFEET transition [7]. Figure 11 compares the 14.8-MeV neutron-induced SEU cross section in the National Institute of Advanced Industrial Science and Technology (AIST) [8] with the negative muon cross section of the same SRAM chips. The cross sections are normalized by the 28-nm cross sections. You

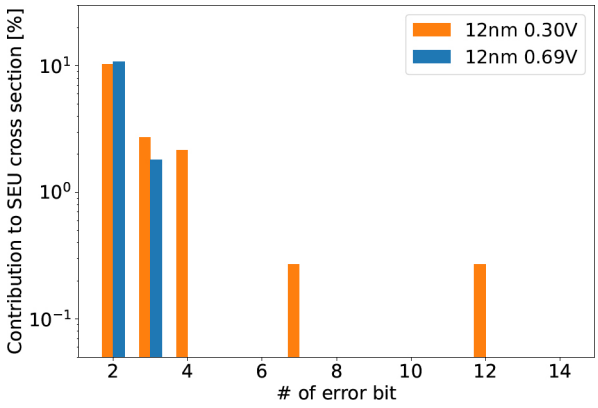


Fig. 9. Distribution of bit flip counts of MCUs in 12-nm devices. The supply voltage is 0.30 V and 0.68 V.

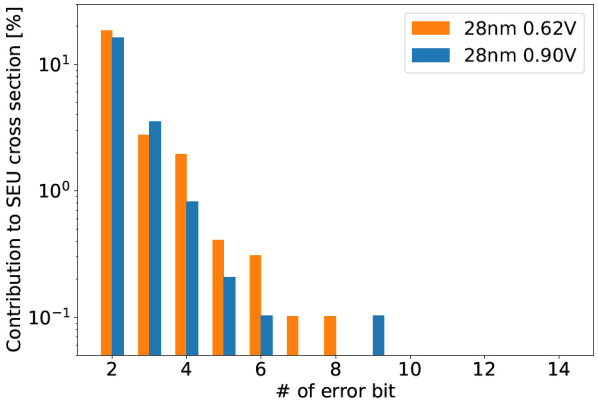


Fig. 10. Distribution of bit flip counts of MCUs in 28-nm devices. The supply voltage is 0.62 V and 0.90 V.

can see that the SEU cross section decreased at almost the same rate from 28-nm planar to 12-nm FinFET SRAMs. Meanwhile, as discussed with Fig. 7, the negative muon-induced SEUs are caused mainly by negative muon capture reactions, similar to reactions induced by neutrons. Therefore, it could be reasonable that a similar drop of SEU cross section is observed in negative muons and neutrons.

## IV. Conclusion

An experiment was conducted on 12nm FinFET and 28nm bulk planar SRAM to investigate the SEU under positive and negative muon irradiation. The SEU cross sections resulting from negative muon irradiation were approximately more than ten times larger than that from positive muon irradiation in both devices. The dependence on supply voltage was similar for both positive and negative muons, with the SEU cross sections decreasing as the supply voltage increased. The results suggest that negative muon capture reaction is dominant compared to direct ionization in our devices. The SEU cross section reduction from 28-nm planar to 12-nm FinFET SRAMs due to negative muons was similar to those

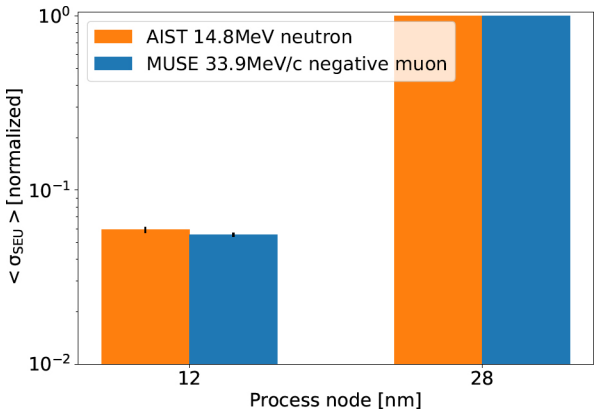


Fig. 11. 12-nm SEU cross section at 0.69 V normalized by 28-nm SEU cross section at 0.77V.

due to neutrons. Future work includes analyzing simulation-hardware correlation.

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