Design Guideline for Resistive Termination of On-Chip High-Speed Interconnects

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Abstract— **This paper discusses the resistive termination of on-chip high-performance interconnects. Resistive termination can improve the bandwidth of on-chip interconnects, on the other hands, increases the power dissipation. Therefore a design guideline for resistive termination is necessary. In this paper, we propose a method to determine the termination of on-chip interconnects. The termination derived by the proposed method provides minimum sensitivity to process variation as well as maximum eye-opening in voltage.**

I. Introduction

As the performance of LSIs improves, on-chip interconnects are becoming more and more important. One of the problems preventing the performance enhancement is on-chip global interconnects. Recently to attack this problem, high-speed signaling and throughput driven interconnection are becoming a hot research topic both in design and EDA communities [1], [2]. There are some approaches to realize the high-performance signaling and one of the common and fundamental techniques is the resistive termination. Conventionally, on-chip interconnects are connected to the receiver input directly. These interconnects are regarded as open-ended transmission-lines. However to achieve high bit rate signaling over 10Gbps, resistive termination is required [3]. On the other hand, resistive termination increases the power dissipation because static current flows through the terminator. Therefore designers have to carefully use resistive termination.

For PCB wires and cables, resistive termination is a common technique because impedance matching is important to prevent the multiple reflection of signal wave. However in LSIs, the loss of the wire is significant. Even if the multiple reflection occurs, the reflected wave attenuates while propagating on the interconnect. Therefore it is not clear in what condition we should use the resistive termination. Furthermore, process variation is becoming more and more important in LSIs. The on-chip resistance for termination realized by MOS or polysilicon varies due to process variation. Therefore robustness to process variation must be examined when designing high-performance interconnection.

This paper proposes a method to determine the terminator resistance adapted to use for on-chip lossy transmission-lines. We improve the analytical eye-opening estimation in Ref. [3]. Reference [3] provides the analytical performance estimation for only open-ended and impedance matched termination. In this paper, we derive a formula of the eye-opening with arbitrary termination. By using the derived formula, our method indicates the situations when the resistive termination should be used and the optimal value of termination resistance. Furthermore, our method provides the sensitivity to the variation of the termination resistance. From the sensitivity, designers can decide the design margin for process variation. The contribution of this paper is a design guideline of termination for high-speed on-chip interconnection that gives both the maximum eye-opening in voltage and minimum sensitivity to process variation.

Section II explains the effect of the resistive termination. In Section III, we derive the formula for analytical performance estimation. We then show a method to decide the optimal termination and derive the sensitivity to process variation in Section IV. Section V concludes this paper.

II. Impact of Resistive Termination

In this section, the effects of resistive termination are explained. We first explain the effect on signal waveform and then we discuss the power dissipation.

A. Signal waveform

We here demonstrate the effect of resistive termination on the signal waveform. Conventionally, the signal waveform swings from ground level to the supply voltage because on-chip interconnects are open-ended lines. By using resistive termination, the amplitude of the signal waveform becomes smaller than the supply voltage. It looks a demerit but resistive termination improves the eye-diagram in high bit rate region [3]. Figure 1 is the eye-opening voltage versus the signal bit rate. The interconnect is a co-planar structure and its characteristic impedance is 100Ω. The interconnect length is 10mm. The driver output impedance is adjusted to 100Ω. The supply voltage is 1V. In the case of the open-ended transmission-line, the eye-opening at low bit rate is large and close to the supply voltage. However as the bit rate becomes higher, the eye-opening degrades very rapidly. On the other hand, if the receiver side of the interconnect is terminated by a 100Ω resistor, we can obtain about 100mV eye-opening at 100Gbps signaling. Thus the resistive termination is necessary for high-speed signaling.

B. Power dissipation

The serious problem in using resistive termination is increase of the static power dissipation. When the resistor is connected between the signal line and the ground, static current flows through the terminator. Figure 2 shows the energy per bit of 20Gbps signaling. The interconnect is 5mm long and the characteristic impedance is 100Ω. The solid line is the simulation result of energy per bit when the resistive termination is used. In Fig. 2, the energy per bit of open-ended line is shown by the dashed-line. As shown in Fig. 2,

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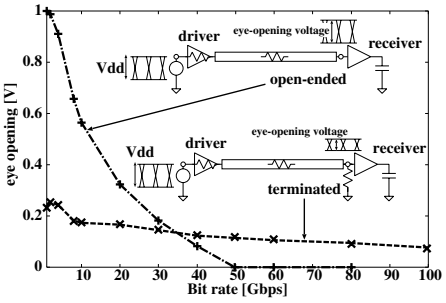

Fig. 1. Eye-opening versus signal bit rate (10mm length, $Z_0 = 100\Omega$).

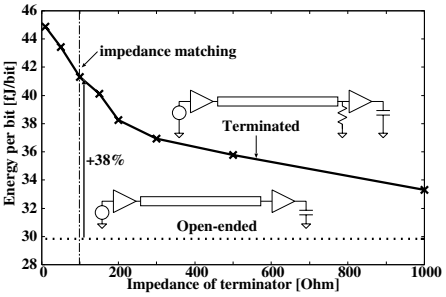

Fig. 2. Energy per bit and the resistance of the terminator (5mm length, $Z_0 = 100\Omega$, 20Gbps signaling).

resistive termination increases energy per bit. As the resistance of terminator becomes small, the power dissipation increases. When the terminator achieves impedance matching (100Ω), energy per bit increases by 38% from the case of open-ended.

When we use resistive termination, the energy dissipation increases as shown in Fig. 2. On the other hand, as shown in Section II-A, resistive termination does not necessarily improve the eye-diagram. Therefore we have to carefully use resistive termination.

III. Analytical Estimation of Eye-Opening

This section describes an analytical method to estimate the interconnect performance.

A. PieceWise-Linear waveform model

We here describe the piecewise-linear (PWL) waveform model proposed in Ref. [3]. This model assumes that the attenuation of the interconnects is the dominant factor that degrades the signal integrity. The circuit model of terminated transmission-lines is shown in Fig. 3. The resistance, inductance and capacitance per unit length are R, L and C respectively. The impedance Z_0 is the characteristic impedance of transmission-line. At the receiver side, the interconnect is terminated by the resister and the resistance value is R_t. At the driver side, we assume that the driver of the interconnect achieves impedance matching. In other words, the output impedance of the driver is equal to the characteristic impedance Z_0. For simplicity, the supply voltage V_{dd} is 1V. This assumption does not lack the generality because the circuit model in Fig. 3 is a linear circuit.

We model the waveform at the receiver side of transmission-lines by the PWL waveform model shown in Fig. 4. Figure 4 is the eye-diagram by two isolated pulse ($0\cdots010\cdots0$ and $1\cdots101\cdots1$). If the crosstalk noise is small, these isolated

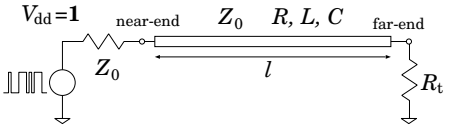

Fig. 3. Circuit model of a transmission-line with resistive termination.

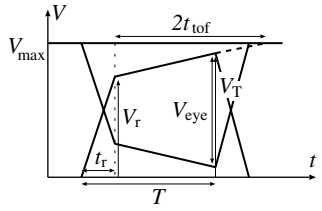

Fig. 4. PWL waveform model.

pulses determine the eye-opening. In Fig. 4, the time t_r is the transition time of input pulse and period T is the minimum width of input pulse. The voltage V_r is rise voltage that is determined from the attenuation and the termination of the interconnect. The voltage V_T is the voltage at the time T. The voltage V_T decides the maximum eye-opening voltage. The voltage V_{max} is the voltage level when the continuous "1" is input to the interconnect. The voltage V_{max} is determined by the resistance of the terminator, the resistance of the interconnect and the output resistance of the driver. The time t_{tof} is the signal time-of-flight that is determined from the interconnect length and the velocity of electromagnetic wave. From Ref. [4], if the driver achieves impedance matching, the voltage at the receiver side reaches V_{max} when the time $2t_{tof}$ passed after the rising. By using this characteristic, we can derive the voltage V_T.

From the PWL waveform model in Fig. 4, the maximum eye-opening voltage V_{eye} is expressed as

$$V_{eye} = \begin{cases} \max\{V_{max} - 2(V_{max} - V_T), 0\} & (T - t_r < 2t_{tof}) \\ V_{max} & (T - t_r > 2t_{tof}) \end{cases}. \quad (1)$$

Resistive termination changes the reflection coefficient and the maximum voltage V_{max}. Therefore designers can tune the eye-opening by using resistive termination.

B. Derivation of eye-opening voltage

The amplitude of the pulse injected to the interconnect is expressed as $V_{near} = V_{dd}/2 = 1/2$ because this paper assumes that the driver output impedance is equal to the characteristic impedance Z_0. The pulse attenuates as propagating on the lossy transmission-line. The amplitude of the attenuated pulse at the receiver side is expressed as

$$V_{far} = V_{near} \exp(-\alpha l) = n/2, \quad (2)$$

where the parameter α is the attenuation constant of the interconnect and the parameter n is the attenuation parameter defined as $n = \exp(-\alpha l)$. As the attenuation becomes weak, the parameter n becomes larger and if the line is lossless, the parameter n is equal to 1. Since the shunt conductance of the on-chip interconnects is small, the attenuation parameter n can be approximated to $n \simeq \exp(Rl/2Z_0)$ [5]. The reflection

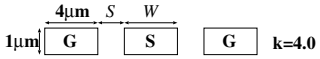

Fig. 5. Cross section of the co-planar structure.

coefficient Γ at the receiver side is expressed as $(R_t - Z_0)/(R_t + Z_0)$. Therefore the rise voltage V_r is calculated by

$$V_r = V_{far} \times (1 + \Gamma) = \frac{n}{2} \frac{2Z_n}{Z_n + 1}, \quad (3)$$

where the parameter Z_n is the normalized impedance defined as $Z_n = R_t/Z_0$. $Z_n = 0$ means short-circuit termination, $Z_n = 1$ means matched termination and $Z_n = \infty$ means open-ended. By using the normalized impedance Z_n, the maximum voltage V_{max} is expressed as

$$V_{max} = \frac{R_t}{Z_0 + Rl + R_t} = \frac{Z_n}{1 - 2\log n + Z_n}. \quad (4)$$

The voltage V_T is expressed as

$$V_T = V_r + (V_{max} - V_r) \frac{T - t_r}{2t_{tof}}. \quad (5)$$

From Eq. (5), the first equation of Eq. (1) is rewritten as

$$\begin{aligned} V_{eye} &= 2V_r + (V_{max} - V_r) \frac{T - t_r}{t_{tof}} - V_{max} \\ &= \left(\frac{Z_n}{1 - 2\log n + Z_n} - \frac{nZ_n}{Z_n + 1} \right) \left(\frac{T - t_r}{t_{tof}} - 1 \right) + \frac{nZ_n}{Z_n + 1}. \end{aligned} \quad (6)$$

The equation above is valid in the region $T < 2t_{tof}$. As mentioned in Eq. (1), the maximum eye-opening V_{eye} is equal to V_{max} in the region $T > 2t_{tof}$.

C. Verification by circuit simulation

We here show some experimental results for the verification of the proposed method. As an interconnect model, we assume the co-planar structure shown in Fig. 5. We vary the wire width W, the spacing S and the resistivity of the wire. The permittivity of the insulator is set to 4.0 and the time-of-flight t_{tof} of the 10mm wire is 66.7ps. We extract the frequency characteristics by a 2D field-solver. For circuit simulation, we model the interconnect by a model that can represent the frequency dependency [6]. On the other hand, the analytical method cannot handle frequency-dependence of the interconnect characteristics. We therefore have to choose the characteristics at a certain frequency. To choose the extraction frequency, we use the method based on the interconnect length [7]. When the interconnect length is 10mm, the extraction frequency is 3.75GHz. The random NRZ pulse whose transition time is one tens of the pulse width ($t_r = T/10$) is injected through the output resistance of the driver.

Figure 6 shows the maximum eye-opening voltage V_{eye} with various attenuation parameter n. The x-axis is the normalized impedance Z_n and the input bit rate is fixed to 20Gbps. In Fig. 6, the result of the proposed method and that of the circuit simulation are plotted. From the Fig. 6, the curves by the proposed method are close to the simulation results. Therefore the proposed method is valid to estimate the eye-opening voltage. Figure 6 also shows that the eye-opening

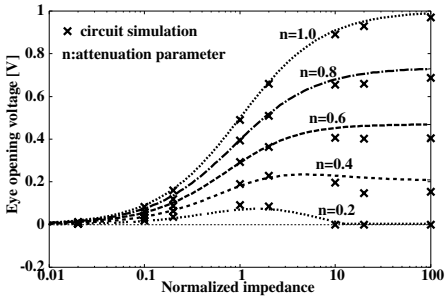

Fig. 6. Eye-opening voltage versus the normalized impedance (with various attenuations, 20Gbps input, 10mm length)

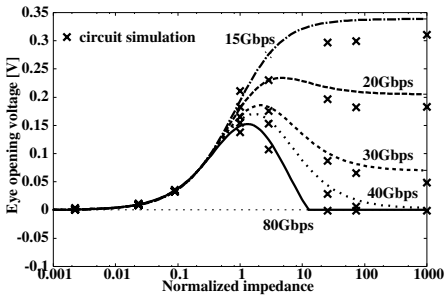

Fig. 7. Eye-opening voltage versus the normalized impedance (with various bit rate, $n = 0.4$! $10mm length)

has maximal value at a certain termination resistance under strong attenuation. When the attenuation is weak ($n \geq 0.6$), the eye-opening is large as the normalized impedance is large. This means that the open-end termination maximizes the eye-opening. However as the attenuation becomes strong ($n \leq 0.4$), the eye-opening becomes maximum at a certain normalized impedance. The border of the region where the resistive termination is effective is discussed in the next section.

Figure 7 shows the plot of the eye-opening voltage versus the normalized impedance. The attenuation parameter n is fixed to 0.4 and the input bit rate is varied from 15Gbps to 80Gbps. Figure 7 also shows that the proposed method is close to the results of the circuit simulation. When the bit rate is low, the eye-opening monotonically increases as the normalized impedance increases. As the bit rate becomes higher, the maximum value appears and the normalized impedance that makes the eye-opening maximum becomes smaller. At the 40Gbps or higher, the eye-opening of open-ended ($Z_n = \infty$) transmission-lines becomes almost zero. On the other hand, if the termination is adjusted to the optimal value, the eye-opening is over 150mV at the 80Gbps. From Fig. 6 and Fig. 7, the resistive termination is necessary when the attenuation is strong and the input bit rate is high.

IV. Design Guideline for Resistive Termination

This section describes a method to choose the optimal resistance of the termination. The formula derived in previous section provides a design guideline that indicates when the resistive termination should be used. We verify that the termination given by the guideline is superior also in robustness.

A. Termination for maximizing the eye-opening voltage

The resistance value where the eye-opening becomes maximum is derived from the derivative of Eq. (6). From the solu-

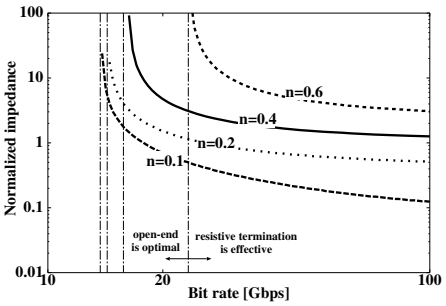

Fig. 8. Optimal normalized impedance versus signal bit rate.

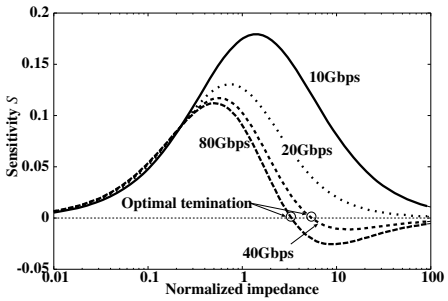

Fig. 9. Sensitivity to the variation of the resistance (attenuation $n = 0.6$! $ 10mm length interconnect)

tion of an equation $\partial V_{\rm eye}/\partial Z_{\rm n} = 0$, the normalized impedance that makes eye-opening maximum is expressed as

$$\begin{aligned} Z_{\rm n} = &\left[(1-2\log n)\{(1-\tau)-n(2-\tau)\}\right. \\ &\left.-\left|-2\log n\right|\sqrt{n(1-2\log n)(1-\tau)(2-\tau)}\right] \\ &/\{(\tau-1)(1-2\log n)+n(2-\tau)\}, \end{aligned} \tag{7}$$

where we define a parameter τ as $\frac{T-t_{\rm r}}{t_{\rm tof}} = \tau$ for simplicity. If the denominator of Eq. (7) closes to zero, the optimal normalized impedance reaches an infinity value. The bit rate where the denominator becomes zero is calculated from an equation

$$\frac{T-t_{\rm r}}{t_{\rm tof}} = \frac{1-2n-2\log n}{1-n-2\log n}. \tag{8}$$

This equation indicates a critical bit rate. When the bit rate is higher than the critical rate, resistive termination is effective, and otherwise open-ended termination is optimal.

Figure 8 shows the relationship between the bit rate and the optimal normalized impedance. The curves are the optimal normalized impedance and the vertical dashed lines are the borders determined by Eq. (8). From Fig. 8, the optimal normalized impedance becomes smaller as the bit rate becomes higher. The optimal normalized impedance also depends on the attenuation. The region where the resistive termination is effective is larger when the attenuation is strong (the attenuation parameter n is small). From the discussion above, the resistive termination is more effective where the bit rate is high and the attenuation is strong.

B. Sensitivity to the variation of resistance

In recent design, taking process variation into account is significantly important and the discussion on the sensitivity to the variation is necessary to decide the design margin.

The derivative of Eq. (6) means how the eye-opening changes when the normalized impedance changes. We therefore can use this derivation as an indicator of the sensitivity to the resistance variation. We define the sensitivity of eye-opening to the variation of resistance value as

$$S = \frac{Z_{\rm n}}{V_{\rm dd}}\frac{\partial V_{\rm eye}}{\partial Z_{\rm n}}. \tag{9}$$

The sensitivity S means the eye-opening variation in the percentage of the supply voltage when the resistance value of terminator changes 1%. If the terminator has the optimal resistance determined by the method in Section IV-A, the sensitivity S is equal to zero. Therefore the optimal resistance that makes the eye-opening maximum is also optimal from the viewpoint of process variation.

Figure 9 shows the sensitivity S and the normalized impedance. From Fig. 9, the normalized impedance where the sensitivity becomes maximum is smaller than the optimal normalized impedance. The sensitivity becomes maximum where $Z_{\rm n} = 1.2$ at 10Gbps and $Z_{\rm n} = 0.5$ at 80Gbps. Therefore the termination whose resistance value is smaller than the optimal is sensitive to process variation. As mentioned in Section II-B, smaller terminator resistance increases the power dissipation. From the discussion above, designers should not use smaller terminator resistance than the optimal resistance, because all performance metrics, tolerance to process variation, power dissipation and eye-opening degrade.

V. Conclusion

This paper proposes a method to determine the resistance of the termination. The proposed method is based on an analytical eye-opening estimation and provides the optimal termination that makes the eye-opening maximum. The proposed method provides a design guideline of resistive termination from the fundamental parameters, i.e. bit rate, characteristic impedance and attenuation. Therefore the proposed method is especially efficient at the early stage of circuit design. The proposed method also provides the sensitivity to the variation of the terminator resistance. By using the proposed method, designers can decide the termination of the signal wire and the design margin for the variation of the resistance value.

Acknowledgement

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