Measurement and Analysis of Delay Variation due to Inductive Coupling

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***Abstract*— Inductive coupling is becoming a design concern for global interconnects in advanced technologies. This paper discusses interconnect delay variation due to inductive coupling. We first examine the difference in delay change curve with respect to relative transition timings of aggressors and victim between with and without considering inductive coupling by simulation. We verify that the difference in delay change curve due to inductive coupling is also observed in measurement of test chips.**

I. Introduction

In nano-meter technologies, interconnect delay dominates gate delay and accurate estimation of interconnect delay becomes more important. Capacitive crosstalk noise is a well known factor that causes interconnect delay variation. In recent processes, inductive coupling is predicted to be one of obstacles for accurate delay estimation because of progressive improvement in circuit operation speed. The impact of inductive crosstalk emerges in global and clock interconnects with lower resistance and longer interconnect length [1], [2].

Several works have verified correlation between measurement results and simulation results for capacitive coupling noise [3]–[5]. On the other hand, although inductive coupling noise is widely studied mainly based on simulation [6]–[8], correlation between simulation and measurement has been reported only in a few papers [2]. Measurement in frequency domain and TDR/TDT (time domain reflectmetry/transmission) measurement are performed, but the measured interconnect structure is much different in length, width, and number of coupled wires from interconnects actually integrated in current technologies owing to limitation of measurement equipments. A work [9] measured effect of self-inductance on delay, but coupling effect is not evaluated. To measure waveforms of inductive coupling noise, Refs. [10], [11] developed a measurement circuitry. However, in the fabricated chip, inductive coupling noise is not observed, and its reason is not clearly discussed.

In this work, we evaluate impact of inductive coupling on interconnect delay in a 90nm technology both by simulation and by measurement. The contribution of this work is to reveal the following two things: (1) impact of inductive coupling on timing is limited such that the overview of delay change curve with respect to transition timings of aggressors and victim is not totally different with that of capacitive coupling only though there some differences, and (2) focusing on the differences unique to inductive coupling, the measured delay change curve is close to the simulation results by using RLC-distributed coupled interconnect model rather than RC-distributed coupled model.

II. Impact of inductive crosstalk noise on interconnect delay

This section discusses influence of inductive coupling on interconnect delay.

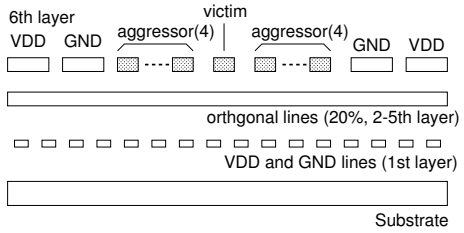

Fig. 1. Bus structure for evaluation.

We use a bus structure for crosstalk noise evaluation. We assume a 90nm CMOS process with six metal layers. The wire material is copper. The supply voltage is 1.0V. The interconnect cross-section is shown in Fig. 1. A victim and eight aggressor interconnects are aligned at the sixth metal layer for global interconnection. The center wire of the nine coupled wires is victim and the others are aggressors. To clearly observe inductive crosstalk noise, both interconnect width and spacing are set to 4μm. This interconnect structure is the same with that in the fabricated chip discussed in the next section. RLC of interconnects are extracted by a 3D field solver [12]. Silicon substrate is not considered in RL extraction, because wires in the first layer run in parallel to the bus wires, and the magnetic field is shielded. A frequency-dependent coupled transmission line model [13], [14] is used for the victim and aggressor interconnects in circuit simulation.

Figure 2 shows the far-end noise waveform at the center line of nine coupled lines when all aggressors make rise transition. The length of interconnects is 1400μm. The solid line is the simulation result considering both inductive and capacitive coupling, and the dashed line corresponds to capacitive coupling only. In the simulation of capacitive coupling only, we use a common RC-distributed coupled interconnect model, that is a finely-segmented RC ladder circuit with coupling capacitances. In the case of inductive and capacitive coupling, a sharp spike, which is a big difference from capacitive coupling only, is followed by a gentle bump. The gentle bump is close to the noise of capacitive coupling only except time offset. The spike width is basically determined by the interconnect length and the difference in propagation speed of different mode noises [8]. In the example of Fig. 2, the spike

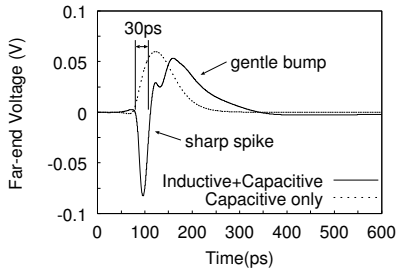

Fig. 2. An example of far-end noise waveform at the center line of nine coupled lines.

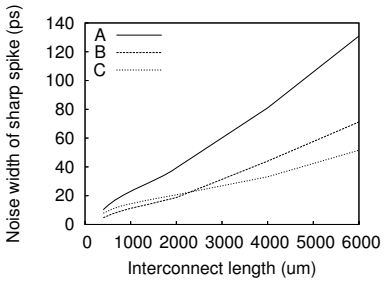

Fig. 3. Relation between noise width of sharp spike and interconnect length.

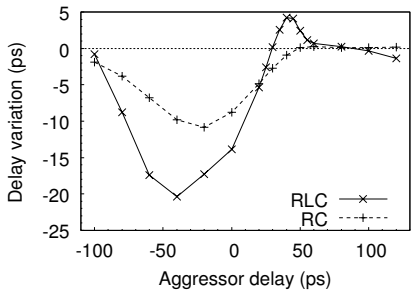

Fig. 4. Comparison of delay change curve between RLC and RC models.

width is about 30ps.

The peak voltage of the sharp spike depends on interconnect length, spacing and so on. A primary factor that determines the width of the spike is interconnect length. Figure 3 shows the dependency of spike width on interconnect length. There are three curves with different driver size and wire width. For A and B, the wire width is 4μm, and it is 1μm in C. The driver output impedance in the case of A is 170 Ω and that of C is 340Ω, which are twice larger than the characteristics impedance of the interconnects. In the case of B, the driver output impedance is 680Ω. Figure 3 shows that the spike width is proportional to interconnect length. In recent designs, long interconnects are divided into several 0.5-2 mm interconnects by repeater insertion. Though there is difference according to interconnect width and driver size, the spike width of 0.5-2mm long interconnects is 5-40ps.

We vary the relative transition timing of the victim and aggressors, and evaluate the delay variation. Figure 4 shows so-called delay change curve, that is the relationship between the relative transition timing and delay variation. The solid line is the delay variation considering both inductive and capacitive coupling, and the dashed line corresponds to capacitive coupling only. The differences we can see are:

- magnitude of delay variation caused by capacitive coupling only is smaller.
- timing when the amount of delay variation becomes maximum is slightly different.
- with both inductive and capacitive coupling, delay increase is observed.

The second difference can be explained by the time offset of the gentle bump in Fig. 2. The third difference of delay increase is caused by the sharp spike. When the sharp spike overlaps the victim transition, the interconnect delay increases because the victim transition direction is opposite to the spike. We find that the delay increase is relatively small though the voltage magnitude of the spike is larger than that of the gentle bump. The impact of inductive coupling on delay is not as significant as we expected from the noise waveform in Fig. 2.

To clarify the reason, we evaluate noise immunity of a receiver gate to the sharp spike, because if a receiver gate has good noise immunity, the sharp spike does not affect interconnect delay strongly even though the voltage magnitude of the spike is significant at the far-end of interconnects. Here inverters are used for evaluation because inverters are commonly inserted as repeaters. We inject a triangle waveform to the receiver, and evaluate the output waveform of the receiver as shown in Fig. 5.

Figure 5 shows the amplitude of the output waveform under various DC input voltage of the receiver. The inverter size of the receiver is 8X and the output load is a 1X inverter. The x-axis is the DC bias voltage of the receiver input. The height of triangle wave is set to 0.1V, since the peak noise voltage in 1mm-long wires is 0.1V in the bus structure of Fig. 1. The spike width is 5ps, 10ps, 20ps, and 40ps, which correspond to 0.5mm-2mm length interconnects. We think that 1mm-long interconnects are frequently used in this 90nm process, and the typical spike width is 20ps. From Fig. 5, the amplitude of the output waveform becomes maximum when input DC voltage is 0.5V. The range of DC input voltage in which the noise propagates through the receiver gate is limited, and when DC input voltage is below 0.4V and above 0.7V, the injected noise is almost filtered out. In addition, a shaper noise, i.e. a noise with smaller noise width is easily filtered out, since the receiver gate behaves as a low-pass filter. This effect of low-pass filter becomes significant as the output loading of the receiver gate increases because the time constant of the filter becomes large.

We vary the output loading of the receiver from 1X to 32X inverter, and evaluate the output waveform. Here, the receiver size is 8X. The results in Fig. 6 indicate that when the receiver has fanout-4 (32X) loading, the sharp spike whose width is 20ps is not amplified, even though the DC input voltage is 0.5V. From the above results, the interconnect delay variation by the sharp spike does not tend to be a serious problem.

III. Measurement circuit design

To verify the discussion in the previous section, we design a circuit to measure the delay change curve. This section explains the measurement circuit implemented on test chips fabricated in a 90nm CMOS process with six metal layers.

A. Measurement circuit structure

The measurement circuit consists of a ring oscillator, nine coupled lines, variable delay, and a counter. There is one victim line at the center of the coupled lines, and the other lines are aggressor lines. The interconnect structure is shown in the Fig. 1. The ring oscillator includes the victim line, and the variation of the propagation delay of the victim line is observed as the variation of the oscillation frequency. The counter counts the toggles of the ring oscillator in a given

operation time, and the time cycle of the ring oscillator is calculated from the counter value.

The relative transition timing of the aggressors and victim can be varied independently by changing the number of the inserted inverters in the part of variable delay by control signals. We can vary the relative timing from -7 to 7 in unit inverter delay, where the timing difference is even, the transition directions of the aggressor and the victim is the same, and when it is odd, the direction is opposite. In this technology, the unit inverter delay is 13ps. We can also set each aggressor quiet independently.

In our implementation, the control and counter signals are stored in scan-chained flip-flops, and we can set and get signals in flip-flops serially. Therefore this measurement can be easily performed by a pattern generator and a logic analyzer, because all signals are digital and the IO speed of few MHz is fast enough. To provide stable power supply voltage, we place a large amount of decoupling capacitance under bus wires.

B. TEG configurations

We designed and fabricated three configurations of the measurement circuits whose interconnect structure and driver/receiver size are different.

TEG_small_driver
: The sizes of driver and receiver are 8x and 8x. The width and spacing of the wires are 4μm.

TEG_large_driver
: The sizes of driver and receiver are 32x and 8x. The width and spacing of the wires are 4μm.

TEG_narrow_wire
: The sizes of driver and receiver are 16x and 8x. The width and spacing of the wires are 1μm and 4μm.

The wire length in all TEGs is 1.4mm, and it is common length for global interconnects. In TEG_small_driver, the driver output impedance is eight times larger than the characteristics impedance of the interconnects, and hence it is expected that less inductive effect will appear. On the other hand, the stronger effect of inductive coupling is expected to observe in TEG_large_driver. TEG_narrow_wire aims to measure the effect of inductive coupling in narrower wires whose width is more popular for global interconnection.

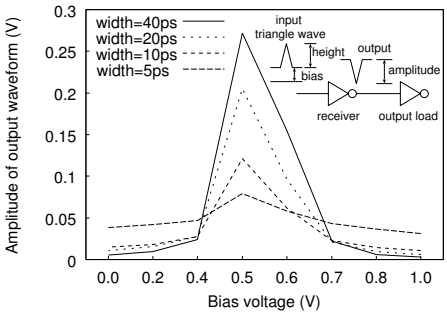

Fig. 5. Noise immunity evaluation (noise width is varied).

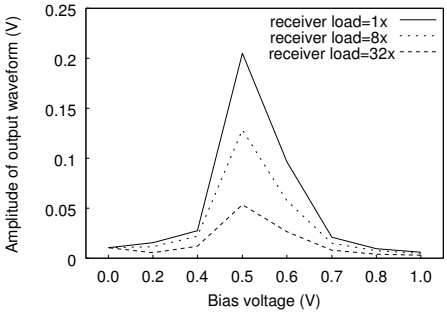

Fig. 6. Noise immunity evaluation (receiver load is varied).

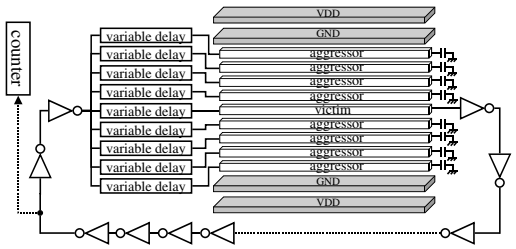

Fig. 7. The structure of measurement circuit.

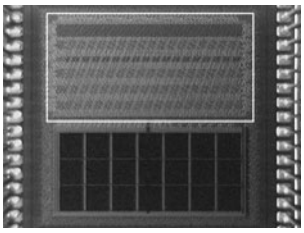

Fig. 8. Micrograph of the fabricated chip. The measurement circuits are located at the upper half of the chip. The chip size is 2.4mm x 2.4mm.

IV. Measurement result and duscussion

We measured the delay variation caused by coupling noise with the fabricated chip described in section III. The chip micrograph is shown in Fig. 8. We measured the cycle time of the ring oscillator both when aggressors are quiet and when aggressors are activated, and computed the delay variation. Figures 9-11 show the measurement results when all aggressors change in the same direction with the victim. We vary the relative transition timing of the victim and the aggressors, where the timing of aggressors is changed simultaneously. The x-axis is the relative transition timing normalized by the unit inverter delay. Figures 9-11 also show the result of circuit simulation. In these figures, "RLC model" means that interconnects are modeled as a frequency-dependent RLC-distributed coupled interconnect model [13], [14]. and "RC model" means that interconnects are modeled as an RC-distributed coupled interconnect model, which is commonly used for analyzing capacitive coupling noise.

Because the victim and all aggressors change in the same direction, the sharp spike in Fig. 2 increases the delay, and the gentle bump, to the contrary, decreases the delay. Several positive delay values are observed both in RLC model and the measurement result. For example, when the relative timing difference is 4 unit inverter delay in Figs. 9, 11, delay increase is observed in TEG_large_drive and TEG_narrow_wire, although the simulation with RC model estimates delay decrease. Figure 12 shows the simulated waveforms at the far-end and the receiver output in TEG_large_drive. A sharp spike

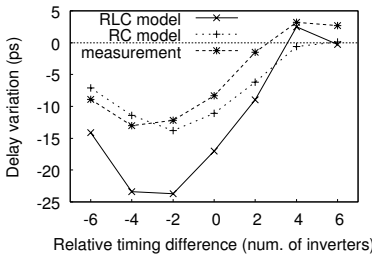

Fig. 9. Delay change curve of TEG_large_driver.

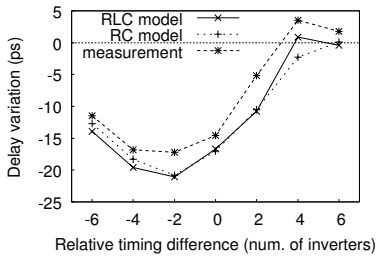

Fig. 11. Delay change curve of TEG_narrow_wire.

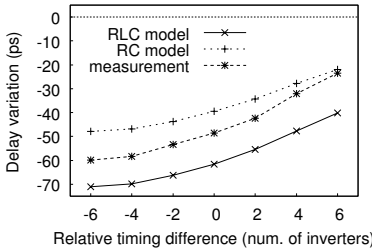

Fig. 10. Delay change curve of TEG_small_driver.

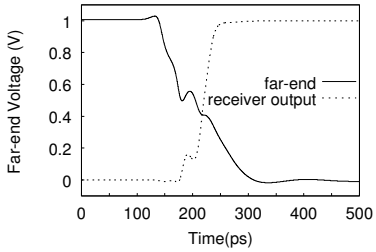

Fig. 12. Waveforms at far-end and receiver output.

is superposed on the victim transition around 0.5V, and hence the output transition of the receiver is delayed. We think that the delay increase is consistent with the simulation result, and inductive coupling noise emerges in the actual chip.

As discussed in Section II, there exists a timing offset between the gentle bump noise estimated with inductive and capacitive coupling and that only with capacitve coupling. This timing offset causes the relative timing difference that makes the amount of delay variation maximum, which is found in Fig. 4. The timing of maximum delay variation of RLC curve is earlier than that of RC curve. In case of Fig. 9, the peak timings of RC model and RLC model are roughly -2 and between -2 and -4 respectively. The peak timing of measurement is about -4, which is close to that of RLC model. Although the absolute values of the measured delay variation do not perfectly agree with the simulation results, we think that phenomena due to inductive coupling arise in real chips, and hence the simulation results with RLC interconnect model are closer to the measurement results.

V. Conclusion

In this paper, we discussed interconnect delay variation caused by inductive coupling, focusing on delay change curve with respect to relative transition timings of aggressors and victim. We show that delay increase happens in certain timings even though all aggressors and victim switch in the same direction, which can not be observed as long as only capacitive coupling is considered. We experimentally demonstrate that a sharp spike due to inductive coupling tends to attenuate by receiver gates, and hence its impact on delay is not significant.

In order to verify the above discussion based on simulation, we fabricated and measured test chips. The measured delay change curves follow the features that come from inductive coupling, and the simulation with RLC model provides better estimation than that with RC model.

Acknowledgement

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