Characterization and Understanding of Cosmic Ray-Induced Soft Errors in SRAMs

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Abstract— **This paper reviews soft errors in SRAM at ground level, focusing on neutron-induced soft error rates (SER) and muon-induced single event upsets (SEUs) across different SRAM technologies. The study explores SER characterization methods for terrestrial environments using accelerator facilities, presenting new findings on muon-induced SEUs in 12-nm FinFET, 28-nm, and 65-nm planar SRAMs.**

Keywords-soft error; VLSI; neutron; muon; single event upset; SRAM

I. INTRODUCTION

Soft errors caused by cosmic rays are increasingly recognized as a threat to the reliability of integrated circuits, particularly as Society 5.0 seeks to develop highly reliable systems. These errors pose a significant challenge, especially for AI systems, which are being integrated into critical applications such as autonomous driving and nursing robots. As a result, there has been a growing focus on assessing the reliability of neural networks and their hardware, with extensive studies conducted in this area (e.g., [2-7]). A comprehensive survey of this research domain can be found in [8].

In the terrestrial environment, soft errors are caused by alpha particles from packaging materials and neutrons from cosmic rays. Alpha particles, as ionized radiation, directly generate electron-hole pairs, while neutrons induce soft errors indirectly through reactions with transistor materials, producing charged secondary particles like protons and alpha particles. These particles create electron-hole pairs, and the collected charge at the transistor's drain causes a temporary glitch, leading to soft errors. A glitch in a combinational circuit is called a single event transient (SET), while one that upsets memory is called a single event upset (SEU). Alpha-induced soft errors can be reduced with low-emission packaging, but neutrons, which are harder to block, remain a major source of soft errors in terrestrial environments.

Digital System-on-Chips (SoCs) consist of SRAMs, flip-flops (FFs), and combinational logic. SRAMs are known to be the most sensitive components [9], so the focus here is on SEUs in SRAM. However, when SRAMs are protected by error-correction codes (ECC), FFs become the most vulnerable [9]. If radiation-hardened FFs are used [1], SETs can become a serious concern. In this case, SETs, including the more problematic single event multiple transients (SEMTs) [10], propagate through logic gates, making them very difficult to mitigate [11].

In recent years, neutrons have been identified as a major cause of soft errors in integrated devices, leading to extensive research and development focused on mitigating neutron-induced errors. Recent studies [12] highlight that muons are a potential source of soft errors in terrestrial environments. There are two types of muons: negative and positive. Muons could comprise a significant portion of ground-level secondary cosmic rays, accounting for about three-quarters of the total cosmic ray flux. According to [13], a sharp increase in muon-induced SEUs is predicted when the critical charge—the threshold charge required to cause an SEU—reaches a certain point. As transistors continue to shrink and operate at lower voltages, concerns about muon-induced soft errors are growing.

This paper examines neutron-induced soft error rates (SER) in SRAM for terrestrial environments, focusing on SER characterization methods using accelerator facilities. Additionally, we present recent findings on muon-induced SEUs in 12-nm FinFET, 28-nm, and 65-nm planar SRAMs.

II. NEUTRON

Neutrons have long been a major source of SEUs, and numerous measurement results have been reported. For instance, the effects of low-voltage operation, including subthreshold operation, have been analyzed [14-17]. One study experimentally demonstrates a sudden increase in SER when secondary protons deposit sufficient charge to cause SEUs [15]. Additionally, the angular dependency of neutron irradiation on error patterns has been observed (e.g., [18, 19]), as these patterns significantly influence the effectiveness of ECC.

Acceleration tests using spallation neutron beams with energy spectra similar to terrestrial neutrons are commonly used to estimate SERs. However, as noted in JESD89B [20], only a few facilities offer suitable neutron spectra. Another method in [20] uses the four-parameter Weibull function to fit SEU cross-section data from (quasi-)mono-energetic neutron or proton sources. This approach, however, requires at least four data points at different

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energies, making it costly. To address this issue, we have developed a new method for estimating terrestrial SER [21]. This approach uses a one-time irradiation test with any neutron source, combined with Monte Carlo simulations using tools like the Particle and Heavy Ion Transport code System (PHITS) [22] and Geant4 [23]. Applying this method, we estimated the terrestrial SER for 65-nm bulk SRAM across various conditions and facilities, finding that the ratio between the minimum and maximum estimated SERs was 1.8. This method allows using any neutron source for SER evaluation, helping to alleviate the beamtime shortage at atmospheric neutron facilities.

We examined the effect of irradiation direction on SEU cross sections in 65-nm bulk SRAM. The number of SEUs from board-side quasi-monoenergetic neutron irradiation was 20% to 30% lower than those from the plastic package side [24]. Monte Carlo simulations revealed that the SER for plastic package-side irradiation was nearly double that of board-side irradiation. The simulations also showed that the material composition in front of the memory chip significantly influences SER. Specifically, hydrides, such as plastic, significantly increase SER due to the higher production of secondary H ions from neutron-hydrogen elastic scattering [24, 25].

Recent devices have become more sensitive to neutrons with energies below 10 MeV, whereas the acceleration factor is typically based on the number of neutrons above 10 MeV. For 65-nm SRAM, the SER contribution from low-energy neutrons is estimated to be less than 6% in the terrestrial environments of New York and Tokyo [26]. In this case, excluding neutrons below 10 MeV in the acceleration factor calculation during accelerated neutron tests, as per the JESD89 standard, may still yield reasonably accurate SER estimates, as noted in [27]. However, for 12- and 28-nm SRAMs, low-energy neutrons in the 1 to 10 MeV range contribute approximately 18% to the total SER, which could result in significant estimation errors. For these advanced nodes, a lower energy threshold, such as 2 MeV for 12-nm SRAM, is more suitable for accurate SER estimation [28].

III. MUON

We conducted both positive and negative muon irradiation experiments on SRAMs at J-PARC MUSE. While several studies have reported on positive muon irradiation (e.g., [12]), [29, 30] are the first to explore negative muon irradiation, making our experiments groundbreaking. The results for 65-nm SRAMs [29-34] confirm that muons can indeed induce soft errors, with negative muons having a greater impact than positive muons. This is attributed to the physical process where negative muons are captured by atomic nuclei, leading to increased error rates.

Following the 65-nm experiments, we conducted positive and negative muon irradiation experiments on 28-nm, 20-nm, and 12-nm SRAMs [35, 36, 37]. While similar observations were made as with the 65-nm SRAMs, we did not observe a significant increase in the SEU cross section. As transistor structures shift to FinFET, the sensitive volume decreases due to its 3D architecture, leading to reduced charge deposition. This trend is consistent with neutron-induced SEUs [37]. However, when the supply voltage is lowered, the SEU cross section for positive muons increases significantly in 12-nm SRAM. This suggests that once the critical charge drops below a certain threshold, muon-induced soft errors originating from direct ionization could become dominant, as discussed in [13] through simulations.

IV. CONCLUSION

This paper discussed soft errors in SRAM at ground level. First, we examined neutron-induced soft error rates (SER) in SRAM in terrestrial environments, with a focus on SER characterization methods using accelerator facilities. Next, we presented recent findings on muon-induced SEUs in 12-nm FinFET, 28-nm, and 65-nm planar SRAMs.

Future work includes further validation of the proposed neutron-induced SER characterization method [21], which combines simulations with a one-time irradiation experiment using an arbitrary neutron source, applied to more advanced transistors and SOI devices. For muons, we are investigating the impact of high-speed muons passing through chips, as their numbers far exceed those of muons stopping in chips. Another issue to be addressed is the challenge of defining the sensitive volume in 3D transistors for a wide LET range of ions and muons [38, 39].

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