An 88.5 fs_{rms} Integrated Jitter and −76.2 dBc Reference Spur mmW PLL Utilizing a Ripple Compensation Phase/Frequency Detector

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***Abstract*— Millimeter-wave (mmW) phase-locked loops (PLLs) typically favor a wide loop bandwidth for stronger suppression of the out-of-band phase noise from a voltage-controlled oscillator (VCO). Unfortunately, doing so lowers the degree of attenuation to the PLL reference spurs. This paper proposes a ripple compensation phase detector (RCPD) for extending PLL loop bandwidth and phase noise suppression without sacrificing reference spur performance. The RCPD inherently consists of a pair of PDs that generate respective ripple simultaneously, with each PD's ripple current compensating the other, resulting in a glitch-free RCPD output. A calibrator is also introduced to reduce device mismatches. With the proposed techniques, the proposed mmW PLL was implemented using 22 nm bulk CMOS technology. The mmW PLL operates from 32.7 to 39.4 GHz, achieving an integrated jitter and reference spur of 88.5 fs_{rms} (1 kHz to 100 MHz) and –76.2 dBc, respectively, with a figure-of-merit (FoM) of –247.5 dB.**

***Index Terms*— Calibration, CMOS, millimeter-wave (mmW) circuit, phase-locked loop (PLL), phase/frequency detector (PFD), phase noise, reference spur.**

I. Introduction

THE era of big data has witnessed a dramatic increase in data rates over the last decade, with rates boosted beyond 112 Gb/s for wireline and wireless interconnects [1], [2], [3]. To enable such high data throughput, a frequency synthesizer, typically realized by a phase-locked loop (PLL), has become essential for generating a low-jitter and low-reference-spur clock. Low-jitter performance is critical for extending the recovered eye opening in wireline links and achieving low error vector magnitude (EVM) in wireless communication, while low-reference spur helps attenuate out-of-band energy aliasing [4]. Additionally, due to systematic power budget constraints, the power consumption of a PLL must be sufficiently low. For example, in high-speed wireless interconnects, the preferred EVM is lower than −28 dB, and the power budget for one channel receiver is smaller than 100 mW. Consequently, many recent high-speed links limit the modulation scheme to 16/64-QAM [5], [6]. Given these requirements, designing a fully integrated and high-performance PLL has become one of the most urgent needs for enabling next-generation exa-scale links. As the quality factor (Q-factor) of CMOS inductors is limited to approximately 15 at mmW frequencies [7], a wide PLL loop bandwidth (f_{BW}) is preferred to attenuate more phase noise from a voltage-controlled oscillator (VCO). Unfortunately, the level of attenuation to reference spurs is degraded if simply raising the PLL loop bandwidth. A higher level of spur rejection reduces aliased energy and out-of-band emissions, improving the EVM [4]. Although recent sub-harmonically injection-locked PLLs [8], [9] and sub-sampling PLLs [10], [11] have achieved extremely low jitter with low power consumption compared to traditional charge pump PLLs (CP-PLLs), they typically generate higher levels of reference spur even when a high-frequency reference is used.

In an integer-N PLL, the optimal f_{BW} can be found by inspecting the intercept point of the PLL in-band and out-of-band phase noise profiles. Here, the PLL in-band phase noise is normally dominated by input reference noise or phase detector (PD) noise, whereas the out-of-band phase noise is dominated by VCO phase noise. As the VCO phase noise is poor due to the wide frequency tuning range (FTR) requirement and poor Q-factor of inductor coils, a wide f_{BW} is preferred, which in turn degrades ripple rejection. In light of this, this article proposes a novel PD that aims to break the trade-off between low-jitter performance and ripple rejection. Given ripple compensation phase detector (RCPD), the proposed PD achieves ripple compensation by introducing a pair of identical PDs in a push-pull fashion without doubling power consumption. These two PDs generate identical ripple current simultaneously. The result is the mutual compensation of ripple at the RCPD output without impeding the phase alignment process. A calibrator is

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introduced to enhance the matching between the two PDs, minimizing ripple over process variation. The RCPD can be further extended to a RC-phase/frequency detector (RC-PFD), which can also perform frequency detection and VCO lock detection. With this technique, an mmW PLL achieves state-of-the-art jitter and reference spur performance over a wide FTR.

The rest of this paper is organized as follows. Section II summarizes recent developments in mmW PLLs and their PDs, followed by the introduction of ripple compensation technique and its concept. Section III elaborates on the implementation of the RCPD and its extension to RC-PFD, as well as calibration. Section IV elaborates the design of mmW circuits and PLL. Measurement verifications and discussion are provided in Section V, and this article is concluded in Section VI.

II. Concept of Ripple Compensation

A. Recent CMOS MmW PLLs

Sub-sampling PLLs (SS-PLL) and sampling PLLs [10], [11], [12], [13], [14] were recently reported to fulfill low-power and low-jitter performance. In an SS-PLL, due to the high PD gain, the phase noise of the PD and CP is sufficiently suppressed. SS-PLLs are recognized for attaining the best figure-of-merit (FoM) among all PLL architectures. However, owing to the binary frequency-shift keying (BFSK) modulation effects, clock feedthrough, and charge injection, many SS-PLLs have a high reference spur level of around −50 dBc. Additionally, sub-sampling PDs have a limited acquisition range, necessitating a frequency-tracking loop (FTL). On the other hand, in a sampling PLL, the divider phase noise is amplified by N^2, where N represents the PLL divider ratio. Since the sampling PD acquisition range is increased by N, sampling PLLs are considered more robust than SS-PLLs. In fact, the divider chain phase noise can be confined to one flip-flop by employing a retimer at the divider chain output [14].

PLL in-band phase noise contributed by PD can be expressed by [10]

$$\mathcal{L}_{\text{in-band}} = S_{i.PD}/2K_{PD}^2 + \mathcal{L}_{\text{ref}}. \quad (1)$$

As the gain of a sampling PD (i.e., K_{PD}) is high, the PD intrinsic phase noise $S_{i,PD}$ is strongly attenuated. Therefore, $\mathcal{L}_{\text{in-band}}$ is instead governed by reference phase noise $\mathcal{L}_{\text{ref}}$, resulting in low-jitter performance. However, sampling PLLs suffer from clock feedthrough and charge injection, both stemming from the sample-and-hold operation.

Recent PDs for constructing low-power and low-jitter mmW PLLs have been reported. The MSSF (i.e., master-slave sampling filter) PD has a steep PD gain profile [13], which greatly attenuates the PD phase noise. However, MSSF necessitates a harmonic trap to attenuate the reference spur owing to charge injection and clock feedthrough. The reference spur was improved from −47 to −65 dBc, albeit with off-chip calibration required. In [15], a notch filter following the XOR-gate was reported. Featuring a multi-stage *RC* network and realizing that the ripple frequency at the XOR-gate PD output is $2f_{ref}$ (f_{ref} here denotes the reference clock frequency), the introduced notch filter dampened the ripple at $2f_{ref}$ by approximately 14 dB. As it inevitably introduced poles to the PLL, the level of ripple attenuation affects loop stability. Additionally, the K_{PD} of an XOR-gate is not high enough to sufficiently attenuate its phase noise. In [16], a current-reuse sampling PD was reported. The PD is featured in a push-pull complementary fashion, attempting to suppress the voltage ripple at the PD output by neutralizing the charge injection and clock feedthrough without the need for calibration like [13]. Likewise, the *RC* loop filter (LF) located at each latch output introduces poles to the loop, potentially reducing the loop phase margin as well as the PD acquisition range, thereby necessitating an extra FTL. The sampling PD reported in [17] has the advantages of simple realization and high K_{PD}. However, it also suffers from charge injection and clock feedthrough.

State-of-the-art research has also explored PFD/CP topologies for achieving low-jitter clocks. A mmW CP-PLL reports 54 fs_{rms} jitter with low reference spur [18], but it consumes 45 mW power as its PD gain is $I_{cp}/(2\pi)$, necessitating a large CP current I_{cp} to sufficiently dampen the CP phase noise. In [19], the CP incorporates feedback to enhance the matching at its output pull up/down network, attaining a reference spur of –61 dBc. Yet, a 2.28 GHz reference clock was used, and the loop bandwidth was approximately 600 kHz. A time-amplifying phase-frequency detector was reported in [20]. Similarly, the PFD attenuates its in-band phase noise with a large K_{PD}. However, periodic reference ripples were introduced due to mismatches between the current source and the load capacitors. With such a PFD, the PLL exhibits −47.55 dBc reference spur and 60 fs_{rms} at 25.8 GHz.

In summary, state-of-the-art mmW PLLs exhibit trade-offs among reference spur, jitter, acquisition range, and loop stability.

B. Ripple Generation in Single Switch PD

Since the concept of ripple compensation stems from the mixer PD, its analysis begins with an investigation into a single MOS switch in a traditional mixer PD featuring, as illustrated in Fig. 1(a). The NMOS M_1 serves as a sampler, sampling the voltage of the divider output. The sampled result is first dampened by resistor R_L and then stored at the capacitor C_{PD}. The subsequent transimpedance amplifier (TIA) converts the sampled voltage to a proportional current, modulating the VCO toward phase locking.

In a single mixer PD, the phase error ($\Delta\varphi$) is the amount of how much the phase difference between reference phase and divider output phase deviates from $\pi/2$. With a larger phase error, the mixer PD has a longer time (ΔT) to inject (or absorb) charge to its output capacitor, translating to a proportional near-DC voltage by $\Delta V_{PD} = \frac{1}{C_{PD}} \int_{-\infty}^{\Delta T} i_{PD} dt$, where C_{PD} is the PD output capacitor. The following TIA converts ΔV_{PD} to current by $I_{OUT} = \text{G}_\text{m} \Delta V_{PD}$, where G_m is the transconductance gain. From this aspect, the mixer PD is inherently a linear PD, where the TIA output current amplitude is proportional to $\Delta\varphi$.

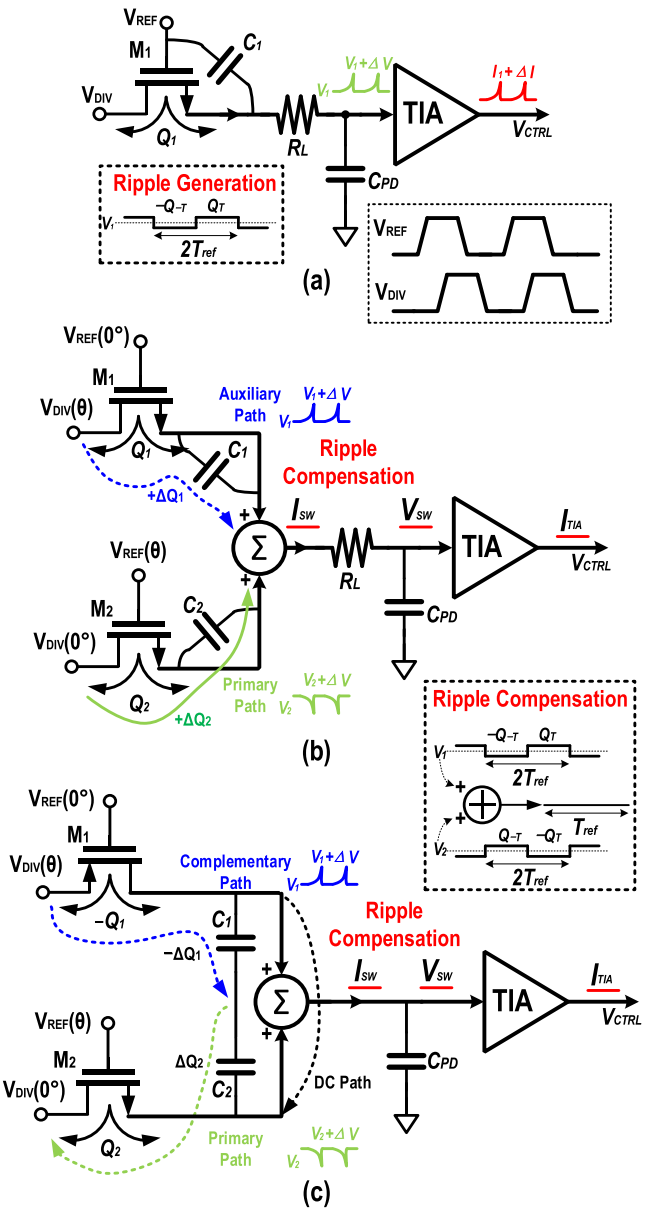

Fig. 1. Concept of ripple compensation: (a) illustration of ripple generation by single switch in a mixer PD [21], followed by a TIA, (b) ripple compensation evolved from (a), and (c) enhanced version for ripple compensation.

If both input signals (i.e., V_{ref} and V_{div}) are square pulses, the frequency term appearing at M_1 output is estimated as follows:

$$\begin{aligned} y_1(t) &= a_1 \sum_{k=1}^{\infty} \frac{\cos\left[(2k-1)\,\omega_{ref} t\right]}{2k-1} \\ &\quad \times a_2 \sum_{k=1}^{\infty} \frac{\sin\left[(2k-1)\,\omega_{div} t\right]}{2k-1} \\ &= V_0 + V_1 \sin\left(\omega_{ref} t\right) + V_2 \sin\left(\left(\omega_{ref} + \omega_{div}\right) t\right) + \ldots, \end{aligned} \tag{2}$$

where ω_{ref} and ω_{div} denote the reference frequency and divider output frequency in radians, respectively, and $\omega_{ref} \approx \omega_{div}$ in the locked state. Clearly, the frequency components include a near-DC term, the fundamental term, and higher harmonic terms. In (2), the near-DC term V_0 is generated by $\omega_{ref} - \omega_{div}$, whereas the fundamental term ω_{ref} stems mainly from $2\omega_{ref} - \omega_{div}$ and $\omega_{ref} - 2\omega_{div}$. Higher harmonic terms are suppressed by the output load R_L and C_{PD}. As such, the ω_{ref} term dominates the reference spur. During phase alignment, V_{ctrl} is modulated by V_0 until the net current of TIA is nulled.

Other non-idealities raise the reference spur level. Specifically, the transition of the reference clock couples to the switch output through parasitic C_1, exhibiting clock feedthrough. Moreover, charge injection occurs upon the ON/OFF switching by an instantaneous charge Q_1, a non-ideality commonly observed in traditional CP. When M_1 turns on, it absorbs this charge ΔQ, and when it turns off, it dispels this charge through its drain and source nodes. Fortunately, the BFSK effect is negligible here since there is no direct path from the switch to the VCO load. Therefore, clock feedthrough and charge injection both enhance the reference spur for such a PD.

C. Concept of Ripple Compensation

In light of the above investigation, the ripple compensation technique is introduced to reduce reference spur. As conceptualized in Fig. 1(b), an auxiliary path is dedicatedly added to join the primary path for phase detection. To perform ripple compensation, the charge injected by the main path must be well compensated by that of the auxiliary path within the same period, leading to $\Delta V_{PD} = \frac{1}{C_{PD}} \int_0^{T_{ref}} (i_{PD.m} - i_{PD.aux}) dt = 0$, where $i_{PD.m}$ (main path current) is cancelled out by $i_{PD.aux}$ (auxiliary path current). The current summer ensures the above current cancellation. In conventional PLL exploiting mixer PD, $i_{PD.m}$ cannot be cancelled. A loop filter is necessary to attenuate $i_{PD.m}$, reducing the reference spur. Doing so, however, a tradeoff is created between the level of attenuation and the PD acquisition range. With a higher level of attenuation to $i_{PD.m}$, the PD acquisition range is reduced, potentially resulting in false lock. Yet, owing to ripple compensation, the level of attenuation to $i_{PD.m}$ does not rely on the filter corner frequency, but instead the matching between $i_{PD.m}$ and $i_{PD.aux}$.

A phase difference θ at the PD input is required to ensure the above ripple compensation. By realizing that a single switch mimics a sampling mixer and recalling from the harmonic rejection mixer, which cancels out the images through a quadrature configuration, $\theta = 90°$ is examined for ripple compensation. The switch output voltage can now be expressed as follows:

$$\begin{aligned} y_2(t) &= a_1 \sum_{k=1}^{\infty} \frac{\cos\left[(2k-1)\,\omega_{ref} t\right]}{2k-1} \\ &\quad \times a_2 \sum_{k=1}^{\infty} \frac{\sin\left[(2k-1)\,\omega_{div} t\right]}{2k-1} \\ &\quad - a_3 \sum_{k=1}^{\infty} \frac{\sin\left[(2k-1)\,\omega_{ref} t\right]}{2k-1} \\ &\quad \times a_4 \sum_{k=1}^{\infty} \frac{\cos\left[(2k-1)\,\omega_{div} t\right]}{2k-1} \end{aligned}$$

$$= V_0 + V_1 \sin\left(\left(\omega_{ref} + \omega_{div}\right) t\right) - V_2 \sin\left(\left(\omega_{div} + \omega_{ref}\right) t\right) + \bullet\bullet, \quad (3)$$

clearly, y_2 contains only a near-DC term without any disturbance by harmonic terms only if $a_1 \times a_2 = a_3 \times a_4$. Operating akin to the harmonic rejection mixer, ripple compensation can be realized by duplicating a sampling PD and combining both PDs to perform phase detection, both driven by quadrature input phase.

The above ripple compensation, however, suffers from several shortcomings. Since one more PD is involved, both power consumption and noise are doubled. Furthermore, charge injection and clock feedthrough are enhanced instead of being neutralized, as illustrated in Fig. 1(b). For these reasons, the above configuration is evolved to Fig. 1(c), where the switch M_1 is replaced by its complementary version. Likewise, all harmonics generated by both PDs are mutually compensated when they are fully matched. Nonetheless, clock feedthrough can be compensated when $C_1/C_{PD} = C_2/C_{PD}$, whereas charge injection is nulled when $|\Delta Q_1 - \Delta Q_2|/C_{PD} = 0$. In principle, these two conditions are identical to those in a conventional current steering CP. In sampling PD [13] or double sampling PD [14], however, clock feedthrough and charge injection cannot be neutralized but instead being filtered, rendering the level of ripple rejection to be coupled with PD noise and loop stability.

On the other hand, in Fig. 1(b), if the primary PD is realized by a mixer PD or an XOR-gate PD, like the designs in [15] and [21], respectively, resistor R_L is still required since each PD has to draw current from the power supply. In Fig. 1(c), however, the current drawn by PMOS M_1 can be reused directly by its complementary transistor M_2, halving the power consumption and omitting the need for a resistor.

D. Ripple Frequency Boosting Effect

Ripple compensation performed by the above topologies relies on the fact that both paths are fully matched, which is difficult considering process, voltage, and temperature (PVT) variations. That is, Fig. 1(c) inherently suffers from poorer mismatches compared with the architecture in Fig. 1(b). As indicated in (3), when mismatches occur, such that $V_1 \neq V_2$, the $2f_{ref}$ harmonic term appears and dominates the reference spur. This characteristic is particularly helpful for wide f_{BW} PLLs since the ripple amplitude undergoes a higher level of attenuation by the LF due to its inherent frequency boosting. As will be shown in the next section, the ripple frequency would further rise up to $4f_{ref}$ for a differential topology. From this aspect, the ripple compensation technique still holds the advantage of suppressing the reference spur when mismatches occur.

In [22], the spur-frequency multiplying technique enables the spur frequency to be multiplied from f_{ref} to more than $10f_{ref}$, where a VTC (i.e., voltage-to-time converter) and a TVC (i.e., time-to-voltage converter) are necessitated to serve the above purpose. As no narrow pulse is generated, spur-frequency boosting by ripple compensation consumes less power when a high-frequency reference (i.e., $f_{ref} > 250$ MHz) is used. The spur frequency, boosted by RCPD, is 2X than that of the double sampling PD [14], without the need for a duty cycle corrector. In addition, with a high PD gain, the RCPD phase noise become smaller than the reference phase noise, achieving the same goal as the double sampling PD in terms of PD noise contribution.

III. Circuit Implementation of RCPD and RC-PFD

A. RCPD

As RCPD can be evolved from a sampling mixer, Fig. 2(a) and (b) depict the realization of two versions of the sampling mixer. Here, PMOS P1–P4 serves as the sampler, whereas PMOS P5–P8 form the current summer. The tail current source M_{PR} injects static current into the current summer. R_L and C_{PD} constitute the output load. R_L not only defines the voltage gain but also attenuates unwanted harmonics. Same principle applies to Fig. 2(b), which is an all-NMOS version. As the voltage gain is associated with the ripple amplitude, a lower frequency corner at the output is preferred for higher attenuation of the ripple, which, however, sacrifices the PD acquisition range as well as the PLL phase margin [23]. Considering the fact that the phase comparison is conducted twice in one reference cycle due to the differential topology, the $2f_{ref}$ harmonic dominates the reference spur. Using a differential Gilbert-cell mixer PD, an mmW PLL generated a -34 dB reference spur even when $f_{ref}/f_{BW} > 20$ [21]. The high level of reference spur is due to the fact that the excessive charge accumulated through phase comparison in $0.25T_{ref}$ is supposed to be compensated in the next quarter cycle, periodically perturbing the V_{ctrl}. This operating mechanism is inherently akin to an XOR-gate PD analyzed in [13].

The above sampling mixer PD has evolved into the RCPD, as illustrated in Fig. 2(c) and (d), by duplicating the sampling mixer PD and joining them in the current domain. Ripple compensation is performed such that whenever a ripple appears at the output node V_0, where $V_0 = V_{0.dc} + \Delta V$, a ripple with the same amplitude and phase disturbs $\bar{V}_0$ as well, allowing $\bar{V}_0 = \overline{V_{0,dc}} + \Delta V$. This corresponds to the topology of Fig. 1(b). The resulting TIA output current is $I_{TIA} = G_m \times (V_0 - \bar{V}_0) = G_m \times (V_{0.dc} - \overline{V_{0,dc}})$, which is free of any ripple. However, as discussed in Section II-C, charge injection and clock feedthrough are both enhanced instead of being neutralized, dominating the reference spur. Furthermore, the power consumption is doubled.

Considering these shortcomings, the RCPD is therefore evolved into a complementary fashion, as illustrated in Fig. 3, which is the circuit implementation of Fig. 1(c). Here, NMOS N1–N8 constitute the primary PD, whereas PMOS P1–P8 establish the complementary PD, which is "folded" to the primary PD. With this configuration, the current drained by the primary PD must be fed by the complementary PD, halving the power consumption. Due to current reuse, resistor R_L has been omitted. Similar to conventional CP, clock feedthrough and charge injection through P5–P8 can be mutually neutralized by their complementary counterparts N5–N8. The static current for both PDs is defined by their respective tail current sources, M_{NR} and M_{PR}. Here, M_{NR} is fixed, but M_{PR} is configurable to allow for mismatch calibration, as elaborated in Section III-B. Fig. 4 visualizes the operating principle of the RCPD. During

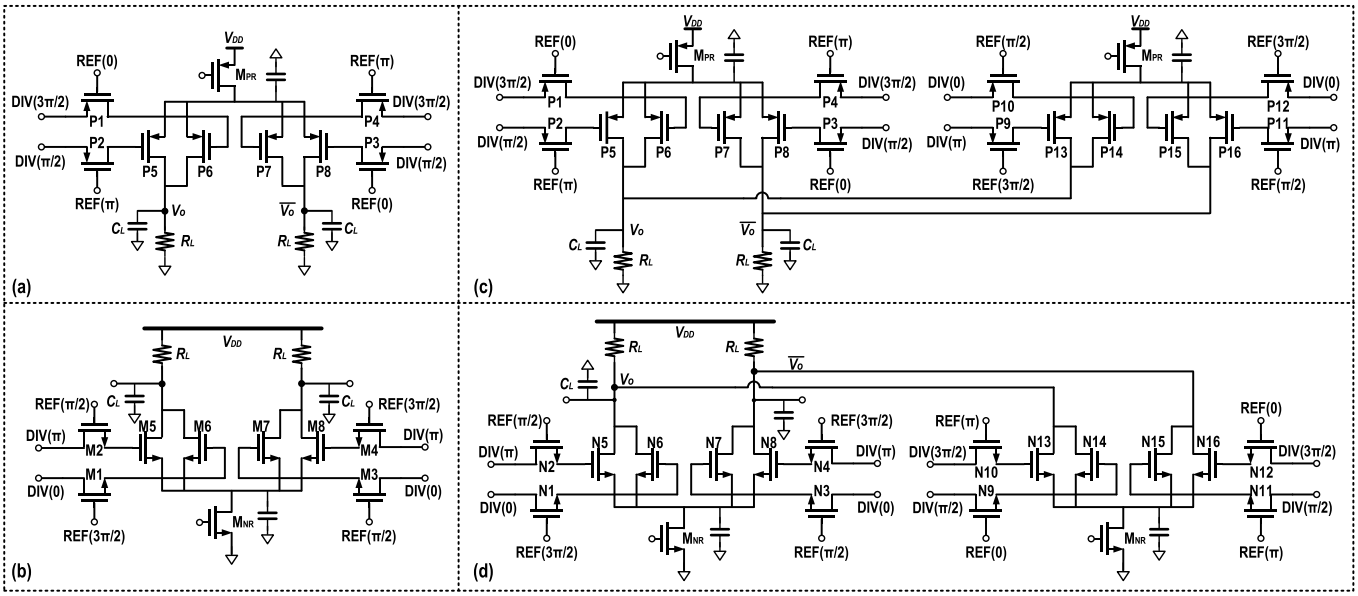

Fig. 2. (a) and (b) Sampling mixer PD in which the current summer is realized by P-type and N-type MOSFET, respectively, (c) and (d) circuit implementation of RCPD evolved from (a) and (b), respectively.

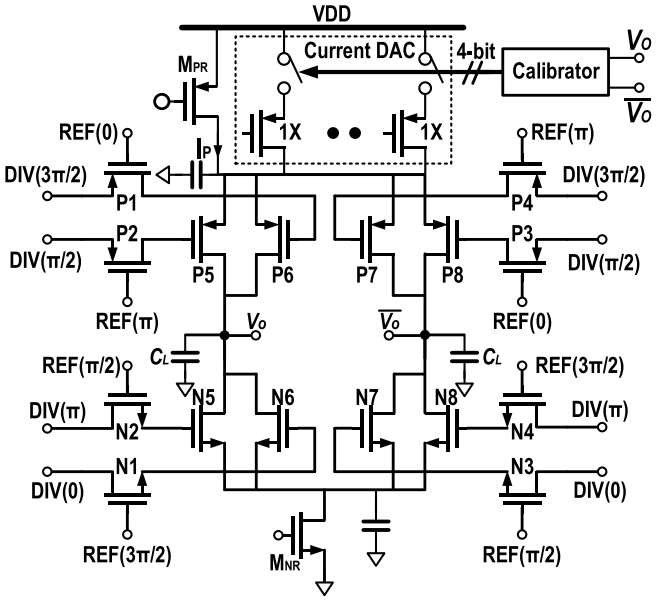

Fig. 3. Circuit implementation of the proposed RCPD.

phase alignment, the TIA net output current denotes the polarity of $V_0 - \bar{V_0}$. For instance, considering the case where the reference clock lags, the net current $(I_{N6} - I_{P6})$ –$(I_{N5} - I_{P5})$ is negative, increasing the V_{ctrl} as well as the VCO frequency f_{vco}. Likewise, when the reference clock leads, V_{ctrl} is decreased, as is the VCO frequency. In the equilibrium state, the net current remains nulled thanks to ripple compensation. From this aspect, ripple compensation does not impede phase alignment, whereas it can neutralize the ripple current at all times. Note that when more than one pair of sampling PDs participate in ripple compensation, the above conclusion still holds. The penalty is that more input phases are required, complicating the PLL input design.

Figs. 5(a), (b), and (c) provide the simulated PLL reference spur associated with the duty cycle distortion (DCD) of the reference clock, the current mismatch between the primary and the complementary PD, and the transistor width ratio between the primary and the complementary PD, respectively. In this simulation, $f_{vco} = 38.4$ GHz, $f_{ref} = 0.3$ GHz, and $f_{BW} \approx 10$ MHz. The reference buffers, proposed RCPD and TIA are designed with transistor models, while other PLL blocks use Verilog-A models, to reduce the required transient simulation time. Then, DFT analysis is performed to evaluate the PLL reference spur. As observed, the PLL reference spur at $2f_{ref}$ and $4f_{ref}$ is substantially degraded due to DCD, current, and size mismatches. An optimal transistor width ratio is found at approximately 1.55, and the optimal current for M_{PR} is found through manual tuning. The reference spur at $2f_{ref}$ becomes prevalent at a large mismatch, simply owing to the diminishing of ripple compensation. Under such circumstances, it is hard to distinguish whether the ripple compensation technique attempts to eliminate or enhance the $2f_{ref}$ term or both.

By regrouping (3), the PLL reference spur is degraded by I/Q phase error θ_{err} as indicated as follows.

$$\text{Spur}_{\text{PLL}} \approx 20\log\left[\frac{K_{VCO}\frac{H_{TIA}}{4f_{ref}/f_{c.TIA}}\frac{V_4}{4f_{ref}/f_{c.LF}}}{2\sqrt{2}\pi \times f_{ref}}\theta_{err}\right], \quad (4)$$

where H_{TIA} is the TIA conversion gain, $f_{c.TIA}$ is TIA corner frequency, $f_{c.LF}$ denotes the corner frequency of the loop filter, V_4 represents the ripple amplitude. The term $4f_{\text{ref}}$ denotes the reference spur frequency at 4 times of f_{ref}, due to ripple compensation and its frequency boosting effect. The simulated result in Fig. 6 approximately matches the above analysis. In general, θ_{err} can be well controlled to within 0.6° and 0.14° for polyphase shifter and static divider (Section IV), respectively.

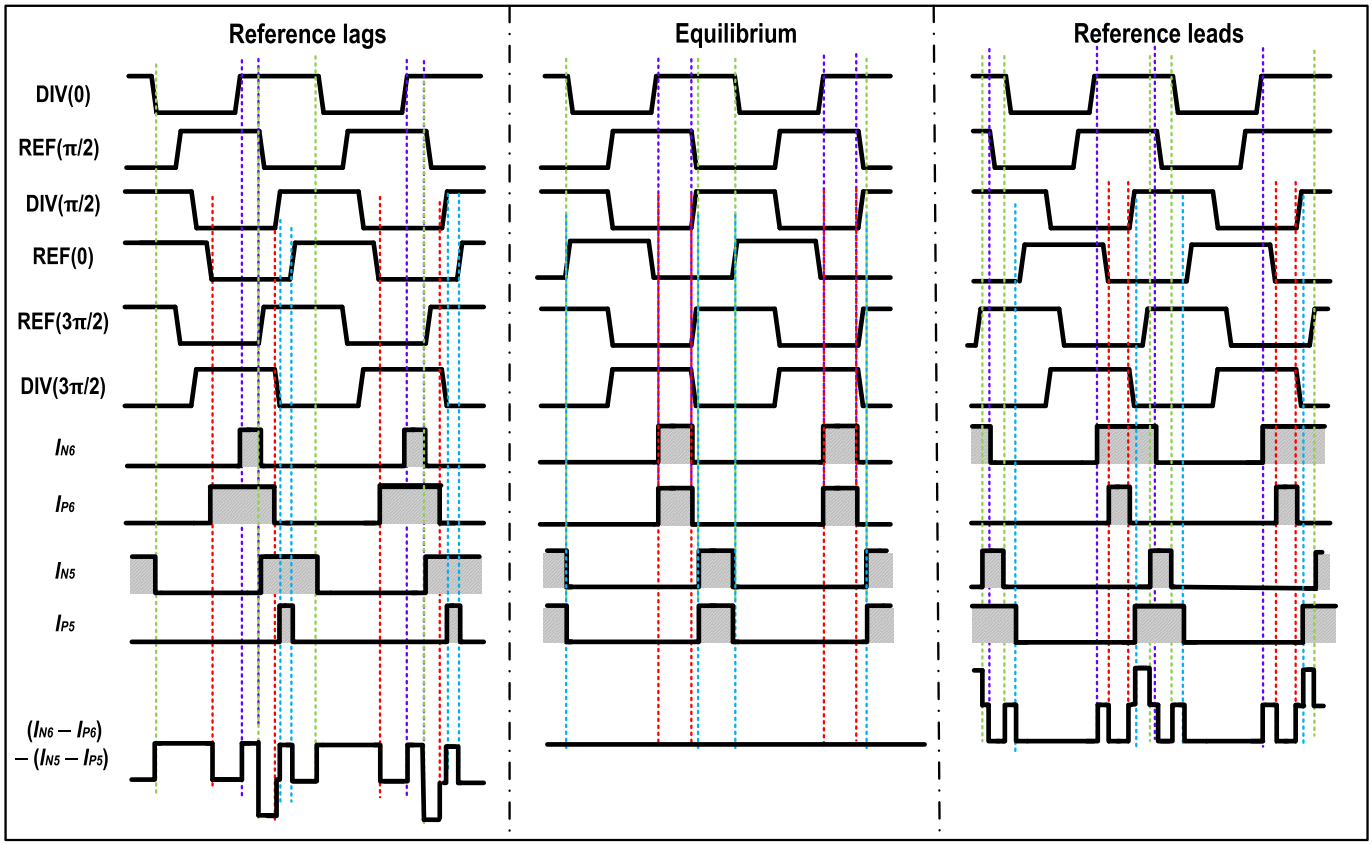

Fig. 4. Timing diagram for the proposed RCPD as well as ripple compensation at the equilibrium state.

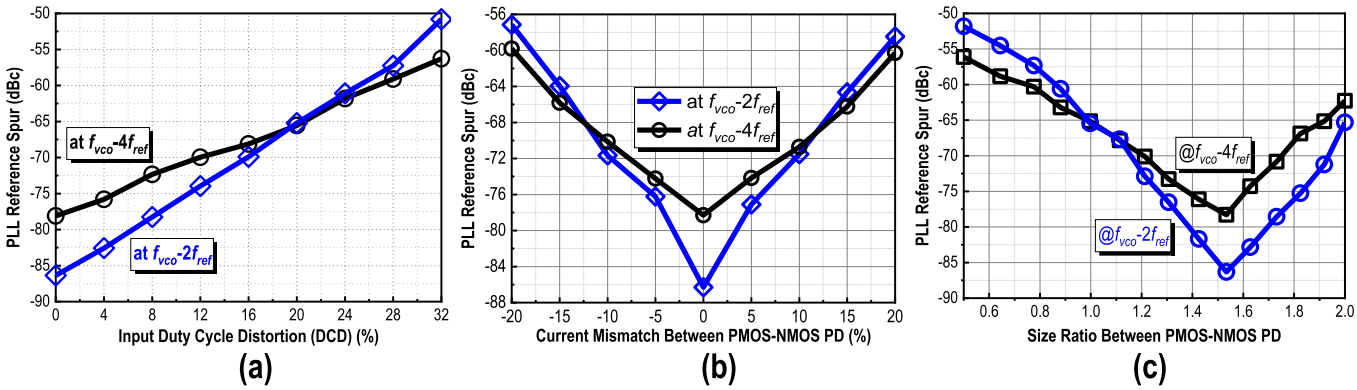

Fig. 5. Simulated PLL reference spur against (a) duty cycle distortion (DCD) of the input reference clock, (b) current mismatch between the primary and the complementary PD, and (c) transistor width ratio between the primary and the complementary PD.

From all the above aspects, mismatch calibration is mandatory.

B. Calibrator for Ripple Compensation

As the sources of generating ripple for RCPD are rich, it is difficult to minimize ripple by respectively extracting and dealing with each source. Consequently, calibration is performed by lumping all the possible nonidealities and tuning only one circuit parameter until an optimal operating point is found, which is supposed to minimize the overall nonideal effects. In fact, the PLL reference spur mainly steams from the perturbation voltage V_{PD} at the PD output, as evaluated as follows.

$$\mathrm{Spur}_{\mathrm{PLL}} \approx 20\log\left[\frac{\frac{N\times\omega_{BW}\times H_{TIA}}{\sqrt{1+(4\omega_{ref}\times R_{LF}C_{LF})^2}}V_{PD}}{2K_{PD}\times 4\omega_{ref}}\right], \quad (5)$$

Here, $R_{LF}C_{LF}$ is a first-order low-pass filter (LPF) in the LF, whose corner frequency must be at least tenfold of f_{ref}, so as not to lower the PLL loop stability. K_{PD} should be large enough for dampening the PLL in-band phase noise, but it cannot be arbitrarily large considering the LF size. Therefore, the remaining choice is to reduce V_{PD}, which highly relies on the matching as illustrated in Fig. 5. As such, the tail current of the complementary PD I_{MPR} is tuned for calibration in this

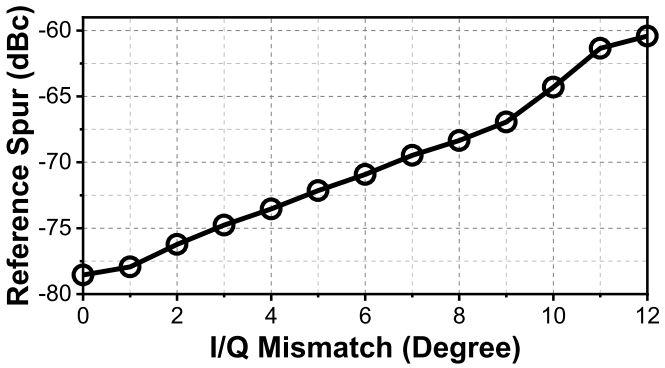

Fig. 6. Simulated PLL reference spur degraded by input I/Q mismatch.

work. The effectiveness of tuning I_{MPR} for ripple calibration can be clearly observed from Fig. 5(b).

The calibrator is therefore proposed as illustrated in Fig. 7. It is composed of two paths, namely sweeping path and decision path. Clocked by the reference signal, the sweeping path includes a thermometer code converter. The decision path contains the RCPD, an envelope detector (ED), a quantizer, and a register array. The ED firstly amplifies the small signal of the RCPD output, then generates an output DC voltage whose amplitude corresponds to the power level of the RCPD output. The subsequent quantizer converts the above DC voltage to digital code, stored by the following register array.

Fig. 8 provides an example illustrating the process of calibration. At the beginning, the thermometer code starts with the lowest state, which is <0000>, indicating the smallest current of I_{MPR}. Signal C_{Dec} is asserted, initializing the calibration by refreshing all the registers. At such a state, the decision path performs the phase detection and generates ripple at the RCPD output. A time interval T_{Cal} is allocated for the decision path to record the current level of ripple. T_{Cal}, which is specified by a programable divider inside the thermometer code converter, should be at least 10 times greater than $1/f_{BW}$, to allow sufficiently long time for phase alignment. After the PLL is settled, the quantizer's digital output code represents the voltage level of the ripple. Then, the thermometer code rises to <0001>, and the calibrator goes through the above process again, until the state <1111> is completed, which corresponds to the maximum current allowed by I_{MPR}. Eventually, C_{Dec} returns to zero, and the register array ultimately chooses the minimum digital output code of the quantifier found during the sweeping history, finalizing the calibration and lock the state.

The effectiveness of the above calibration has been verified in Section V-B. Noted that, other sources of reference spur generation, such as the mismatches of TIA, can be possibly calibrated by the introduced approach.

C. RC-PFD

As the RCPD evolved from a sampling mixer PD, it may suffer from a finite acquisition range [23], rendering an FTL necessary. Moreover, VCO lock detection is preferred considering a wide FTR of a mmW PLL. With these in mind, the RCPD has evolved into the RC-PFD, as shown in Fig. 8, which consists of a frequency detector (FD) and a lock detector (LD). The FD is composed of a pair of RCPDs and a pair of hysteresis buffers, followed by a DFF and a CP (i.e., CP2). By revising (3) and allowing $f_{ref} \neq f_{div}$, the RCPD output would contain a beating signal with a frequency of $f_{bt} = |f_{ref} - f_{div}|$, with harmonic terms of f_{bt}. To enable frequency detection, only f_{bt} is needed. As such, the hysteresis buffer is a high-gain yet narrow-band amplifier. Operating like the bang-bang FD, whether the divider output is lagging or leading can be determined by allowing one RCPD (i.e., V_2) to sample the other (i.e., V_1), and the sampled result (i.e., V_Q) drives the CP2 to either inject or sink the current to the capacitor in the LF. The current of CP2 is ∼3X than that of the TIA output current to ensure dominating at the beginning of phase alignment.

The operation of LD is based on FD. At the beginning, the VCO band register is initialized to the lowest band, corresponding to operation at the lowest frequency. According to V_Q, if f_{ref} is still higher, the VCO band register would jump to a higher band upon receiving the falling edge of V_2 two times. This process continues until the f_{ref} is lower than the f_{div}. Then, a counter continuously samples V_2. In the case that the counter overflows, indicating that f_{bt} is small enough, the band register is locked by the counter, and the CP2 starts to conduct current to the LF. Otherwise, the above flow is restarted since an error may have occurred. The estimated lock detection time T_{LD} for the Mth VCO band is provided as follows, which is decoupled from the PLL loop dynamics. T_{ct} denotes the time required for the counter to overflow.

$$T_{LD} \approx \sum_{i=1}^{k\leq M} \left(\frac{1}{|f_{bt}|}\right) + T_{ct}\Bigg|_{\substack{f_{ref} - \frac{f_{VCO,k-1}}{N} > 0 \\ f_{ref} - \frac{f_{VCO,k}}{N} < 0}}, \quad (6)$$

According to simulation, the RCPD can sweep all possible values of V_{ctrl} when the PLL is locked without support from the FD. This observation may indicate a sufficiently large acquisition range for the RCPD, suggesting that the FTL is not necessary. However, FTL is still implemented in this work to account for potential locking failures. In fact, since CP2 is clocked by V_2, it remains off when locked. Accurate extraction of the acquisition range for RCPD requires further investigation in future work.

IV. MmW Circuits and PLL

A. VCO and Dividers

A wide FTR is preferred in the design of mmW PLLs to cover various applications, necessitating a wideband VCO. A mmW Class-C VCO is illustrated in Fig. 10(a), where coarse tuning is achieved using 3-bit capacitor banks. An error amplifier drives the PMOS P1 to provide a regulated voltage of approximately 0.9 V, supplying the VCO with current I_P. The simulated power supply rejection ratio (PSRR) is 52 dB. This configuration not only reduces VCO frequency pushing but also decouples it from noise due to wire-bonding. Since the VCO tank quality factor deteriorates when more capacitor banks are switched on, a current DAC is employed to compensate for this loss depending on the VCO band register.

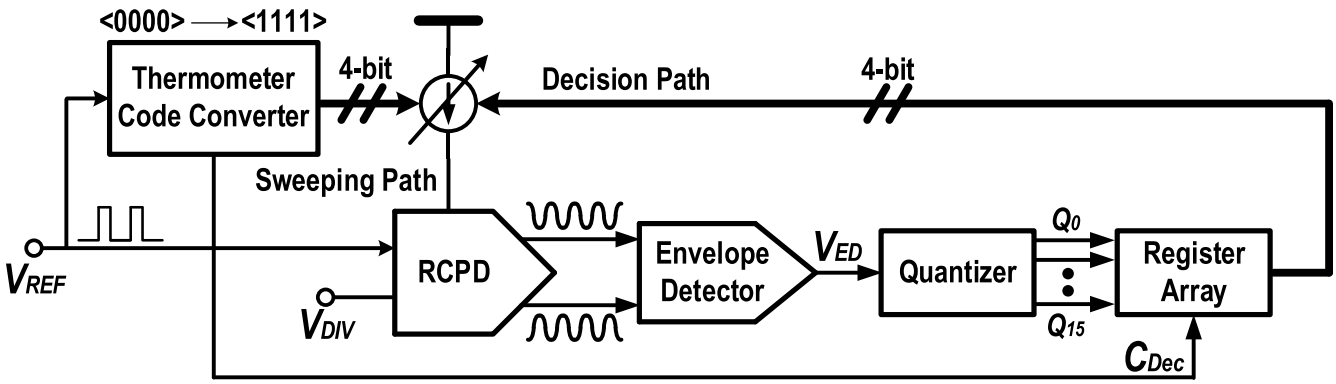

Fig. 7. Calibrator for ripple compensation.

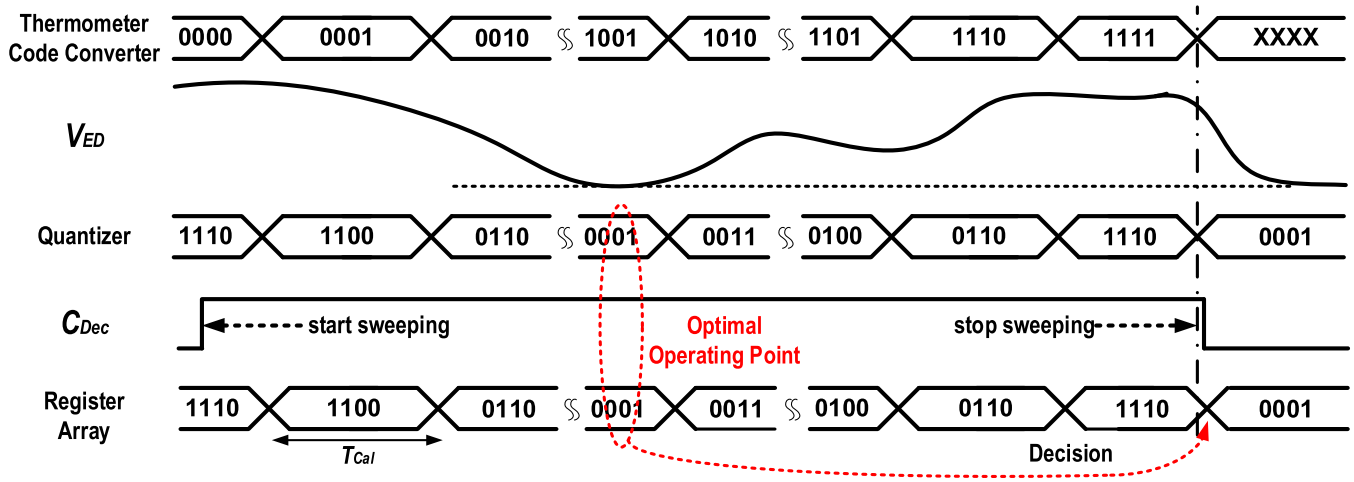

Fig. 8. Exemplified timing diagram for RCPD calibration.

This also ensures that the VCO output swing is large enough to drive the prescaler at all operating frequencies, albeit with slightly higher power consumption. Due to the channel-length modulation effect of the core transistors *N1* and *N2*, their drain current I_{vco} varies during oscillation. To relax this effect, another current DAC M_{N1} and its dummy compensates for the variation by allowing $|\partial(I_v - I_{vco})/\partial V_{DDL}| = |\partial I_v/\partial V_{DDL}|$. With proper sizing, the power penalty of M_N is constrained to no more than 27%. The result is an ~3.2 dB reduction to the VCO phase noise in the presence of power supply noise. More capacitor banks may widen the FTR, but the VCO suffers from potential oscillation failure under PVT variation. Considering possible gate leakage through the varactor, which would raise the reference spur, the varactors are realized using 1.8 V thick-oxide accumulation-mode MOS transistors.

With a large input from the VCO, the prescaler can be realized using an injection-lock frequency divider (ILFD), Miller divider, or static divider. ILFD is preferred for high-frequency and low-power scenarios, but its locking range is narrow. The static divider can lock over a wide band but consumes high power and occupies a large area at mmW frequencies. The Miller divider performs in between. Fig. 10(b) depicts the Miller divider. Here, $M_{5,6}$ serves as the regeneration pair, while the output voltage feeds back to the diode-connected pair $M_{3,4}$. The Miller divider fails to divide the input frequency

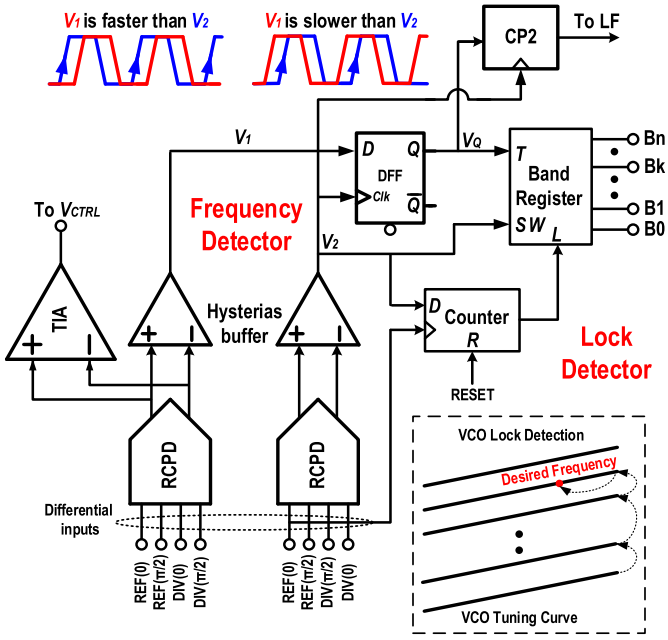

Fig. 9. RC-PFD evolved from RCPD.

(i.e., f_{vco}) at high frequencies since its open-loop gain drops below unity, and at low frequencies as the third harmonic

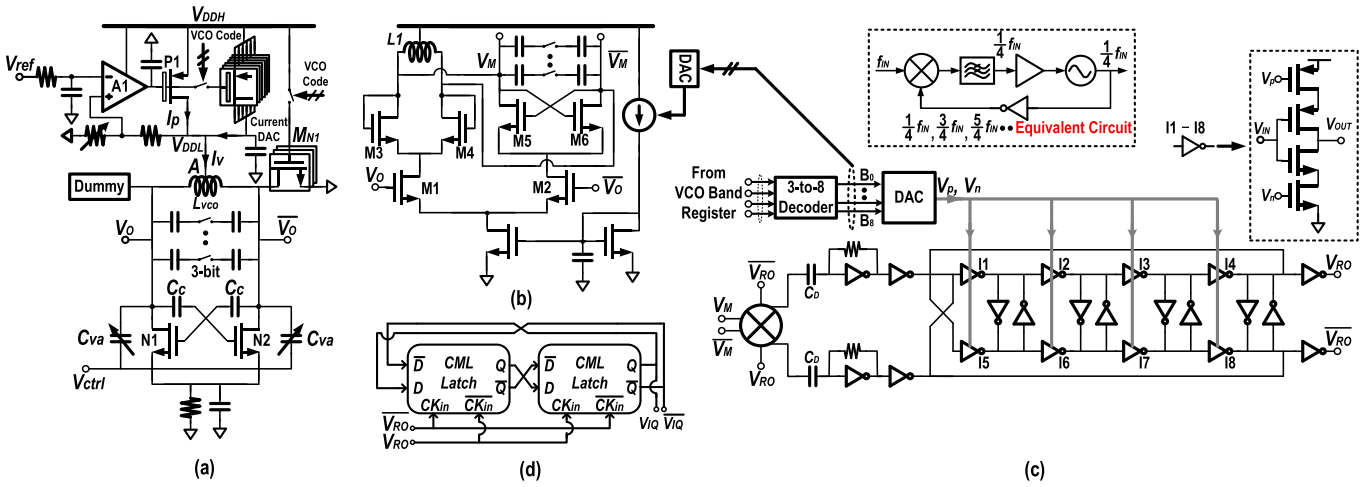

Fig. 10. MmW PLL building blocks includes (a) VCO (bias circuit not shown), (b) configurable Miller divider, (c) configurable ring-based ILFD, and (d) static divider generating I/Q signal for the RCPD performing ripple compensation.

(i.e., $3f_{vco}/2$) is not sufficiently suppressed. Consequently, capacitive banks are employed to govern the center frequency of the Miller divider, extending its locking range.

A low-power ring-based ILFD serves as the subsequent divide-by-4 frequency divider, as shown in Fig. 10(c). The input signal with a frequency of f_M mixes with the ILFD output, which contains a rich set of odd harmonics of $(1/4)f_M$, where f_M is the Millr divider output frequency. The result is the mixing between f_M and $(3/4)f_M$, generating the $(1/4)f_M$ signal and locking the ring VCO. Other mixed frequencies are far outside the ring VCO locking range. Likewise, the natural oscillation frequency of the ring VCO is determined by the delay of each inverter, and a DAC realized by an array of resistors manipulates the current flowing through each inverter, extending the locking range. According to simulation, such a ring-based ILFD consumes at least twice as much power as the Miller divider if deployed as the prescaler under PVT variation, since the magnitude of the $(3/4)f_M$ tone is greatly attenuated at higher frequencies.

The low-frequency dividers are realized using a static divider, as shown in Fig. 10(d), with their power consumption and area scaling down across each stage. It can also easily generate the I/Q signals. Monte Carlo statistics reveal that the I/Q mismatch is approximately 0.14°. At the end of the divider chain, a pair of DFFs sampled by a high-frequency clock reset the divider output phase, attenuating the divider chain phase noise as discussed in [12].

B. MmW PLL Architecture and Loop Dynamics

Fig. 11 sketches the mmW PLL block diagram. It contains a reference I/Q generator, the proposed RC-PFD with embedded FD and LD, an LF, a VCO, and a divider chain. The reference I/Q generator is composed of a hybrid *RC* network, $R_{s1,2}$ and $C_{s1,2}$. The resistors $R_{s1,2}$, with dummy resistors surrounding them, are made large enough to reduce their process variation. Yet, I/Q mismatch still exists. A calibrator realized by a phase detection loop may serve to minimize I/Q mismatch, but it inevitably introduces multiple noise sources to the PLL loop. In this work, a duty-cycle corrector (DCC) circuit featuring a cross-coupled inverter configuration reduces the I/Q mismatch to approximately 0.6°, as indicated by Monte Carlo simulation, at the cost of an extra 1.3 mW power consumption. According to Fig. 6, such an I/Q mismatch poses negligible impact on the PLL reference spur.

Another benefit of the RCPD is the elimination of a voltage level shifter and its associated noise if various supply voltages are utilized. In this work, the TIA and the VCO are supplied by a 1.8 V power supply, while other building blocks use 0.9 V. This is because, instead of generating continuous narrow pulses like conventional PFD/CP [18], the RCPD generates a near-DC output voltage whose amplitude is proportional to the phase error, similar to a mixer PD. As such, the TIA does not require a level shifter; it generates a proportional current to the LF based on its input voltage. However, a level shifter is necessary in conventional CP-PLL designs like the one in [24], which may fail to generate narrow pulses for $f_{ref} > 250$ MHz, as is the case here.

PLL open-loop gain (G_{open}) is expressed by (7):

$$G_{open} \approx \frac{K_{PD} \times H_{TIA}}{1 + j\frac{\omega}{\omega_{RCPD}}} \times \frac{1}{R_{lf}C_{lf}} \frac{(j\omega + \omega_Z)}{j\omega C_p\left(j\omega + \omega_p\right)} \times \frac{K_V}{N \times j\omega}, \tag{7}$$

where ω_p is a pole created at the RCPD. $\omega_p = 1/[R_1(C_1||C_2)]$, and $\omega_Z = 1/(R_1C_1)$. The channel length modulation effect of the TIA has been neglected. The phase margin associated with ω_{RCPD} can be evaluated as follows:

$$\phi_{PM} = \arctan(\frac{\omega_{UGB}}{\omega_Z}) - \arctan(\frac{\omega_{UGB}}{\omega_{RCPD}}) - \arctan(\frac{\omega_{UGB}}{\omega_p}), \tag{8}$$

Here, the unit-gain bandwidth is represented by ω_{UGB}. Allowing $\partial\phi_{Pm}/\partial\omega_{UGB}$ to be zero and recognizing that $\omega_{CMPD} \gg \omega_Z$ and $C_{p2} \ll C_{p1}$, the optimal unit-gain bandwidth is approximated as $\sqrt{\omega_{RCPD}\omega_z}$. With $C_{PD} = 3$ pF, the calculated G_{open} exhibits seven poles evaluated at 38.56 GHz, at the origin, 1.91×10^9, 1.86×10^9, 1.96×10^8, 6.54×10^7,

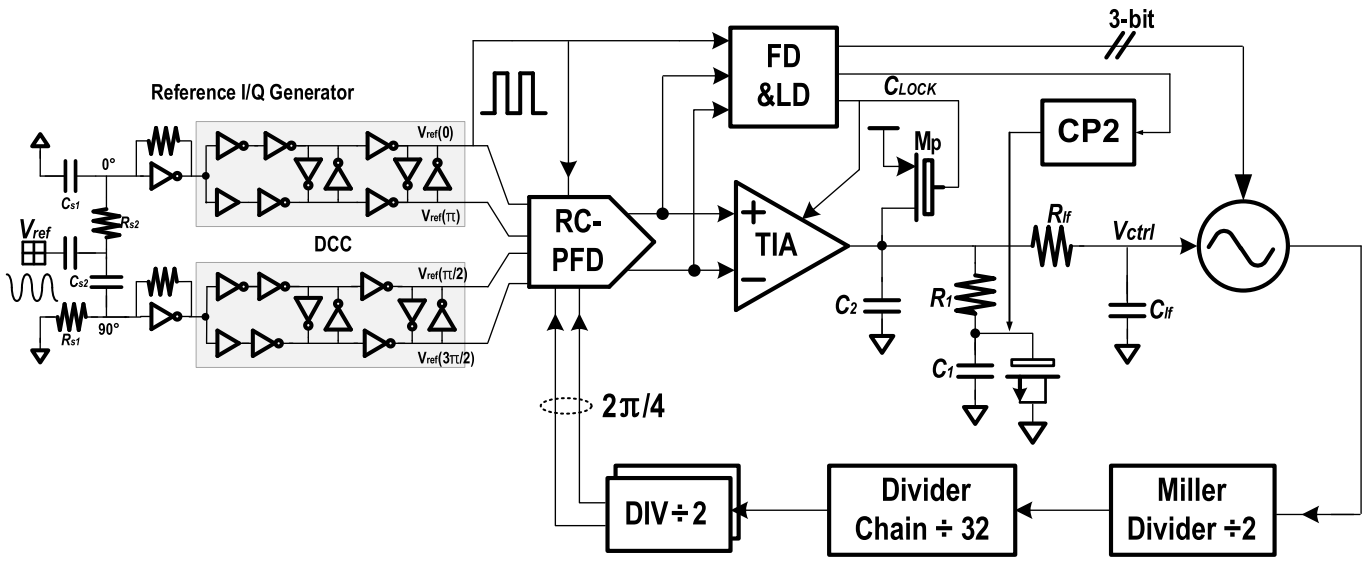

Fig. 11. Proposed CMOS mmW PLL exploiting RC-PFD.

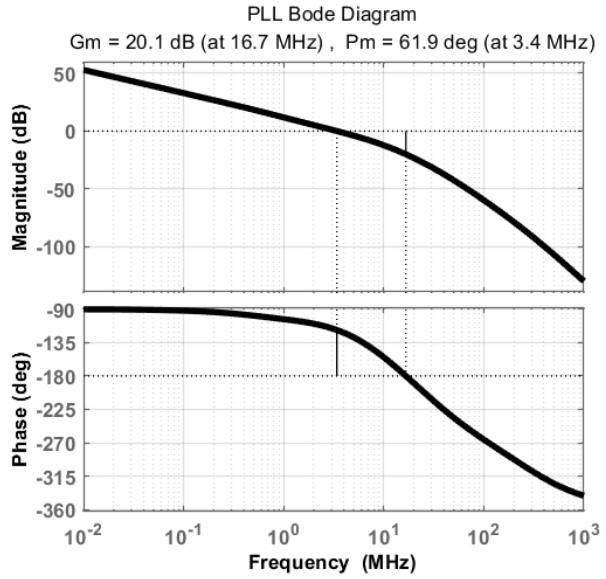

Fig. 12. Calculated Bode diagram of the mmW PLL.

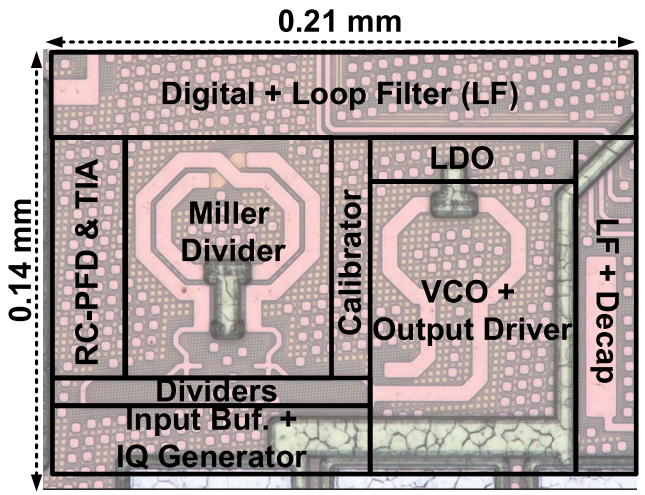

Fig. 13. Die photo of the CMOS mmW PLL.

1.75×10^7, and 5.35×10^6 Hz, in which the poles at 1.91×10^9 and 1.75×10^7 Hz are neutralized by two respective zeros. One zero located at 6.61×10^6 Hz remains in between the two dominant poles. The above distribution leads to an f_{BW} of approximately 3.4 MHz and a $\emptyset_{PM}$ of 61.9°. Fig. 12 visualizes the calculated Bode diagram of G_{open}.

V. Experimental Verifications

The proposed mmW PLL was implemented in a 22 nm bulk CMOS technology. Fig. 13 provides its die photo, occupying an active area of 0.03 mm^2. The bare chip was mounted to a board, supplied by an external low-noise regulators. On-wafer probing was conducted to verify the PLL performance.

A. VCO

Measured VCO FTR is illustrated in Fig. 14, indicating an FTR from 32.5 to 39.5 GHz, with a 3-bit coarse frequency tuning. The VCO controlled voltage is allowed up to 1.8 V as thick-oxide varactors are utilized. The temperature drift rate for all VCO bands were measured to be ranged from −2.6 MHz/°C to −1.8 MHz/°C.

B. Reference Spur and Calibration

The 300 MHz reference clock was provided by the R&S SMF 100A. PLL reference spurs and phase noise were verified sing R&S FSUP 50 signal source analyzer, and time-domain experiment was conducted using Tektronix mixed domain oscilloscope. Fig. 15 provides the time-domain measurement of the calibration for ripple compensation. It was conducted long after the PLL was settled, and a reset signal initialized the process. As observed, the sweeping path continuously tunes the I_{MPR}, varying the level of the RCPD output voltage ripple. A sufficiently long time interval of ∼10 μs has been allocated for each state to ensure the PLL was well settled within it. At the end, the decision path chose the state at which the minimum ripple was found.

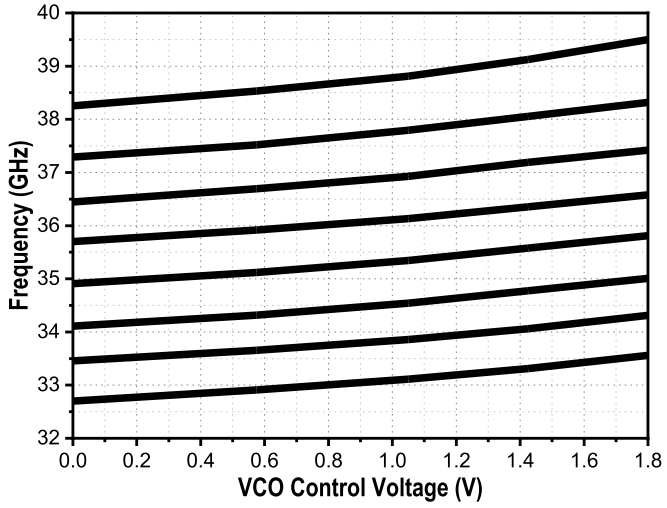

Fig. 14. Measured VCO FTR.

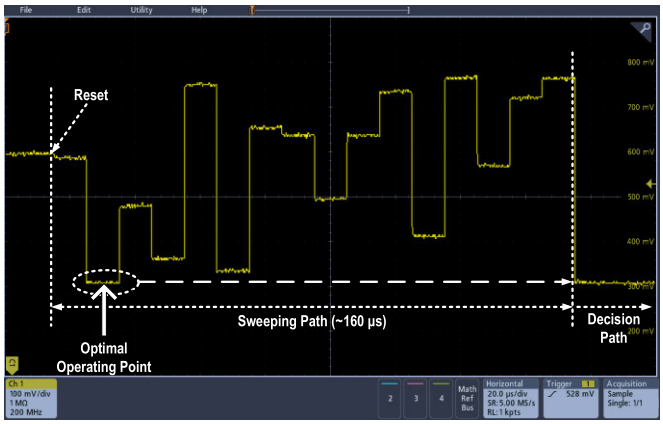

Fig. 15. Time-domain measured result of the calibration for ripple compensation.

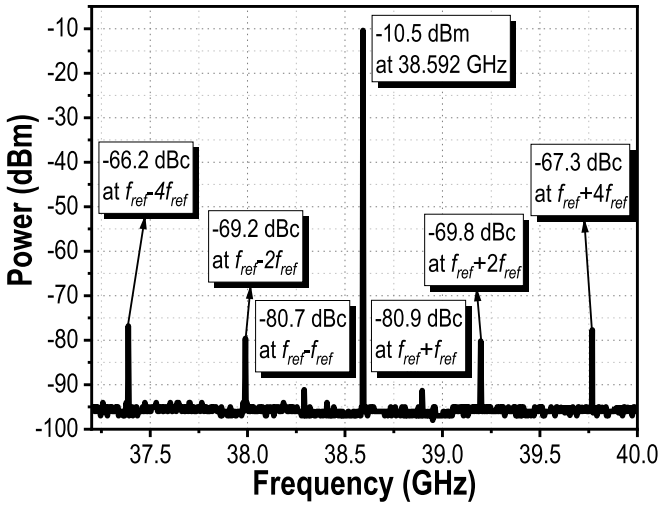

Fig. 16. Measured PLL reference spur with calibrator OFF.

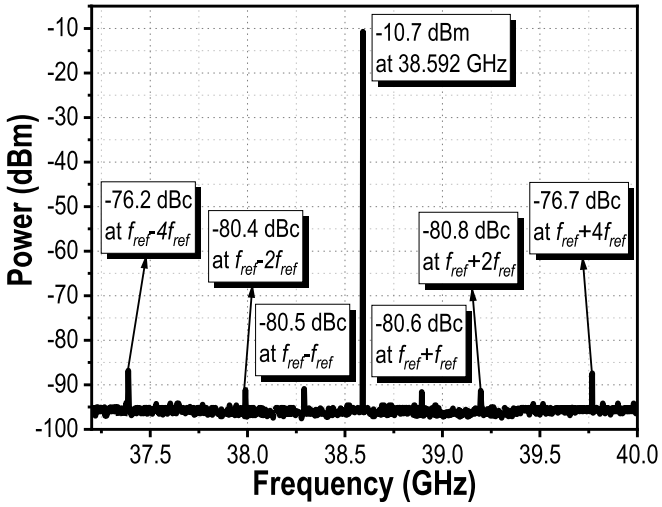

Fig. 17. Measured PLL reference spur with calibrator ON.

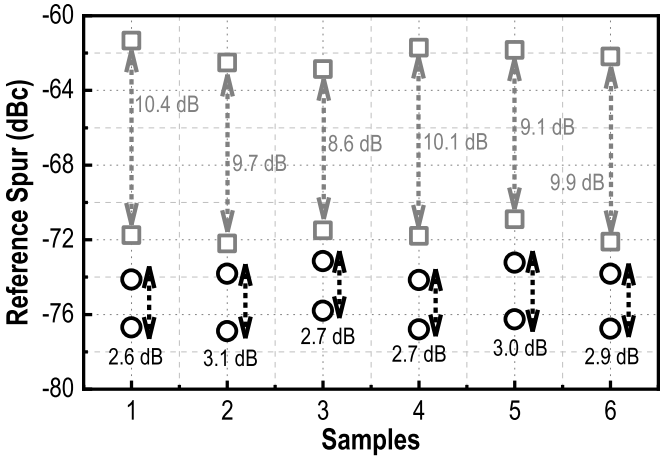

Fig. 18. Summary of mmW PLL reference spur over entire PLL FTR for 6 samples (rectangle: calibration OFF, circle: w/ calibration ON).

The measured reference spur w/o and w/ the above calibration is shown in Fig. 16 and Fig. 17, respectively. Clearly, the PLL generates spurs mainly at offset frequencies of $\pm f_{ref}$, $\pm 2f_{ref}$, and $\pm 4f_{ref}$. Among them, the $\pm f_{ref}$ spurs are small, possibly due to substrate coupling or electromagnetic crosstalk among wires. The $\pm 2f_{ref}$ spurs stem from unbalanced of ripple compensation, and also from direct coupling from both PDs to the VCO. The $\pm 4f_{ref}$ spurs, whose power level are dominating, are however owing to the ripple frequency boosting effect of the RCPD. Digital codes of <1111> has been assigned to the thermometer code converter for the case where calibration was OFF. As observed, with calibration ON, the reference spurs at $\pm 2f_{ref}$ and $\pm 4f_{ref}$ have been attenuated by 11.2 dB and 10.0 dB, respectively, indicating an improvement on the ripple compensation. Fig. 18 summarizes the measured reference spur w/ and w/o calibration for the entire PLL FTR for 6 samples. Obviously, the calibration scheme has enhanced the robustness of the ripple compensation.

In the case of calibration being performing for reference spur, Fig. 19 summarizes the measured reference spur against temperature variation without trigging a new calibration. The reference spur was degraded almost linearly with temperature, possibly due to worse matching in the RCPD, poorer matching in the TIA, as well as a higher leakage through the varactor, all of which cannot be calibrated against temperature variation in this implementation. A background calibration dedicated for temperature variation is desired in future work for compensating the above effects.

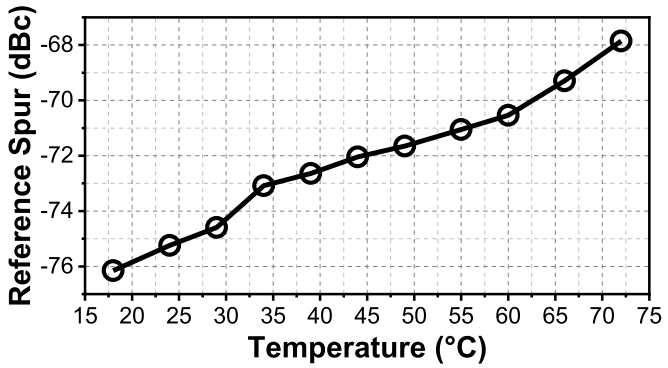

Fig. 19. Measured PLL reference spur against temperature variation without trigging a new calibration.

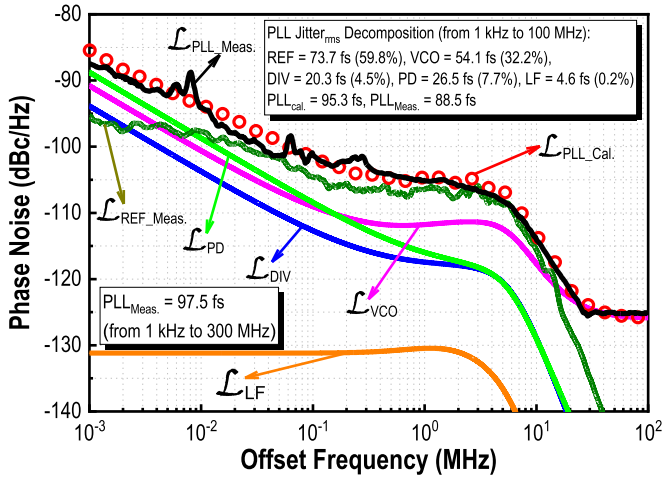

Fig. 20. Measured PLL phase noise, integrated jitter (σ_{rms}), and noise decomposition at 38.592 GHz.

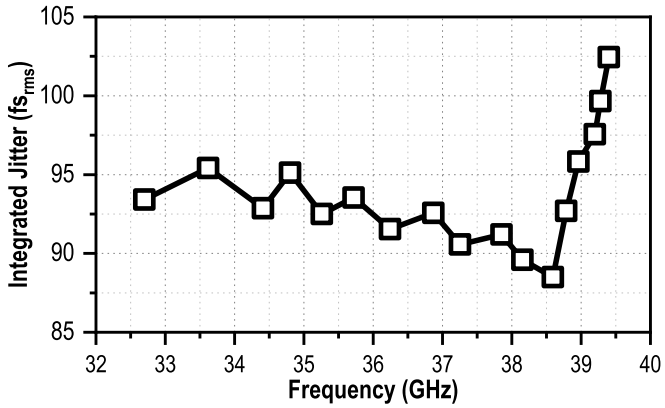

Fig. 21. Measured integrated jitter for the entire PLL frequency tuning range, integrated from 1 k to 100 MHz.

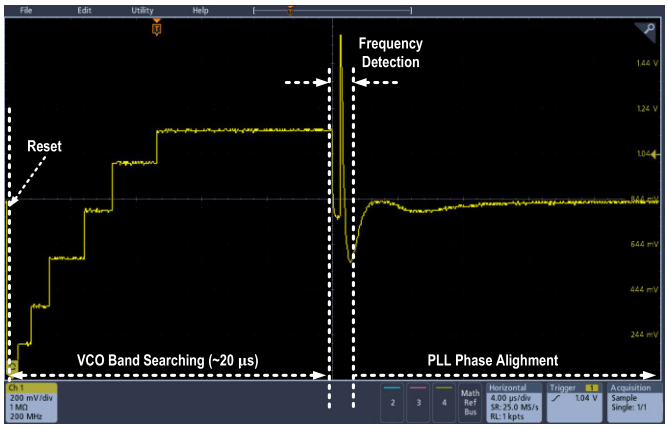

Fig. 22. Time-domain measurement of PLL settling behavior.

TABLE I
PLL POWER BUDGET

Building Block	Power Consumption (mW)
LC VCO + LDO	8.2–9.6
Miller divider	2.2–2.9
Divider chain	2.4–2.7
Input buffer + I/Q generator	1.6
RC-PFD	1.1-1.7
TIA	2.2–2.8
Clock buffers	3.6
RCPD calibrator (off automatically)	0.86
Lock detector (off upon lock)	1.2
MmW driver for testing	18–26
Total	21.3–24.9

C. PLL Phase Noise

PLL measured phase noise at 38.592 GHz and its corresponding noise decomposition is provided in Fig. 20. It measured −94.1 dBc/Hz and −105.2 dBc/Hz, respectively, at 10 kHz and 1 MHz offset. The calculated results fit closely with the measured results. The PLL integrated jitter (σ_{rms}) is 88.5 fs and 97.5 fs, respectively, when the integration range starts from 1 k to 100 MHz and 1 k to 300 MHz. The PLL phase noise becomes saturated for offset frequency beyond 100 MHz due to the low output power of the PLL. During the testing, the phase noise was measured long after the above calibration was completed. However, no observable variation was found for the phase noise when the calibrator remained OFF.

As observed from the noise decomposition, the PD noise, which includes the overall noise from the RCPD and the TIA, is no longer the dominant in-band noise source, thanks to the high PD gain provided by the TIA. The reference clock noise, which includes the measured noise of the clock input, the clock buffer, as well as the I/Q generator, dominates the overall PLL noise, by ∼60%. If a better crystal oscillator like the one adopted in [14] can be provided as the reference, the reference phase noise contribution will be significantly reduced from 59.8% to 1.9%, resulting in a better PLL RMS jitter of 64.4 fs$_{\text{rms}}$, which can be further improved by enlarging the loop bandwidth for more VCO phase noise suppression.

The measured PLL phase noise for the entire operating range is summarized in Fig. 21. Integrated jitter smaller than 103 fs (1 k to 100 MHz) was achieved.

D. PLL Locking Behavior

PLL settling behavior was measured as shown in Fig. 22. Upon assigning a reset signal, the PLL began with the lock detection. That was, the VCO state was initialized to <000>

TABLE II
SUMMARY OF RECENT SILICON-BASED MMW PLLS

	ISSCC'17 [8]	JSSC'18 [9]	TMTT'17 [25]	ISSCC'16 [26]	JSSC'15 [27]	JSSC'18 [28]	JSSC'22 [29]	ISSCC'20 [30]	**This work**
Technology	65 nm CMOS	130 nm CMOS	180 nm SiGe	65 nm CMOS	40 nm CMOS	28 nm CMOS	22 nm SOI	65 nm CMOS	**22 nm CMOS**
f_{ref} (GHz)	2.0–2.4	8.8–10	0.12	3.5	2.16	0.4915	2.5	0.25	**0.3**
f_{PLL} (GHz)	27.4–30.8	26.5–29.7	29.5–33.4	25.3–30.4	58.0–63.0	23.3–30.2	18.1–21.2	21.7–26.5	**32.7–39.4**
Multi. Ratio N	13	3	246–278	8	26–29	47–62	8	100	**128**
PN at 10 kHz	−100.9	−88#	−80	−96#	−54	−90	−85.8	−95.76	**−94.1**
PN at 1 MHz	−115.6	106.8	−97	−106.8	−104	−104	−109	−107	**−105.2**
$\mathcal{L}_{norm}$ (dBc/Hz^2) at 1 MHz	−232	−226	−227	−220	−227	−227	−221	−231	**−232**
Jitter (σ_{rms})	86 fs_{rms}	147 fs_{rms}	700 fs_{rms} $	107 fs_{rms}	1200 fs_{rms}	115 fs_{rms}	82.7 fs_{rms}	75.9 fs_{rms}	**88.5 fs_{rms}**
Integration Range	1 kHz −100 MHz	100 kHz −100 MHz	1 kHz −100 MHz	1 kHz −100 MHz	1 kHz −100 MHz	20 kHz −500 MHz	10 kHz−100 MHz	10 kHz− 30 MHz	**1 kHz −100 MHz**
Ref. Spur (dBc)	−39.1	−40	−40	/	−30	−65.1	−43	−45	**−76.2**
Power (mW)	24.3	23.2	63	87	40	31	36.5	16.5	**22.5**
Area (mm^2)	0.46	1	5.2	1.8	0.07	0.11	0.3	0.5	**0.03**
FoM (dB)	−247	−243	−225	−240	−222	−244	−246	−250.2	**−247.5**
$FoM_{JIT,N}$ (dB)	−259	−248	−250	−249	−237	−262	−255	−270	**−269**

#: measured at 100 kHz $: extracted from the published phase noise plot

and the PLL performed the VCO band searching at the smallest f_{VCO}. The frequency steadily rose up until a right band was found for the VCO, which took ∼20 μs. After that, the LD released the V_{ctrl} to the FD and RCPD, performing phase alignment. The frequency detection has to overwhelm phase alignment at the first place, by considering the finite acquisition range of the RCPD. It was automatically turned off when f_{div} is sufficiently closed to f_{ref}, then handed over the loop for phase alignment. The PLL took an overall settling time of ∼40 μs.

E. Performance Comparison

The mmW PLL power budget is provided in Table I. As the RCPD calibrator and the LD can be shut down automatically, their power have not been counted. Power burned by the mmW output driver has not been counted too, since it is only meant for testing, and not integrated in a future transceiver.

Standard metrics evaluating PLL performance involve $\mathcal{L}_{\text{norm}}$ [10], FoM [12], and $\text{FoM}_{\text{JIT,N}}$ [8], expressed as follows.

$$\mathcal{L}_{\text{norm}} = \mathcal{L}_{\text{in-band}} 20\log(N) - 10\log(f_{ref}), \tag{9}$$

$$FoM = 10\log\left[\left(\frac{\sigma_{rms}}{1s}\right)^2 \times \left(\frac{Power}{1mW}\right)\right], \tag{10}$$

$$FoM_{JIT,N} = 10\log\left[\left(\frac{\sigma_{rms}}{1s}\right)^2 \times \left(\frac{Power}{1mW}\right)\right] + 10\log\left(\frac{f_{ref}}{f_{PLL}}\right). \tag{11}$$

Recent silicon-based mmW PLL performance have been summarized in Table II. Thanks to the proposed ripple compensation technique, the achieved PLL reference spur is at least 10 dB lower than the design exploiting injection-locked PLL [8], [9], charge pump PLL [25], [26], [28], [29], and the PLL with charge − sharing locking technique [30]. The low reference spur level is primarily due to mutual spur cancellation, as well as the ripple frequency boosting effect, both enabled by the RCPD. Since the RCPD inherently evolved from a mixer PD, the high PD gain ensures its noise contribution to be smaller than the reference phase noise, leading to low-jitter performance. The push-pull fashion of the RCPD results in low power consumption when performing ripple compensation. With these merits, the attained σ_{rms}, $\mathcal{L}_{\text{norm}}$, FoM, and $\text{FoM}_{\text{JIT,N}}$ by the proposed PLL compare favorably with recent mmW PLLs.

VI. CONCLUSION

A ripple compensation phase detector (RCPD) for PLL reference spur suppression without degrading the PLL phase noise has been introduced in this article. It is featured by a pair of phase detector with mutual ripple compensation, for which the PLL loop bandwidth can be greatly increased to attenuate more VCO noise. A calibrator is proposed to enhance the matching between the two phase detectors. The RCPD is further extended to realize robust lock detection and frequency tracking.

Experimental results confirmed that the proposed millimeter-wave PLL achieved an FTR of 32.7 to 39.4 GHz, minimum integrated jitter of 88.5 fs_{rms} (integrated from 1 kHz to 100 MHz), and reference spur of −76.2 dBc. It attains a FoM of –247.5 dB and a $\text{FoM}_{\text{JIT,N}}$ of −269 dB. Since static phase error should be avoided along the phase detection path, the limitation of the proposed technique involves its availability to be exploited in a fractional-N PLL, which may create a tradeoff between the level of ripple compensation and fractional spur suppression.

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