

Performance Prediction of On-chip High-throughput Global Signaling

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Abstract : On-chip global signaling whose performance improves with technology advance is eagerly demanded. This work focuses on wave pipelining on on-chip transmission lines, which is one of probable solutions, and predicts the trend of signaling performance in the future. Experiments reveal that transmission capacity per channel will improve till at least 35nm technology in 10mm-long or below signaling. We also demonstrate that current-mode differential signaling is robust against power supply noise, but power delivery with non-zero impedance degrades the performance.

1 Introduction

Global interconnection delay is one of essential problems to prevent steady performance enhancement with technology advance. To overcome this problem, flip-flop pipelining is widely studied [1, 2]. However increase of power dissipation and latency due to inserted flip-flops/latches are very expensive. Figure 1 shows the propagation delay and transmission capacity of a conventional signaling scheme that transmits a single signal per clock cycle on a 10mm long wire. Although signaling on on-chip transmission lines helps to reduce the propagation delay compared with resistance-dominated wires, the time of flight will become a bottleneck since 150ps is necessary for a 10mm long interconnect in SiO₂, which means 10GHz operation is impossible in the conventional scheme. The speed of electromagnetic wave will be slower than demand in ITRS roadmap, though the wave speed is maximum physically and fundamentally. Wave pipelining on on-chip transmission lines (Fig. 2) is one of possible solutions that are currently studied [3, 4]. Several tens Gbps signaling per channel is promising, and the throughput is expected to improve thanks to technology advance.

Interconnect structure and material are not predicted to drastically change, and the performance of global interconnects in the topmost layer will be roughly unchanged because the top layer is not predicted to scale down. Reference [5] demonstrates that interconnects are capable of several tens Gbps signaling. In the current technology, the interconnect performance is relatively superior to transistor performance in high-speed signaling, and the transmission capacity is limited by the transistor performance. On the other hand, transistor performance is expected to improve steadily with technology advance. An issue to investigate is: 1) whether the signaling performance will improve steadily 2) in what technology the improvement of signaling performance will stop, i.e. when the performance of on-chip transmission line limits the signaling performance. Another issue is the performance evaluation under realistic environment. References [3, 4] report the signaling performance without power supply noise. In actual chips, power supply noise is severe and it may degrade the signaling performance.

The contribution of this paper is signaling performance prediction in the future, and evaluation of the robustness against power supply noise.

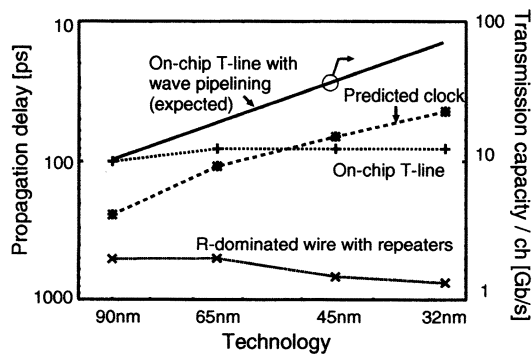


Figure 1: Signaling performance prediction.

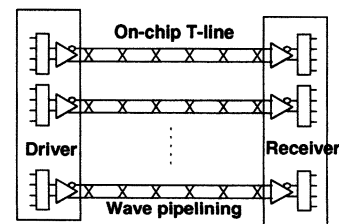


Figure 2: Wave pipelining on on-chip T-lines.

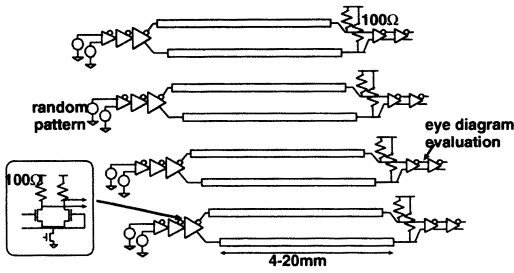


Figure 3: Differential signaling with CML driver and receiver.

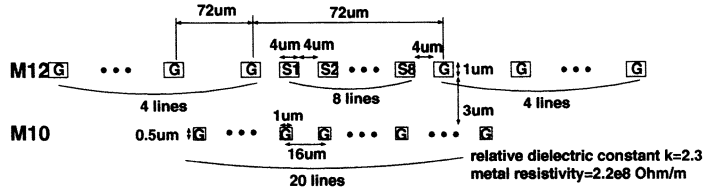


Figure 4: Interconnect structure.

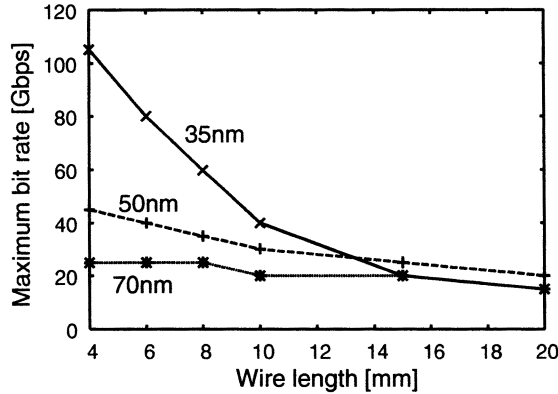


Figure 5: Relation between wire length and maximum bit rate in 35, 50 and 70nm technologies.

2 Performance prediction

We evaluate signaling performance in 70, 50 and 35nm technologies based on ITRS roadmap. The evaluated differential signaling circuit and the interconnect structure are shown in Figs. 3 and 4. The driver is a cascaded three-stage current mode logic (CML) driver, and the receiver is also CML. The termination resistor of 100Ω is close to the characteristics impedance of the transmission lines. The supply voltage of each technology is 0.7, 0.5 and 0.4V respectively. The signal swing is scaled according to the supply voltage. We inject random NRZ patterns and evaluate the eye diagram at the receiver output. We use transistor models developed based on ITRS roadmap [6]. The interconnect is modeled by a field solver and frequency-dependent coupled transmission line model [7, 8]. We vary the interconnect length (4-20mm), bit rate and technology, and evaluate the eye diagram by circuit simulation. We assume that a signaling whose eye opening in voltage is half of that in low-bit rate signaling is functional.

Figure 5 shows the relation between wire length and maximum bit rate in 35, 50 and 70nm technologies. In each technology, the maximum throughput increases as the wire length becomes small. In the region above 10mm length, the signaling performance hardly improves even though transistor performance becomes better. In this region, the interconnect performance limits the maximum transmission capacity. On the other hand, in the region below 10mm, the maximum bit rate improves as technology advances. For example, the maximum throughput increases 25 to 60Gbps in 8mm long signaling. We can guess that the transmission capacity per channel of 4-8mm long signaling will improve in finer technologies beyond 35nm. The expectation that throughput per channel will steadily improve as technology advances in Fig. 1 is appropriate.

3 Impact of PG noise on signaling

Current-mode differential signaling is more robust than voltage-mode single-end signaling against power supply noise [9]. However, the amount of performance degradation of on-chip high-speed signaling is not clearly studied. This section shows a case study in the 50nm technology.

We attach a power grid model that includes wire resistance, wire inductance, series-connected resistance and capacitance that correspond to stable logic gates and well junction [10] (Fig. 6). The power grid is connected to the ideal power source and ground through series-connected resistance and inductance that represent flip-chip package and bumps. The number of bumps is 100. The chip size is 6x6mm, and the pitch of power lines is $250\mu\text{m}$. The ground lines are routed similarly next

to the power lines. The wire width is $30\mu\text{m}$. The impedance between power and ground at CML drivers is shown in Fig. 7. The impedance reaches a peak at 18GHz. We model switching circuits as current sources whose waveform is triangle. The frequency of switching logic is 10GHz. We randomly change the amount of current at each point and in each cycle. An example of the power/ground noise in this situation is shown in Fig. 8(a). The peak to peak noise voltage is about 50mV, where the supply voltage is 0.5V.

Figure 9 demonstrates the eye diagrams in the case of 10mm long signaling at 30Gbps. Figure 9(a) is the eye diagram in the case that the power grid and current source (switching logic) are attached. In Fig. 9(b), no current sources are not attached i.e. only the signaling circuit is operating. In Fig. 9(c), the power grid is not connected i.e. the power and ground are ideal. Comparing Fig. 9(b) with (c), we can see that the non-ideal power supply degrades the eye diagram. On the other hand, the power/ground noise due to switching logic hardly affects signaling quality (Fig. 9(a) and (b)), where the power and ground voltage corresponding to Fig. 9(b) is Fig. 8(b). This result implies that providing low-impedance power delivery is more important than suppressing noise magnitude for current-mode differential signaling.

Figure 10 shows the relation between bit rate and eye opening in voltage with and without power noise. In this experiment, the magnitude of 0.1V is the threshold for judging whether the signaling is functional or not. With this metric, the maximum transmission capacity decreases from 30Gbps to 25Gbps by 17% due to power supply with non-zero impedance.

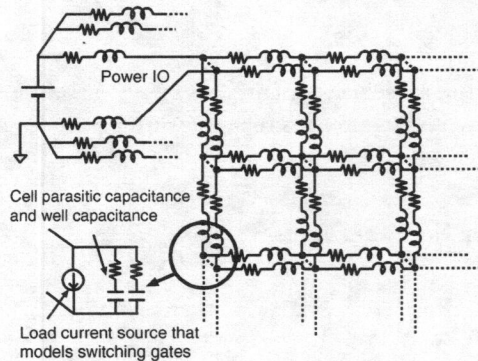


Figure 6: Power grid model.

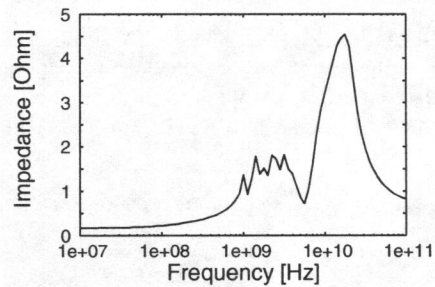


Figure 7: Impedance between power and ground at drivers.

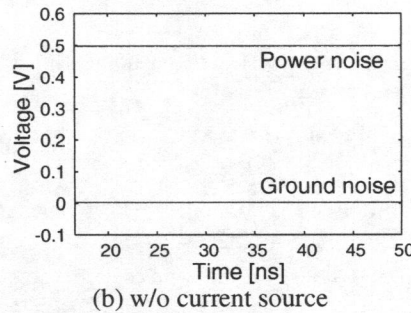
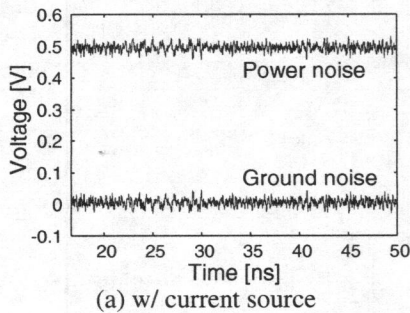


Figure 8: Power, ground noise.

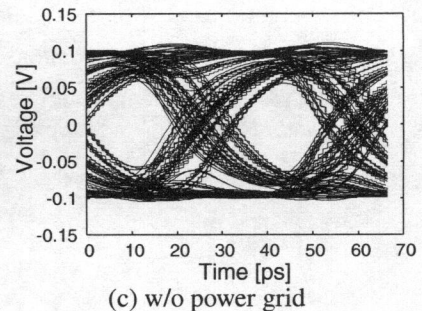
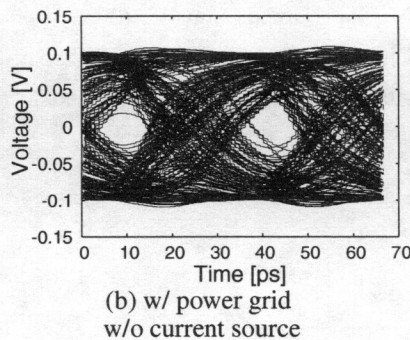
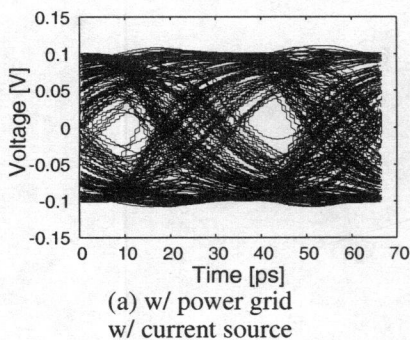


Figure 9: Eye diagrams (10mm, 30Gbps)

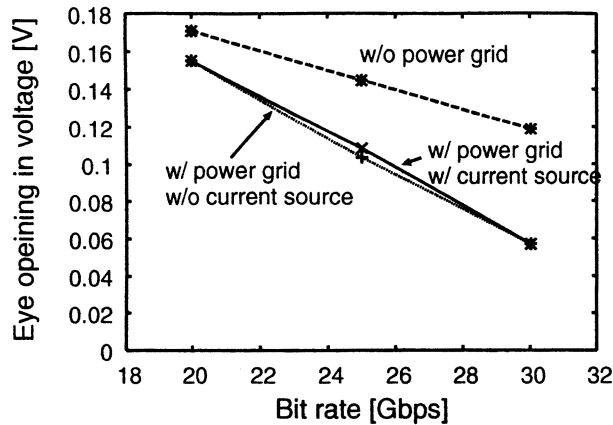


Figure 10: Eye opening in voltage w/ and w/o power grid, and w/ and w/o current source.

4 Conclusion

This paper evaluates the performance in the future of current-mode differential signaling for global interconnection. Our experiments reveal that the transmission capacity per channel will improve as technology advances in several millimeter long signaling. We also experimentally demonstrate that current-mode differential signaling is robust against power supply noise, but finite impedance of power delivery degrades the signaling performance.

Acknowledgment

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