Input Capacitance Modeling of Logic Gates for Accurate Static Timing Analysis

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***Abstract*— This paper discusses how to improve input capacitance modeling of logic gates for accurate STA(static timing analysis). The input capacitance of logic gates exhibits non-linear behavior with respect to input signal voltage. Also, its value varies depending on the driving condition of stable inputs as well as loading of multiple-input gates condition of the gate. For the non-linearity issue, we propose to use an equivalent capacitance value derived by the integration of input current during partial transition instead of full transition. For the second issue, we suggest to consider the minimum capacitance as well as the maximum capacitance, which will eliminate possible errors in the shortest path calculation for hold violation analysis.**

I. INTRODUCTION

The integration scale of circuits keeps increasing for technology progress. The timing constraint of scaled circuits has become tighter and tighter and hence the design margin should be reduced as much as possible for pursuing faster operation. In such a design environment, STA (static timing analysis) is the only viable method for chip-level timing analysis and therefore its accuracy should be of primary importance.

There are many factors that affect the accuracy of STA. Among them, the input capacitance modeling of logic gates is an important factor because a significant amount of load capacitance is still occupied by the input capacitances of gates except for interconnect dominated sections such as clock trees and busses. In STA, the input capacitance of a gate is modeled as a lumped capacitance. There are a few papers that explain the importance of the capacitance modeling [1]–[3]. However, the method of deriving the value of the input capacitance has not been paid enough attention to. Also, although commercial tools for library characterization measure input capacitance under various conditions [4], it is common to pick the maximum value for the inclusion in a timing library. In such a case, the STA can predict the longest delay without optimism so that we can safely check set-up constraints. On the other hand, if we want to analyze the shortest-path delay, the resulting timing is overestimated and there is a possibility of existing shorter delays, which will lead to hold violations.

In this paper, we first discuss the method for deriving a capacitance value of logic gates. Then, we show the importance of having the minimum capacitance value as well as the maximum for accurate timing analysis. Section II describes the non-linear nature of the input capacitance and how it's value varies according to the driving and loading conditions. In Sec. III, we propose a method for deriving an input capacitance and show that the minimum capacitance values are indispensable for timing verification in addition to the maximum values. Section IV concludes the discussion.

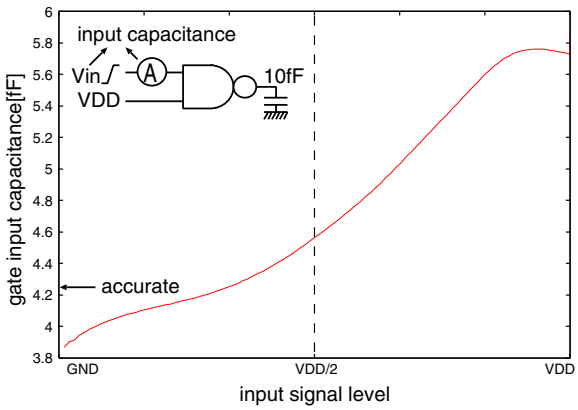

Fig. 1. Non-linear characteristics of the input capacitance.

II. THE CONDITION OF GATE LOADS IN THE MODELING

In this section, we show the characteristics of input capacitance under various driving and loading conditions. We use a two-input NAND gate in a 0.13μm CMOS process as an example. All the characteristics are obtained by circuit simulation (SPICE) using transistor models supplied from a foundry.

First, we show the non-linearity of the input capacitance in Fig. 1. We apply a ramped input signal from GND to VDD with 100ps transition time to "A" input of the NAND gate while keeping the "B" input to VDD (See Fig. 1). The load capacitance of the gate is 10 fF that nearly equals to the load of FO2. The vertical axis represents the input capacitance value that is calculated by integrating the input current from GND to the corresponding input signal level. The input capacitance varies from 3.8fF at the beginning of the input transition to 5.7 fF at the end of the input transition.

Given this non-linear behavior of input capacitance, the problem of input capacitance modeling is to find the value of an equivalent lumped capacitance that results in the same delay when the gate is replaced by the capacitor. Figure 2 illustrates this problem. In the upper circuit, the first gate is driving the second gate with a certain load. What we want to derive is the equivalent capacitance that

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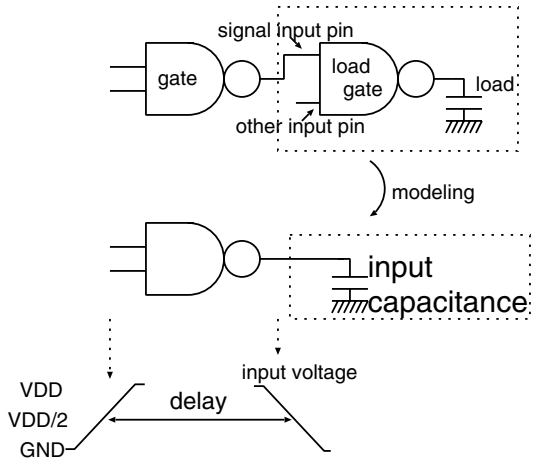

Fig. 2. Input capacitance modeling.

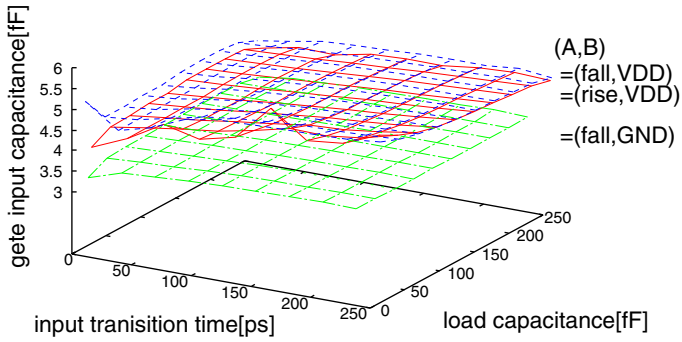

Fig. 3. Gate input capacitances at each condition(A=falling input, B=VDD or A=falling input, B=GND or A=rising input, B=VDD)

produces the same amount of delay for the first gate when the second gate is replaced by a capacitor. In the example of Fig. 1, the equivalent capacitance value becomes 4.3 fF which is indicated as "accurate". It is clearly seen that the input capacitance value of 5.7 fF that is derived from the integration over the whole input transition, which is a typical method for input capacitance calculation, leads to 33% over estimation which will introduce a noticeable error in timing analysis.

Next, we will examine how this equivalent input capacitance varies according to the driving and loading conditions of the gate. The factors considered and their ranges are listed below.

- the capacitance of the load (2fF–250fF)
- the transition time of the input signal (5ps–250ps)
- the transition direction of the input signal (rising, falling)
- the input pin (A, B)
- the voltage of the stable input (VDD, GND)

The ranges of the load capacitance and the transition time are identical to those of the lookup tables for delay analysis used in the STA.

Figure 3 shows the amount of gate input capacitance as a function of the input transition time and the load capacitance for three cases of (A, B)=(fall, VDD), (rise, VDD) and (fall, GND). For each case, it can be seen that the input capacitance does not vary much with respect to the input transition time and the load capacitance. Also, two cases of (A, B)=(fall, VDD) and (rise, VDD) result in almost the same capacitance value. The difference is less than 1 % on average. For those cases, we can safely use a single value for the entire region of the load capacitance and the input transition time. On the other hand, the case of (A, B)=(fall, GND) results in a quite different value. It is about 20 % smaller than those of the other two cases. It is common to choose the maximum value for input capacitance. It is reasonable for the longest delay analysis, that is, for "set-up time" analysis. However, the maximum value is not at all adequate for the shortest delay analysis, that is, for "hold time" analysis that is equally important in timing verification. Therefore we cannot use a single value for the gate input capacitance, but at lease use the maximum and the minimum values as well. Similar discussion holds for the input "B".

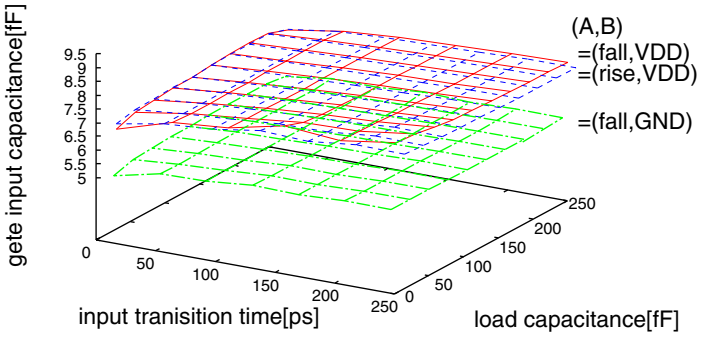

Fig. 4. Gate input capacitances at each condition using 0.18μm process(A=falling input, B=VDD or A=falling input, B=GND or A=rising input, B=VDD)

Figure 4 verifies the results by using another fabrication process, 0.18μm. The input capacitance in Fig. 4 does not vary much with respect to the input transition time and the load capacitance, too. The cases of (A, B)=(fall, VDD) and (rise, VDD) result in almost the same. The input capacitance in the case of (A, B)=(fall, GND) is about 30% smaller than those of the other two cases.

So far, we focus on the method for deriving the amount of lumped capacitance that results in the same delay time when the actual loading gate is replaced by the lumped capacitor. In a static timing analysis, besides the delay time, we have to calculate the transition time of the output signal. Similar discussion may hold for the derivation of the equivalent input capacitance for calculating the output signal transition time. However, transition time is the secondary factor for delay calculation, and hence we may use the delay-equivalent input capacitance for the calculation of output transition time. Figure 5 shows the amount of error in the calculation of output signal transition time when we use the delay-equivalent input capacitance instead of the actual loading gate. The error ranges from -1% to 10% and the average is around 4%. This amount of errors in the output transition time does not affect much in the calculation of delay time for the fan-out gate. A path delay calculation explained in

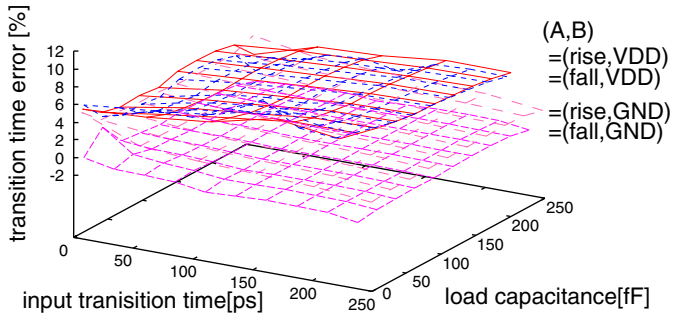

Fig. 5. The transition time error in the input capacitance modeling at each condition.

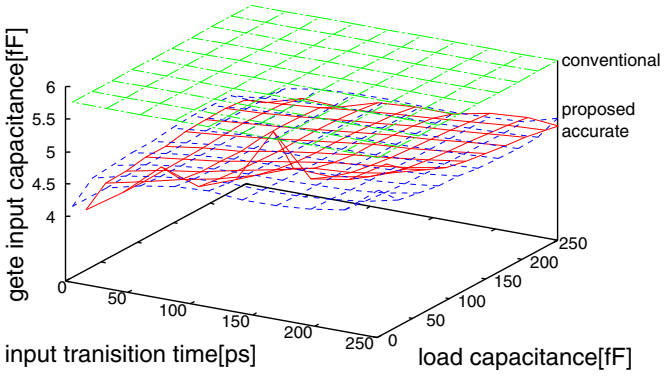

Fig. 6. Gate input capacitances (A=rising input, B=VDD).

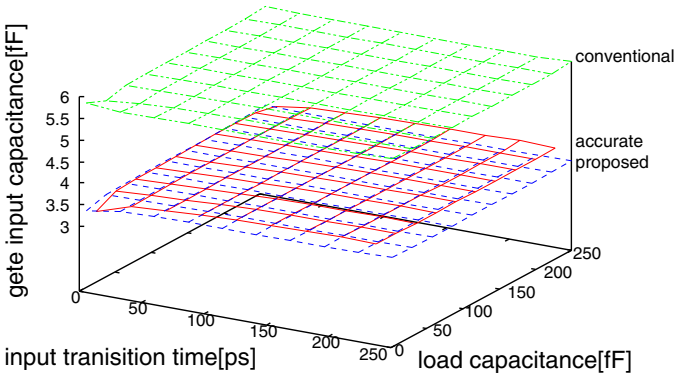

Fig. 7. Gate input capacitances (A=falling input, B=GND).

a later section (Sec. III-B) will confirm this observation. In this example, we can safely use the delay-equivalent input capacitance for both delay time and transition time calculation.

III. How to obtain the value of gate input capacitance

The method to derive the equivalent capacitance described in Sec. II requires a repetitive search using transient analysis. Our discussion in the previous section reveals that we can use a single value for the entire region of the input transition time and the load capacitance. In this case, we may use a less troublesome but accurate enough method to find the input capacitance.

A typical method for deriving an input capacitance, which can be found in commercial tools, is to integrate the gate input current over the whole input transition by applying a full transition signal to the corresponding input. As described in the previous section, this value corresponds to the rightmost value in Fig. 1, and this results in 33 % over estimation in this case, which is not acceptable.

A reasonable method is to integrate the input current from the beginning of the transition to a certain voltage level, not to the end of the transition. Here we propose to use the logical threshold voltage defined in the library for the end of the integration. It is the reason that the input voltage transition of the load gate in obtaining the delay is from the beginning to the logical threshold voltage. In the example explained in Sec. II, the logical threshold voltage is "VDD/2". As seen in Fig. 1, this condition results in 4.5 fF which is a good approximation to the accurate value of 4.3 fF.

A. Accuracy of Modeled Capacitance Values

The accuracy of the proposed integration scheme is explained in Figs. 6 and 7. Input capacitance values obtained by the integration of the input current to the logical threshold voltage("VDD/2") (denoted as "proposed") and to the end of the transition(denoted as "conventional") are derived and compared with the accurate value that gives the same amount of delay, over the whole region of the input transition time and the load capacitance. As we expected, the proposed integration scheme gives a good approximation. Average error over the entire region is 3.2 % and 2.2 % in Figs. 6 and 7, whereas the error of the conventional method is 23 % and 61 %.

Figures 8 and 9 show the results when we assume 0.18μm process. Figure 8 shows the case of (A, B)=(rise, VDD) and Fig. 9 shows the case of (A, B)=(fall, GND). The average error over the entire region is 1% and 1% in Fig. 8 and Fig. 9 respectively. On the other hand, the error of the conventional method is 30% and 70%.

Figures 6 and 8 corresponds to the case of (A, B) = (rise, VDD) which is the maximum value for the input terminal A. Figures 7 and 9 corresponds to the case of (A, B) = (fall, GND) which is the minimum value for the input terminal A. We should use for the former value for the longest path delay calculation, whereas we should use for the latter value for the shortest path delay calculation. In either case, the input capacitance varies little over the whole region of the input transition time and the load capacitance. We can use a single value obtained at, for example, FO4 load and FO4 transition time.

B. Comparison in Signal Propagation Delay

This section examines the accuracy of the input capacitance modeling proposed in the previous section using a simple circuit shown in Fig. 10.

We analyze the path delay of the circuit using two modeling methods: the proposed method described in Sec. III and the conventional method in which the integration of the input

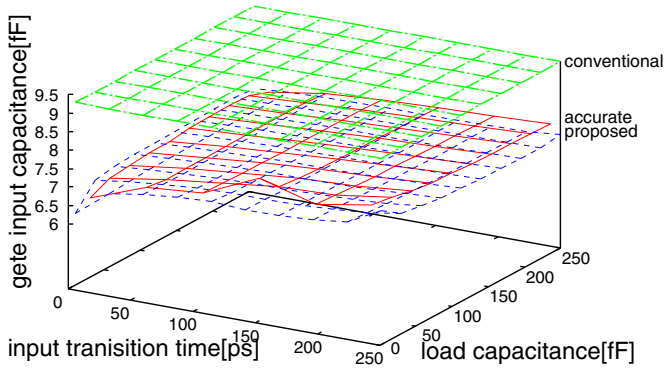

Fig. 8. Gate input capacitances using 0.18μm process(A=rising input, B=VDD)

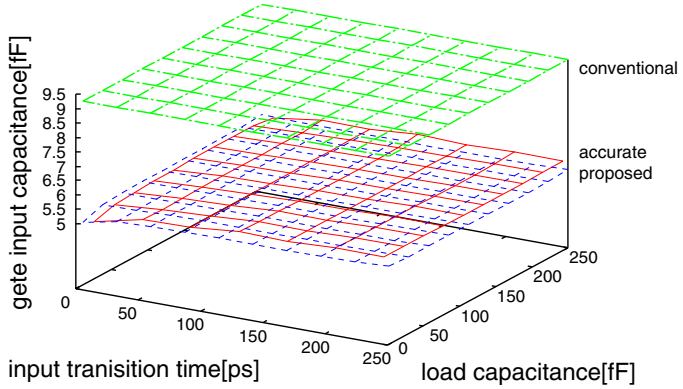

Fig. 9. Gate input capacitances using 0.18μm process(A=falling input, B=GND)

TABLE I

DELAY ERROR AT EXAMPLE CIRCUIT(FIG. 10) WITH CONVENTIONAL OR PROPOSED METHOD

method	delay_{1-4}[psec]	error[%]
circuit simulation	155.2	—
conventional	200.4	29.1
proposed	152.2	−1.9

current is conducted over the whole transition region and a single value of the maximum capacitance is always used as the input capacitance.

Table I summarizes the delay and the error compared with the delay obtained by circuit simulation. As expected, the conventional delay is almost 30% larger than the actual, whereas the proposed scheme gives the error as low as 2%.

Table II shows the errors in signal propagation delay of the same circuit with the 0.18μm process. The error with the proposed method is about 3% whereas the conventional method causes almost 30% error.

From the each verification, our method provides a good approximation even if the fabrication process is changed.

IV. CONCLUSION

This paper discusses a method to model the gate input capacitance for accurate STA. For static timing analysis, we

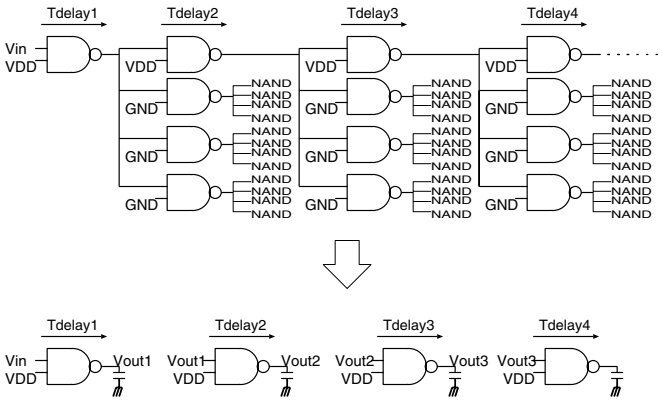

Fig. 10. A circuit used for the comparison.

TABLE II

DELAY ERROR AT EXAMPLE CIRCUIT(FIG. 10) WITH CONVENTIONAL OR PROPOSED METHOD USING 0.18μm PROCESS

method	delay_{1-4}[psec]	error[%]
circuit simulation	343.1	—
conventional	434.6	27
proposed	330.8	−3.5

have to model the gate input capacitance, that is the non-linear capacitance by the lumped capacitance.

A method widely used is calculating the equivalent capacitance from the integral of the current flowing into the gate capacitance. A conventional method derives the equivalent capacitance by integrating over the full transition range of the applied input signal. The capacitance by the conventional method is the maximum capacitance and it provides pessimistic delay. The pessimistic delay estimation is reasonable for checking setup time constrains, but it can cause hold violation. The proposed method derives the equivalent capacitance by the integral from the beginning of the input transition to the logical threshold voltage.

Experimental results show that the conventional method overestimates the input capacitance by 30% and cause over 30% error in delay. The error of the conventional method is clearly unacceptable when it is used in the shortest path delay calculation for the verification of hold-time violation. On the other hand, the errors of the proposed method are 2% in capacitance and 1% in delay. By using the proposed method, we can improve the accuracy of STA and eliminate possible errors in the shortest path calculation for hold violation analysis.

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