A Sampling Switch Design for Liquid Crystal Displays

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***Abstract*— In the design of an active matrix LCD, the ratio of the pixel voltage to the video voltage, abbreviated to RPV, is an important metric of the performance, since the pixel voltage determines the transmitted luminance of the pixel. Hence, in the design of a source driver circuit for an LCD, of primal importance is the issue of how to restrict the admissible allowance of the RPV of a pixel within a specified narrow range. This constraint on the RPV is analyzed in terms of parameters associated with the sampling switch and the sampling pulse, and then by using a minimal number of these parameters, a design scheme is described dedicatedly for the sampling switch, which finds an optimal sampling switch size and an optimal sampling pulse waveform. Experimental results show that an optimal sampling switch attained by the proposed scheme gives rise to a source driver with almost 50% less power consumption than the one by manual design.**

***Index Terms*— CAD tool, sampling switch, sampling pulse, column driver circuit, active matrix liquid crystal display**

I. Introduction

LCDs (Liquid Crystal Displays) have established a firm foothold on the market as flat panel displays, first for calculators, subsequently for personal computers, mobile appliances, digital cameras, etc., and at present with increasing importance for TVs. Thus, development is continuing further on the picture quality as well as the picture function of LCDs, and hence the design automation has to be enhanced more and more for drivers which affect most the performance of LCDs[1] .

In the *TFT*(Thin Film Transistor)-addressed LCD, usually called *active matrix LCD*, as illustrated in Fig.1, the grey shade is controlled individually in each pixel by applying an appropriate pixel voltage. In each column of the column driver circut, a pair of nMOS and pMOS TFTs connected in parallel operates as a sampling switch, which is to sample the video signal and to transmit the signal to the source line, as shown in Fig.2. During the period when a row of pixels are activated by the gate line in the row, the video information (i.e. video voltage) corresponding to a desired gray shade is fed into each pixel in the row, from column to column, whereas all pixels in other rows are blocked by grounding their gate lines.

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Thus, during this period the source drivers have to activate all pixels in the row, and hence the operation speed of the source driver in each column, henceforth designated as *column driver*, is far greater then that of the gate driver in each row, henceforth referred to as *row driver*. This implies that the column driver acts a principal role to determine the RPV (Ratio of Pixel voltage to Video voltage) of each pixel.

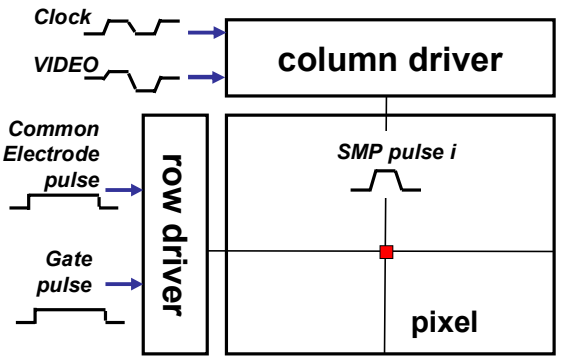

Fig. 1: An active matrix LCD

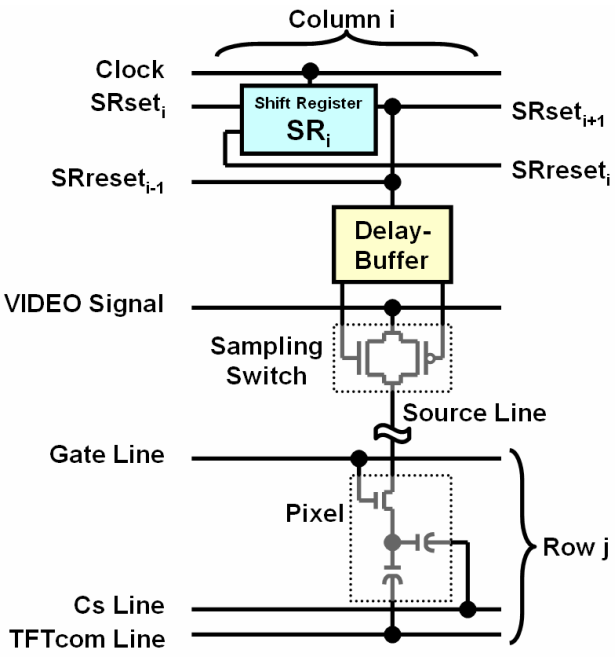

Fig. 2: A circuit for a column of the column driver in active matrix LCD

Given a pixel, let V_{vd} denote the video voltage to be fed into it, and let V_{px} represent the pixel voltage. Then for this pixel we have RPV = $(V_{px}/V_{vd})\times100$[%]. Our ideal goal is how to make this RPV approach to 100[%], or in other words, how to make each pixel attain the desired grey shade.

Recently, with the advance of LCD technologies, the column and row drivers have to be implemented more and more finely on the same substrate as the picture plane. However, in such implementation there occur considerable fluctuations in the transistor performance, which make the design of column drivers difficult from the aspect of the functional verification as well as the minimization of circuit area and power consumption.

We are now studying about a CAD tool for a circuit for one column of a column driver aiming at the following objectives:

- Given a specified value B, restrict the RPV within 100±B [%].
- Minimize the power consumption.
- Minimize the delay and its fluctuation of the sampling pulse from the system clock.
- Implement the column circuit within a certain width specified for a pixel column.

To achieve these objectives, the most intensive work is on the subject of how to determine the size of each transistor in the column driver. This paper intends to seek a design scheme dedicated for the sampling switch of a column driver.

In the following, we first analyze how the design parameters of sampling switch and sampling pulse are related to the RPV, and then seek a minimal number of parameters which contribute most to the behavior of RPV. With the use of these parameters, we propose a design procedure to find an optimal sampling switch size and an optimal sampling pulse waveform. This procedure repeats the circuit simulation SPICE for the circuit modeling a sampling switch and the pixel, and the number of repetitions is reduced by using the minimal number of parameters. Experimental results show that an optimal sampling switch attained by this procedure gives rise to a column driver with almost 50% less power consumption than the one by manual design.

II. Preparations

A. Definitions of Symbols

First, we define design parameters denoting a sampling switch and a sampling pulse. Let W_n be the gate width of an nMOS TFT, and let *SMP* denote a sampling pulse input to this nMOS TFT, for which the rising time, falling time, and intermediate time between them are denoted by t_r, t_f, and t_w, respectively. Similarly, let W_p be the gate width of a pMOS TFT, and let *SMPB* designate a pulse input to this pMOS TFT. For simplicity, let both of SMP and SMPB be of the piece-wise linear waveform, reverse to each other. Thus, W_n, W_p, t_r, t_f, and t_w are regarded as the basic design parameters for sampling switch.

B. Types of Feeding

Although t_r, t_f, and t_w are common to SMP and SMPB, RPV changes differently according as the combination of video voltage V_{vd} and common electrode voltage V_{com} differs, as outlined in what follows.

Here, it should be remarked that the common electrode voltage V_{com} for a row of pixels alternates a high voltage level $V_{com\text{-}high}$ and a low voltage level $V_{com\text{-}low}$, frame by frame, that is, if a pixel receives a video signal when V_{com} is at high level $V_{com\text{-}high}$, then next time it receives a video signal, V_{com} is at low level $V_{com\text{-}low}$. If V_{com} of a row of pixels is set to the low level $V_{com\text{-}low}$, then the pixel voltage of each pixel of the row is lowered, and it is raised to a given video voltage when the sampling switch corresponding to a pixel of the row is open. This type of feeding of a video signal to a pixel is designated as *plus* feeding. On the other hand, if V_{com} is set to the high level $V_{com\text{-}high}$, then the pixel voltage of the row is raised, and it is lowered to a given video voltage when the sampling switch is open. This type of feeding is *minus* feeding.

Between these two types of feeding, we can consider the type such that pixel voltage is *harder* to reach a given video voltage. The type can be found by a few SPICE simulations for the circuit consisting of the sampling switch and the pixel circuit with respect to a few typical values of sampling swtiches. For example, in our experimental results, the minus feeding is the harder case in feeding video voltage into a pixel, that is, in the case of minus feeding, the time from the beginning of t_r to the instance when pixel voltage V_{px} approaches enough to video voltage V_{vd}, is longer than that of plus feeding. Such a harder case can be used to determine the minimum values $W_{p\text{-}min}$ and $W_{n\text{-}min}$ of widths W_p and W_n of sampling switch. Namely, in such a case, if widths W_p and W_n are less than $W_{p\text{-}min}$ and $W_{n\text{-}min}$, respectively, then RPV may not exceed 100−B[%]. Of course, the minimum values $W_{p\text{-}min}$ and $W_{n\text{-}min}$ depend on the lengths of t_r, t_w, and t_f, so that finding these minimum values is not an easy task. But, we can obtain the lower bound of the widths of sampling switch by repeated application of SPICE simulation for typical combinations of video voltage V_{vd} and common electrode voltage V_{com}.

C. Charge Injection

Although pixel voltage V_{px} has been equal to a given video voltage before SMP pulse is falling or the sampling switch turns off, V_{px} may change by the *channel charge injection* after the sampling switch turns off[2,3,4]. This voltage change ΔV_{px} is dependent on W_n, W_p, and source-gate voltage V_{gs} of TFT. If V_{gs} is constant, then we can make this voltage change ΔV_{px} zero by imposing a relation $W_p = a\cdot W_n + b$ on the widths W_p and W_n of nMOS and pMOS, respectively. However, the coefficients a and b of this equation are constants dependent on V_{gs}, and V_{gs} varies according as video voltage V_{vd} changes. Therefore, it is impossible to make ΔV_{px} zero for any V_{vd}. However, it is possible for a particular voltage of V_{vd} by an explicit relation between W_n and W_p.

Noting the nonlinear relation between the transmitted luminance and pixel voltage V_{px}, we can see that there exists a pixel voltage $V_{px\text{-}mdl}$ which changes the transmitted luminance most steeply. If we reduce the change ΔV_{px} of the pixel voltage to zero at this voltage $V_{px\text{-}mdl}$, then the difference of the transmitted luminance caused by the charge injection can be reduced as small as possible. Therefore, we seek this voltage $V_{px\text{-}mdl}$, and by using the source-gate voltage V_{gs} attained by $V_{px\text{-}mdl}$, we find constants a and b which reduce ΔV_{px} to 0.

Since ΔV_{px} is zero only at $V_{px\text{-}mdl}$, at other V_{px} (that is, at the video voltage V_{vd} which does not attain the pixel voltage $V_{px\text{-}mdl}$), pixel voltage V_{px} may change after the sampling switch turns off. Therefore, due to the charge injection, it becomes harder to satisfy the constraints on RPV for any video voltage V_{vd}. However, since the relation $W_p = a \cdot W_n + b$ is imposed on W_p and W_n, the basic design parameters for sampling switch can be reduced to W_n, t_r, t_f, and t_w.

Here, it should be added that the pixel voltage change ΔV_{px} may be larger than 0 at a certain video voltage V_{vd}, and hence it may happen that RPV exceeds 100+B[%] after the sampling switch turns off. This type of violation can happen in an *easier* case of feeding video voltage V_{vd} into a pixel, that is, in the case when pixel voltage V_{px} approach more quickly to V_{vd} than a harder case.

Such an easier case can be used to determine the maximum value $W_{n\text{-}max}$ of width W_n. Namely, if width W_n is increased for satisfying the constraint of 100–B[%] and becomes greater than $W_{n\text{-}max}$, then RPV may exceed 100+B[%] in the easier case. Similarly to the minimum value $W_{n\text{-}min}$, $W_{n\text{-}max}$ depends on the lengths of t_r, t_w, and t_f, but we can obtain the upper bound of W_n by repeated application of SPICE simulation.

D. Fluctuations

In the real world of producing active matrix LCDs, there exist a large variety of fluctuations in the design parameters, transistor performances (SPICE parameters), voltage sources, etc., mainly incurred by the implementation of driver circuits on the same substrate as the picture plane. Therefore, of practical importance are technical ideas of how to treat these fluctuations in the process of designing the sampling switch. In our design we consider the following fluctuations.

- Gate widths W_n and W_p fluctuate within $W_n \pm \sigma_n$ and $W_p \pm \sigma_p$, respectively.
- The high and row voltage levels V_{high} and V_{low} of pulse SMP (SMPB) fluctuate within $V_{high} \pm \upsilon_{high}$ and $V_{low} \pm \upsilon_{low}$, respectively. The supply voltage V_{dd} and V_{ss} also fluctuate, but in the sampling switch these voltages do not appear explicitly. So, we do not introduce symbols for these fluctuations.
- SPICE parameters of nMOS and pMOS of the sampling switch fluctuate among best, typical, and worst cases, and we consider 5 combinations of fluctuations such as nBpB, nTpT, nWpW, nBpW, and nWpB, where n and p denote nMOS and pMOS, respectively, and B, T, W denote best, typical, and worst cases, respectively.

Due to the fluctuations of supply voltages and transistor performances in the delay-buffer circuit, the waveform of SMP pulse also fluctuates. We assume that t_r, t_f, and t_w of SMP pulse fluctuate within $t_r \cdot (1 \pm \varepsilon_r)$, $t_f \cdot (1 \pm \varepsilon_f)$, and $t_w \cdot (1 \pm \varepsilon_w)$, respectively, where ε's are between 0 and 1. Moreover, let T denote the length of the time frame when the video signal keeps a voltage for a pixel, which is equal to a half of the period of the system clock, and let us assume that this time period T also fluctuates within $T \cdot (1 \pm \varepsilon_T)$, where ε_T is between 0 and 1.

Since these ε's are dependent on the performance of the delay-buffer circuit to generate SMP and SMPB, they are unknown in advance. Namely, we are now considering the conditions of SMP and SMPB pulses which satisfy the constraints of RPV, and using these conditions of SMP and SMPB pulses the delay-buffer circuit is designed. Hence, let us assume that estimated values of these ε's are given in the following.

Due to the fluctuations introduced above, the classification of harder and easier cases of feeding video signal into a pixel becomes complicated. In the following, *harder cases* of feeding mean the cases where W_n must be increased so as to raise RPV over 100–B[%], and *easier cases* of feeding mean the cases where W_n must be decreased so as to lower RPV below 100+B[%]. Roughly speaking, harder cases are the cases when

- SMP and SMPB pulses do not swing fully (i.e., V_{high} is $V_{high} - \upsilon_{high}$ and V_{low} is $V_{low} + \upsilon_{low}$) and
- SPICE parameters of both pMOS and nMOS are the worst case.

On the other hand, easier cases are the cases when

- type of feeding is plus feeding,
- ΔV_{px} is positive, and
- SPCIE parameter of pMOS is the best case.

E. Sampling Methods

As described above, when a row of pixels is activated by the row driver circuit, common electrode voltage V_{com} of the row is raised or lowered, and according to V_{com}, pixel voltage V_{px} is also raised or lowered. In order to close V_{px} of a pixel to the video voltage level in advance of the video signal input for the pixel, the sampling method called *double sampling* is used sometimes, which opens sampling switch of a pixel before the video signal for the pixel is input. The normal sampling method is called *simple sampling*, which opens a sampling switch only during the video signal for the pixel is input. The timing charts of these sampling methods are shown in Fig.3.

In the figure, T denotes the time period during when the video signal keeps a voltage for a pixel, and in the case of simple sampling, only one sampling switch opens in each time period T. But, in the case of double sampling, two consecutive sampling switches open simultaneously. Namely, in the time frame when video signal keeps the voltage $VIDEO_i$ for the *i*-th pixel, not only the sampling switch for the *i*-th pixel but also that for the (*i*+1)-th pixel open. We consider these two methods.

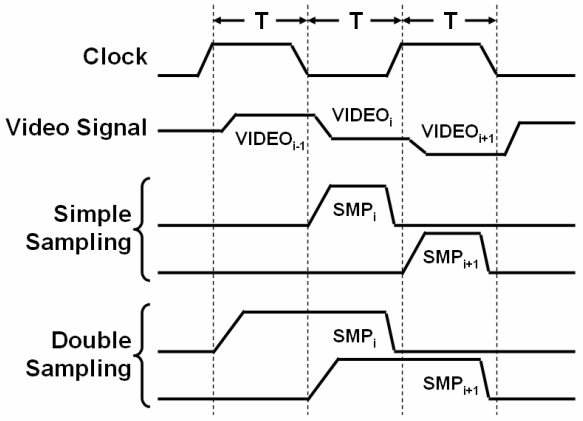

Fig. 3: Timing charts of simple and double samplings

III. DESIGN PROCEDURE

Now, let us describe the proposed design procedure for sampling switch and sampling pulse.

Considering that the longer is the opening period of sampling switch, the shorter we can make widths W_n and W_p, and hence it is better to set the width of the sampling pulse as long as possible, because shortening W_n and W_p contribute to the area and power minimization. Rising time t_r and falling time t_f of pulses SMP and SMPB are regulated by the buffer in the delay-buffer circuit, whereas the nominal length of intermediate time t_w is determined by the delay in the delay-buffer circuit. Hence, we determine t_w by the following equations, which make the pulse width $t_r + t_w + t_f$ of SMP as long as possible.

<The case of simple sampling>

$$(1+\varepsilon_r)\cdot t_r + (1+\varepsilon_w)\cdot t_w + (1+\varepsilon_f)\cdot t_f = T\cdot(1-\varepsilon_T) \quad (1)$$

<The case of double sampling>

$$(1+\varepsilon_r)\cdot t_r + (1+\varepsilon_w)\cdot t_w + (1+\varepsilon_f)\cdot t_f = 2T\cdot(1-\varepsilon_T) \quad (2)$$

With the use of these equations, the basic design parameters W_n, W_p, t_r, t_f, and t_w for sampling switch and sampling pulse are now reduced to t_r, t_f, and W_n. So, our task is to find an optimal 3-tuple (t_r, t_f, W_n) satisfying the constraints on RPV. In order to devise an algorithm to seek an optimal 3-tuple, we first consider the ranges of t_r and t_f.

Let $t_{r\text{-}min}$ and $t_{f\text{-}min}$ denote the minimum of t_r and t_f, respectively, which can be determined by the pulses generated by TFTs with the maximal values of W_n and W_p, respectively. Such maximum values of W_n and W_p are usually given by designers or determined from the width of a column of pixel.

As for the upper bounds of t_r and t_f, we consider the following two conditions:

(i) The sampling switch must turn off between the instance when SMP pulse falls to the bottom and the instance when the video signal begins to show the voltage of the next pixel. Let t_{ph} be the time interval between these instances.

(ii) $t_r + t_f$ should not exceed T, since otherwise SMP pulse can not fully swing in the case of simple sampling, and all nMOSs and pMOSs in two consecutive sampling switches turn on in the case of double sampling.

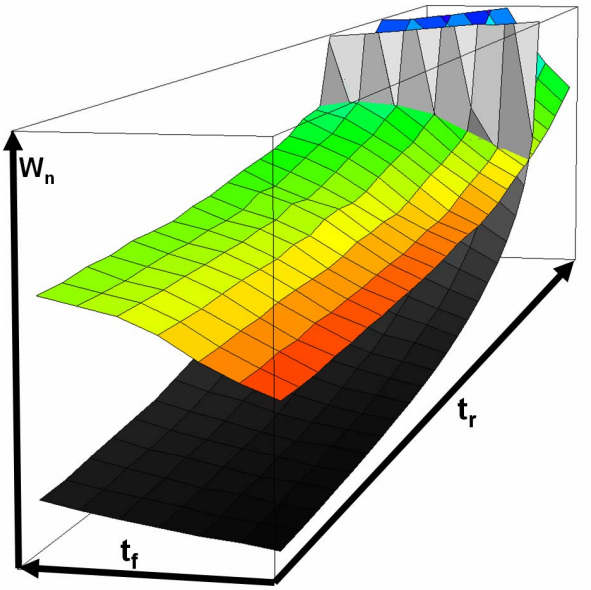

Fig. 4: Typical values of $W_{n\text{-}min}$ and $W_{n\text{-}max}$

From condition (i), we have an inequality such that a half of t_f is less than t_{ph}, and from this inequality we have

$$t_{f\text{-}min}/(1-\varepsilon_f) < t_f < 2\cdot t_{ph}/(1+\varepsilon_f) \quad (3)$$

From condition (ii), we have the following inequalities.

$$t_{r\text{-}min}/(1-\varepsilon_r) < t_r < \{\, T\cdot(1-\varepsilon_r) - t_f\cdot(1+\varepsilon_f)\,\}/(1+\varepsilon_r) \quad (4)$$

Since shorter W_n is better in area and power of the sampling switch, W_n of an optimal 3-tuple (t_r, t_f, W_n) must be minimal. On the other hand, longer t_r and t_f make transistor widths in the buffer circuit smaller, and hence t_r and t_f must be maximal. However, shorter W_n requires longer t_w in order to satisfy the constraints on RPV, and hence by equation (1) or (2), t_r and t_f become shorter. Therefore, there exists a trade-off among t_r, t_f, and W_n.

In order to resolve this trade-off, we must define the optimality of 3-tuple (t_r, t_f, W_n) precisely by considering whole column driver circuit. But if we do so, the number of design parameters becomes too large. So, we focus only on the sampling switch and sampling pulse, and consider a heuristic algorithm to find an optimal 3-tuple (t_r, t_f, W_n). In the following, we will explain such an algorithm which treats W_n as a constraint, and t_r and t_f as objective functions.

Once values of t_r, t_w, and t_f are determined, it is not difficult to find the minimum value $W_{n\text{-}min}$ and the maximum value $W_{n\text{-}max}$ of W_n with the use of SPICE simulation and the binary search, where $W_{n\text{-}min}$ is the minimum width of W_n among all harder cases of feeding video voltage into a pixel which makes RPV equal to 100–B[%], and $W_{n\text{-}max}$ is the maximum width of W_n among all easier cases of feeding which makes RPV equal to 100+B[%]. Typical values of $W_{n\text{-}min}$ and $W_{n\text{-}max}$ are shown in Fig.4. In the figure, the upper and lower surfaces at the left hand side indicate the values of (t_r, t_f, $W_{n\text{-}max}$) and (t_r, t_f, $W_{n\text{-}min}$), respectively, and the space between these two surfaces corresponds to (t_r, t_f, W_n) for which RPV satisfies the constraint. An optimum 3-tuple (t_r, t_f, W_n) exists in this space.

Since the width W_n fluctuates $\pm\sigma_n$, the optimal value of W_n must satisfy $W_{n\text{-}max} - W_{n\text{-}min} > 2\sigma_n$. Moreover, since $W_p = a\cdot W_n + b$ also fluctuates $\pm\sigma_p$, W_n must satisfy $W_{n\text{-}max} - W_{n\text{-}min} > 2\sigma_p/a$. Hence, we determine an optimal W_n by the following equations.

$$W_n = (W_{n\text{-}max} + W_{n\text{-}min})/2 \quad (5)$$

$$W_{n\text{-}max} - W_{n\text{-}min} = \max[\, 2\sigma_n,\ 2\sigma_p/a\,] \quad (6)$$

In order to determine optimal values of t_r and t_f, we check the variation of t_r with respect to t_f, because the range of t_f is much smaller than that of t_r. Then, we select pair (t_r, t_f) such that

- t_r is maximal and
- $W_{n\text{-}max}$ and $W_{n\text{-}min}$ obtained for (t_r, t_f) satisfy (6).

According to the results of pre-experiments, t_r has a unique maximal value for the possible values of t_f, and hence we can find the maximal value of t_r by a method similar to the binary search. A brief description of the overall design procedure is as follows.

Step 1: For the video voltage which makes the transmitted luminance of a pixel change most steeply, seek constants a and b of relation $W_p = a\cdot W_n + b$ which reduces pixel voltage change ΔV_{px} due to

the charge injection to 0.

Step 2: By using the following operations with respect to t_f, find a pair (t_r, t_f) such that t_r is maximal. As mentioned above, t_r has a unique maximal value, and hence we use a kind of binary search to find a maximal value.

2.1 Set $t_{f\text{-}L}$ = the lower bound of t_f, and $t_{f\text{-}U}$ = the upper bound of t_f.

2.2 While $t_{f\text{-}U} - t_{f\text{-}L}$ is not small enough, conduct the following operations for $t_f = (t_{f\text{-}U} + t_{f\text{-}L})/2$, and find a 3-tuple ($t_r$, t_f, W_n).

2.2.1 Set $t_{r\text{-}L}$ = the lower bound of t_r, and $t_{r\text{-}U}$ = the upper bound of t_r.

2.2.2 While $t_{r\text{-}U} - t_{r\text{-}L}$ is not small enough, conduct the following operations for $t_r = (t_{r\text{-}U} + t_{r\text{-}L})/2$, and find W_n satisfying (5) and (6).

- For pair (t_r, t_f), compute t_w by using (1) or (2).
- For (t_r, t_w, t_f), calculate the maximum value $W_{n\text{-}max}$ of W_n which makes RPV equal to 100+B[%] with the use of easier cases.
- For (t_r, t_w, t_f), calculate the minimum value $W_{n\text{-}min}$ of W_n which makes RPV equal to 100–B[%] with the use of harder cases.

2.2.3 Replace $t_{r\text{-}L}$ or $t_{r\text{-}U}$ by t_r so that W_n satisfying (5) exists in between $t_{r\text{-}L}$ and $t_{r\text{-}U}$.

2.3 Replace $t_{f\text{-}L}$ or $t_{f\text{-}U}$ by t_f so that maximal t_r exists in between $t_{f\text{-}L}$ and $t_{f\text{-}U}$.

Step 3: From 3-tuple (t_r, t_f, W_n) obtained in Step 2, calculate 5-tuple (t_r, t_w, t_f, W_p, W_n) which determines the sizes of sampling switch and the waveform of SMP pulse.

IV. Experimental Results

We have applied the proposed procedure to a sampling switch of the column driver which has been designed in manual already. Since the double sampling was used in the manual design, we used equation (2) in the procedure. Fig.4 shows the values of (t_r, t_f, $W_{n\text{-}max}$) and (t_r, t_f, $W_{n\text{-}min}$) for this sampling switch as described in the previous section. Our procedure does not enumerate all these values, but seeks an optimal 3-tuple (t_r, t_f, W_n) which belongs to the space between the two surfaces in Fig.4.

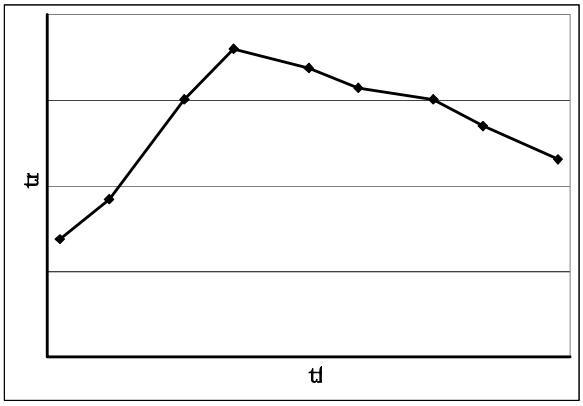

Fig. 5: A variation of t_r with respect to t_f

A typical variation of t_r with respect to t_f is shown in Fig.5, from which we can see that there exists a unique t_f at which t_r becomes maximal. Note here that for this pair (t_r, t_f), the waveform of SMP pulse such that the rising time is t_r, the falling time is t_f, and the intermediate time t_w satisfying (2) is obtained, and for this SMP pulse, the maximum value $W_{n\text{-}max}$ and the minimum value $W_{n\text{-}min}$ of W_n satisfying equation (6) are obtained. Hence, with the use of these $W_{n\text{-}max}$ and $W_{n\text{-}min}$, we can calculate W_n by equation (5) and W_p by $W_p = a \cdot W_n + b$, which determine the size of the sampling switch. The CPU time to find an optimal design parameters (t_r, t_w, t_f, W_p, W_n) was about 30 minutes by SunBlade 2000 and Smart SPICE[5].

The values of W_n and W_p obtained by our procedure have been reduced by 62% and 47%, respectively, in comparison with those obtained by manual design. Moreover, t_r has been increased by 50%. As a result, the constraints imposed on the sampling pulse generation can be lightened such that the power consumption of the column driver can be reduced by 46% through 54%.

In order to see the robustness of the column driver designed by using our procedure, we evaluated RPVs for 270 combinations of the type of the feeding of video voltage into pixel, the fluctuation of supply voltages, and the fluctuation of sampling transistors, where the combinations are selected from 2 feedings (plus and minus), 3 fluctuations (high, typical, and low) of V_{ss}, V_{dd} and system clock voltage, and 5 fluctuations (nBpB, nTpT, nWpW, nBpW, nWpB) of SPICE parameters of nMOS and pMOS of the sampling switch. The histograms of RPVs obtained by our design procedure and by manual design are shown in Fig. 6, where it can be seen that most of the objectives set up for RPVs have been achieved. It should also be pointed out that in manual design there occur the cases in which the constraints for RPV are not satisfied due to the lack in the insufficient treatment of charge injection.

V. Conclusions

In this paper, we proposed a practical design procedure dedicatedly for the sampling switch of active matrix LCDs, which satisfies the required constraint for RPV, the Ratio of Pixel voltage to Video voltage. To do this, we first analyzed how the design parameters of sampling switch and sampling pulse are related to the RPV, and then sought a minimal number of parameters which contribute most to the behavior of RPV. With the use of these parameters, we can truncate the solution space of design parameters to be explored, so that we can reduce the number of SPICE simulations.

Experimental results show that an optimal sampling switch attained by this procedure gives rise to a column driver with almost 50% less power consumption than the one by manual design. The time needed to obtain an optimal solution was around 30 minutes. Hence, the proposed design procedure provides a very powerful tool which contributes greatly to the design automation of column drivers. Development is continuing on constructing a full set of design tools for

column drivers.

Devising a procedure to design the sampling switch and the delay-buffer circuit simultaneously is a remaining future work.

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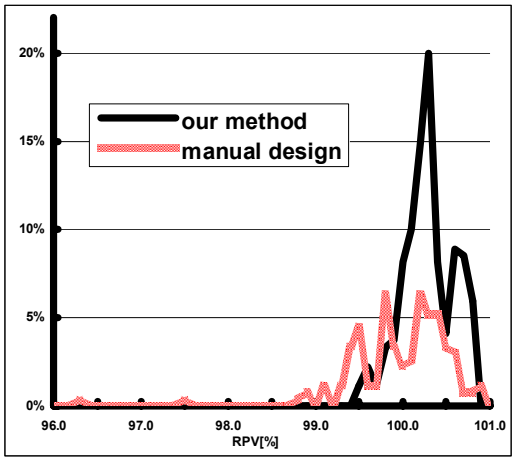

Fig. 6: Histogram of RPVs