Interconnect RL Extraction at a Single Representative Frequency

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Abstract— This paper proposes a method to determine a single frequency for interconnect RL extraction. Resistance and inductance of interconnects depend on frequency, and hence the extraction frequency strongly affects the modeling accuracy of interconnects. The proposed method determines an extraction frequency based on the transfer characteristic of interconnects. By choosing the frequency where the transfer characteristic becomes maximum, the extracted RL values achieve the accurate modeling of the waveform. We experimentally verify that the proposed method provides accurate transition waveforms over various interconnect topologies.

I. Introduction

According to advancements in LSI fabrication technology, performance of LSI chips is predicted to improve continuously [1]. As improving the chip performance, on-chip interconnects become important and accurate modeling of interconnects is crucial for circuit design. One difficulty of interconnect modeling is frequency dependency of the characteristics. Resistance and inductance depend on frequency because of skin- and proximity-effect [2]. In digital circuits, pulse waveforms are commonly used. The frequency spectrum of pulse waveforms widely spreads from DC to frequency several times as high as clock frequency. Therefore to model the behavior of interconnects precisely, designers have to take the frequency characteristics into consideration. To treat frequency dependent interconnects, several modeling methods are proposed [3–5]. These frequency-dependent models improve simulation accuracy. However, in circuit design, the conventional frequency-independent model has an advantage that there are a number of techniques and methods developed so far. Inductance-aware circuit design techniques, such as analytical performance estimation, circuit reduction, buffer insertion and timing analysis, have been widely studied [2, 6–8]. Most of these techniques assume that interconnects can be modeled as a frequency-independent RLC ladder circuit. However, how to cope with frequency-dependency in modeling interconnects as a RLC ladder has not been studied enough, though its modeling accuracy affects design quality. Therefore developing an accurate modeling technique by frquency-independent model is indispensable for designing high-performance circuits, and hence we focus on RL extraction at a single frequency in this work.

In this paper, the extraction frequency based on the transfer characteristic of interconnects is proposed. It is commonly adopted to determine the extraction frequency from the shape of an input signal waveform, especially from the rise time, focusing on the spectrum of the input signal [2]. This is natural and reasonable when we analyze the incident waveform to the near-end (driver output) of the interconnects. On the other hand, our main interest is the analysis of the waveform at the far-end (receiver input). As signals are propagating through an interconnect, high-frequency components easily attenuate. The dominant frequency components that determine the far-end waveform are different from those for the near-end waveform. We observe that the transfer characteristic of interconnects is playing an important role in the waveforms at the far-end of interconnects. Therefore we focus on the transfer characteristic of interconnects and select the frequency where the transfer characteristic becomes maximum as the frequency to use for interconnect RL extraction. A preliminary work is presented in Ref. [9], however, the frequency determination method in Ref. [9] is not practical because it can treat only open-ended uniform transmission-lines without branches. If the interconnect is branching or nonuniform, the transfer characteristic of each segment is different. The proposed method in this paper gives a respective extraction frequency to every segment of an interconnect instead of enforcing a single extraction frequency on the entire interconnect. The proposed method systematically determines the extraction frequencies successively from the sinks to the source by replacing the downstream interconnect with the equivalent load impedance. We experimentally verify that the equivalent circuit of interconnects extracted at the proposed frequency can achieve the most accurate waveform modeling compared with the conventional extraction frequencies. Experimental results show the maximum errors are below 10% in signal delay and signal transition time. The contribution of this paper is that our method realizes accurate transient analysis using frequency-independent interconnect model. The proposed method is effective when the topology and the length of interconnects are fixed, for example, post-layout extraction.

In Section II, the problems in interconnect modeling are described. Section III explains the detail of the proposed method. We then show experimental results in Section IV. Section V concludes the discussion.

II. Problem description

This section describes the problem discussed in this paper. We first show frequency-dependence of interconnect characteristics and demonstrate its impact on transient analysis.

A. Frequency-dependence of interconnect characteristics

Frequency-dependence of interconnect characteristics is mainly caused by skin-effect and proximity effect. The characteristics variation is strongly related with the interconnect structure as well as the frequency. Skin- and proximity-effects are remarkable on wide and thick interconnects because skin

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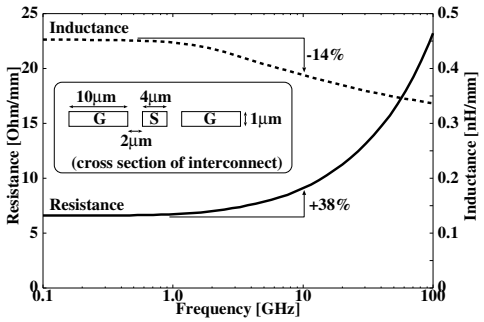

Fig. 1. Frequency-dependence of resistance and inductance. (co-planar structure, signal line width 4μm, ground line width 10μm, spacing 2μm)

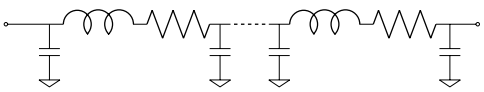

Fig. 2. RLC ladder circuit model.

depth becomes comparable to the interconnect size in relatively lower frequency.

Figure 1 shows an example of resistance and inductance characteristics. The resistance and inductance values are calculated by a field-solver [10]. The assumed interconnect structure is co-planar, and the width of the signal line is 4μm, the width of the ground line is 10μm and their spacing is 2μm. In this case, the resistance increases by 38% from DC to 10GHz, and the inductance decreases by 14% from DC to 10GHz. The resistance and the inductance start changing at relatively low frequency of 1 to 2GHz, and thus frequency-dependence is not negligible to model interconnects in current high-performance circuits any longer.

B. Conventional extraction frequencies

In digital circuits, a trapezoidal pulse that contains multiple frequency components is a common waveform. To model long interconnects that have transmission-line characteristics, an RLC ladder circuit as Fig. 2 is used. This ladder model cannot consider the frequency-dependence of interconnect RL values. In order to derive frequency-independent model of Fig. 2, we have to choose a single extraction frequency.

There are several representative frequencies of periodic pulse waveform. One of them is significant frequency [2]. The significant frequency f_{sig} is expressed by signal transition time t_{r} and defined such that the signal energy from DC to f_{sig} becomes 85% of all signal energy. In the range $7 \leq T_{\text{w}}/t_{\text{r}} \leq 13$ where T_{w} is the pulse width, f_{sig} is given by $0.34/t_{\text{r}}$ [2]. On the other hand, DC is often used for extraction. Reference [11] concludes that the extraction at DC is accurate enough to estimate signal delay and overshoot/undershoot. DC extraction is acceptable when frequency-dependence is weak, e.g. for narrow interconnects or in low frequency. However as shown in the next section, interconnect modeling at these frequencies causes error in evaluating the propagation waveform.

C. Interconnect models and their impact on waveform

Generally, interconnects in VLSIs are expressed by lumped RLC for circuit design. As explained in the previous section, the frequency-independent RLC ladder circuit in Fig. 2 is used to model on-chip interconnects. A number of frequency-dependent models are proposed [3–5]. In this paper, we use the model of Ref. [5] as a golden frequency-dependent model. It is implemented in HSPICE [12] as w-element model. Although frequency-dependent models such as Ref. [5] can provide accurate waveforms, the frequency-dependent model does not tell the designers which frequency component is important in circuit design. Conversely, if we know which frequency component dominantly forms and affects the waveforms at the far-end, we do not necessarily have to use the frequency-dependent model, and we can use many design methods and techniques based on conventional frequency-independent model extracted at the dominant frequency. However the frequency spectrum spreads widely and depends on circuit behavior and interconnect characteristics, and hence it is difficult to specify the most representative frequency from the frequency spectrum. The goal of this research is to determine the representative frequency for modeling interconnects at a single frequency.

Figure 3 shows the impact of frequency-dependence on transient analysis. The simulated circuit is shown in Fig. 3. The interconnect shown in Fig. 1 is driven by a voltage source and a resistor R_{d} that correspond to a CMOS driver whose output impedance is 150Ω. The solid line labeled "FD" shows the voltage waveform at the far-end by the frequency-dependent model. In this paper, we use "FD" as the abbreviation of "Frequency-Dependent model". The dashed lines labeled "DC" and "f_{sig}" are the results of frequency-independent models shown in Fig. 2. "DC" means the RLC ladder model extracted at DC, and "f_{sig}" corresponds to RLC extraction at the significant frequency. The number of ladder is 51. As you see, both waveforms of the conventional frequency-independent models ("DC" and "f_{sig}") are far from that of frequency-dependent model ("FD"). In the signal propagation delay time and the signal transition time (from 0.2V to 0.8V), the errors of "DC" are -28% in delay and -13% in transition time. The errors of "f_{sig}" are 19% in delay and 10% in transition time. When R and L are extracted at DC, the extracted resistance is too low, and, the resistance extracted at significant frequency is too high. From the above observations, we can expect that a certain frequency between DC and significant frequency provides the waveform that is close to the waveform of the frequency-dependent model. If the representative frequency can be determined systematically, we can model interconnects by a single frequency. In the following section, we discuss the way to determine the representative frequency to model interconnects at a single frequency.

III. A Method to determine an extraction frequency

In this section, we propose a method to determine the representative frequency for interconnect RL extraction. The pro-

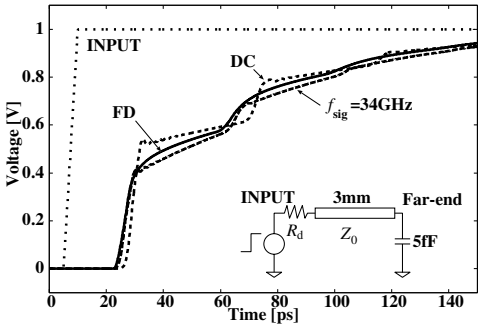

Fig. 3. The impact of frequency-dependence on transition waveform. (interconnect structure is shown in Figure 1, $R_{\rm d} = 150\Omega$)

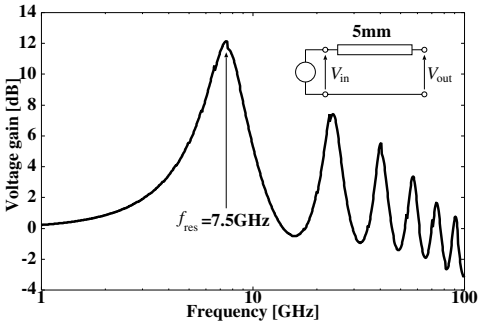

Fig. 5. transfer characteristic of a transmission-line with 5mm long.

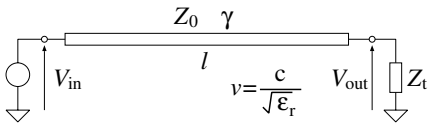

Fig. 4. Transmission-line with impedance load.

posed method determines the extraction frequency focusing on the transfer characteristic of interconnects. We first explain the transfer characteristic of transmission-lines. We then show the detail of the proposed method.

A. Transfer characteristic of transmission-lines

The basic idea of our method is to choose the frequency where the transfer characteristic becomes maximum. We here explain the nature of the transfer characteristic of interconnects based on the transmission-line theory. We here discuss a simple transmission-line as shown in Fig. 4. The characteristic impedance is Z_0, the propagation constant is γ, the length of the transmission-line is l and the velocity of electromagnetic wave is v. The velocity v is equal to $c/\sqrt{\varepsilon_{\rm r}}$, where c is the velocity of light in vacuum and $\varepsilon_{\rm r}$ is the relative dielectric constant of insulator. The load impedance $Z_{\rm t}$ is connected to the far-end of transmission-lines. We write the voltage at the near-end as $V_{\rm in}$ and the voltage at the far-end as $V_{\rm out}$.

According to the transmission-line theory, the voltage transfer characteristic $V_{\rm out}/V_{\rm in}$ is expressed as

$$\frac{V_{\rm out}}{V_{\rm in}} = \frac{1}{\cosh\gamma l + \frac{Z_0}{Z_{\rm t}}\sinh\gamma l}. \qquad (1)$$

Figure 5 shows an example of the transfer characteristic of an open-ended transmission-line. We use the transmission-line shown in Fig. 1 and the relative dielectric constant $\varepsilon_{\rm r}$ is 4. We extract the frequency characteristics by a 2D field solver and model the interconnect by the frequency-dependent model [5]. When the transmission-line is open-ended, the transfer characteristic $V_{\rm out}/V_{\rm in}$ becomes maximum where the quarter wavelength $\lambda/4$ is equal to the line length l. This nature is used for quarter wavelength transmission-line resonators. In this case, the resonance frequency $f_{\rm res}$ where $V_{\rm out}/V_{\rm in}$ becomes maximum is $v/4l = 1.5\times10^8/(4\times5\times10^{-3}) = 7.5$GHz.

This transfer characteristic affects the waveform at the far-end of transmission-lines. The frequency components near the resonance frequency tend to appear at the far-end. On the other hand, the frequency components near the antiresonance frequency hardly affect the waveform at the far-end. Therefore the frequency spectrum at the far-end depends on the input pulse and the transfer characteristic of the interconnect. If the frequency spectrum of the input pulse spreads over the resonance frequency, the frequency components around the resonance frequency are expected to affect the waveform at the far-end. If the resonance frequency is higher than the significant frequency, the frequency components around the resonance frequency are small because almost all of the frequency components concentrate in the range from DC to the significant frequency.

Figure 6 shows the frequency spectrum of the waveform at the far-end in the case that trapezoidal pulses with various transition time $t_{\rm r}$ are injected to the near-end of the interconnect shown in Fig. 5. The transition time $t_{\rm r}$ is varied from 10ps to 50ps, and hence the significant frequency changes from 34GHz to 6.8GHz. The resonance frequency is 7.5GHz. In this case, the significant frequency is nearly equal to or higher than the resonance frequency. The frequency spectrum has is a unique peak at the resonance frequency even if the signal transition time $t_{\rm r}$ is changed. This result indicates the frequency component at the resonance frequency is an important factor which determines the waveform at the far-end of the interconnect. Reference [9] reports that the resonance frequency is suitable for the extraction frequency of open-ended uniform transmission-lines without branches. However, on-chip interconnects is not uniform and have branches. If the interconnect is branching, the transfer characteristic from the driver to one receiver is not the same as that from the driver to the other receiver. Therefore we cannot apply the method in Ref. [9] to branching wire directly.

B. Flow of the proposed method

This section proposes a method to determine the extraction frequency based on the transfer characteristic. We explain the flow of the proposed method. Figure 7 is the conceptual diagram of the proposed method. We divide an interconnect into segments at the branch points or discontinuous points and consider as a tree such that the root node is the output of the driver

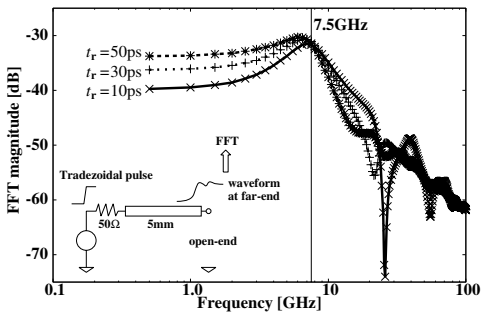

Fig. 6. Frequency spectrum of waveform at the far-end.

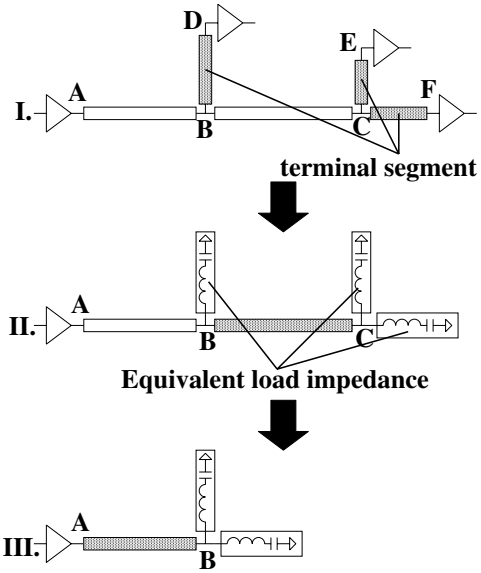

Fig. 7. Conceptual diagram of the proposed method.

and the input of the receiver is the leaf node. The proposed method determines the extraction frequencies for each segment from leaf to root by replacing the downstream branches with the equivalent load impedances.

Assumptions of the proposed method

The proposed method determines the extraction frequency from the topology of interconnects and the length of each segment. We assume that the velocity of electromagnetic wave v is known and a constant value. In LSIs, this assumption is valid because the velocity v depends on the relative dielectric constant ε_{r} and it is constant in the same fabrication process. We also assume that the significant frequency f_{sig} is known. As described in following step, we use the significant frequency as the upper limit of the extraction frequency. Additionally, we assume that the characteristic impedances of each segment are the same. Strictly speaking, this assumption is not correct. However in LSIs, the characteristic impedance of on-chip interconnects does not vary drastically even if the interconnect structure changes. The typical value of co-planar structures is from 50Ω to 100Ω. In the following section, we experimentally verify that these assumptions are reasonable.

Step 1. Determine the extraction frequency for terminal segments

If the length of the segment and the load impedance are known, the frequency f_{res} at which the transfer characteristic of the segment becomes maximum can be determined from Eq.(1). The resonance frequency f_{res} depends on the length of the segment and the load impedance. Generally, as short the segment is, the extraction frequency becomes higher. The frequency f_{res} can be too high frequency to use as an extraction frequency. If the frequency component of the input is too small at the frequency, extracting at the frequency at which the transfer characteristic becomes maximum is meaningless. We therefore set the upper limit of the extraction frequency. As mentioned so far, the significant frequency f_{sig} is defined as the frequency that the 85% of all the energy is included from DC to f_{sig}. In the case that the resonance frequency is higher than significant frequency, the frequency components around the resonance frequency are small and hardly affect the waveform at the far-end. Therefore it is reasonable to use the significant frequency as the upper limit of the extraction frequency. Extraction frequency f_{proposed} is expressed as

$$f_{\mathrm{proposed}} = \min\left(f_{\mathrm{res}}, f_{\mathrm{sig}}\right). \tag{2}$$

Reference [9] reports the case of open-ended uniform transmission-lines. In CMOS circuits, the input capacitance of the gates is small and we can assume the segments connected to the receiver are open-ended transmission-line. The extraction frequencies of these open-ended branches are the frequency where the quarter wavelength is equal to the interconnect length. When the length of a segment is l, the resonance frequency f_{res} is $v/4l$. We cannot apply the method in Ref. [9] to interconnects which have a large capacitive load or a resistive termination because Ref. [9] assumes open-ended transmission-lines. By using Eq. (1), the proposed method can be applied to the interconnects that we cannot be regarded as open-ended transmission-lines.

Step 2. Replacing terminal segments with equivalent load impedances

At step 1, the extraction frequencies of terminal segments are decided. To decide the extraction frequencies of the preceding segments, we replace the segments whose extraction frequency is already decided with equivalent load impedances. This step corresponds to Fig. 7. II. By replacing with the equivalent load impedance, we can calculate the extraction frequency by Eq. (1). For example, in Fig. 7, we can calculate the extraction frequency for the segment B-C by replacing the segment C-E and C-F with the equivalent load impedances.

The load impedance of a certain segment is the input impedance of the downstream branches. For example, the load impedance of the segment B-C in Fig. 7 is the input impedance of the segment C-E and the segment C-F. As shown in Fig 7. II, the input impedance of transmission-lines can be modeled by a RLC series resonator circuit whose resonance frequency is equal to f_{res}. We can ignore the resistance because the proposed method needs only the resonance frequency. The input

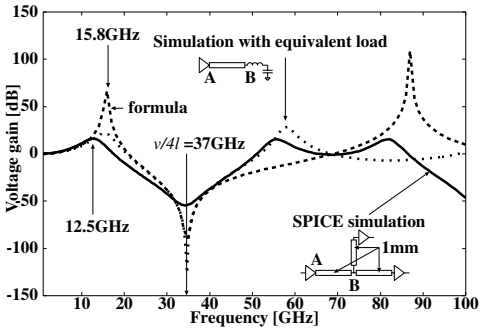

Fig. 8. Voltage gain estimated by the equivalent load impedance.

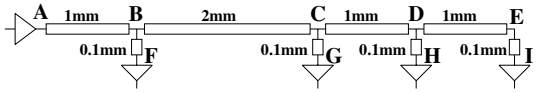

Fig. 9. Stub-bus topology.

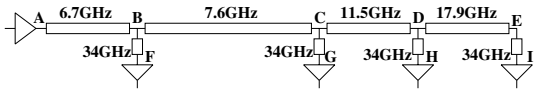

Fig. 10. Extraction frequencies by the proposed method.

impedance of a certain segment is expressed as

$$Z_{\text{in}} = \sqrt{\frac{L}{C}}\frac{1-\omega^2 LC}{\mathrm{j}\omega\sqrt{LC}} \simeq \frac{Z_0}{\mathrm{j}\tan\left(\frac{\omega l'}{v}\right)} \tag{3}$$

where l' is equivalent length defined as $v/4f_{\text{res}}$. We assume that the characteristic impedances Z_0 of each segment are the same. Therefore the value of the inductance L and the capacitance C are determined from the characteristic impedance Z_0 and the resonance frequency f_{res}. This means that once the resonance frequency f_{res} is calculated, the equivalent load impedance is uniquely determined.

Figure 8 shows an example of transfer characteristic estimated by Eq. (1) and the equivalent load impedance defined by Eq. (3). Figure 8 is the voltage gain between node A and node B. The interconnect topology is a branching wire as shown in Fig. 8. The solid line is the transfer characteristic by SPICE AC analysis. The dashed line labeled "Simulation with equivalent load" is the result of SPICE simulation using the equivalent load, and the dashed line labeled "formula" is that by Eq. (1) with the equivalent load impedance. The resonance frequency f_{open} when we assume the segment A-B as open-ended is 37.5GHz. As shown in Fig. 8, the transfer characteristic estimated by Eq. (1) with equivalent load impedance is valid to estimate the peak of the transfer characteristic. On the other hand, the frequency f_{open} becomes antiresonance frequency on the segment A-B and the transfer characteristic at f_{open} becomes minimum. This result shows that we have to consider the load impedance to estimate the first peak frequencies of the transfer characteristic. From the above discussion, the transfer characteristic can be estimated by Eq. (1) with equivalent load impedance by Eq. (3).

By replacing the terminal segments with equivalent load impedance, the terminal segments are eliminated and other segments become terminal segments. We can return to step 1 and determine the extraction frequency for new terminal segments. The proposed method determines extraction frequencies for each segment by iterating the step 1 and step 2.

IV. Experimental Results

This section demonstrates experimental results. We show the experimental results of a major interconnect topology, stub-bus. We then show statistics of experimental results in various situations.

A. Stub-Bus topology

We show the experimental result of stub-bus structure. Figure 9 shows the interconnect topology. The bus line A-B-C-D-E is a fat wire that the signal width $W_{\text{s}} = 10\mu$m, the ground width $W_{\text{g}} = 10\mu$m and the spacing $S = 2\mu$m. The stubs are short and thin wires, that $W_{\text{s}} = 1\mu$m, $W_{\text{g}} = 1\mu$m and $S = 2\mu$m. The driver output impedance is 50Ω and the transition time of input is 10ps.

We here show the frequency determination process step by step. First, the stubs (B-F, C-G, D-H and E-I) are the terminal segment. The resonance frequency of the stubs is 375GHz from the length. The resonance frequency is higher than the significant frequency, 34GHz. Therefore the extraction frequency of stubs is determined to 34GHz. Then we can replace the stubs by the equivalent load from Eq. (3). By replacing the stub E-I, the resonance frequency of the segment D-E is determined from Eq. (1). By iteration of step 1 and step 2, we can obtain the extraction frequency of each segment in the order of D-E, C-D, B-C, A-B. Finally the extraction frequencies by the proposed method are determined as shown in Fig. 10. Figure 11 shows the waveform at the node I and Table I shows the errors in delay and transition time. The ladder model extracted at DC or significant frequency causes serious error especially in signal transition time. As shown in Fig. 11, DC extraction underestimates the attenuation and f_{sig} overestimates. DC extraction also causes 8% error in delay because the extraction at DC causes estimation error in phase velocity. On the other hand, the RLC ladder by the proposed method provides accurate modeling of frequency-dependent interconnect.

B. Results of overall experiments

We evaluate our method under various conditions for verification. In this section, we show the statistical summary of all experiments. We vary the topology of net, lengths of each segment, interconnect structure, driver size and transition time of input. The number of segments in one net is varied from 1 to 5. The length of segment is 200μm–5mm. We use co-planar structure, whose signal width W_{s} and ground width are 1μm–10μm and the spacing S is 2μm–8μm. The output impedance of the driver is 25Ω–100Ω. The transition time of input pulse is 10ps–100ps. By changing those parameters, we evaluate 9,545

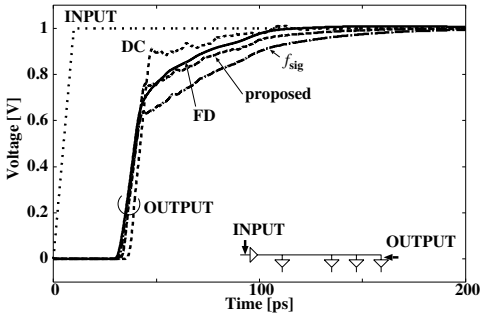

Fig. 11. Waveform at the node I of stub-bus.

TABLE I
ERRORS IN THE DELAY TIME AND THE TRANSITION TIME AT THE NODE I OF THE STUB-BUS.

Extraction Frequency	delay		transition time	
	[ps]	error [%]	[ps]	error [%]
FD	34.5	—	19.5	—
DC	37.3	8.1	6.8	-65.4
Proposed	35.3	2.3	21.2	8.7
f_{sig}	35.3	2.3	40.6	108.2

patterns of net and observe the waveforms at 43,199 nodes in total.

Table II shows the summary of overall experiments. Table II contains the maximum error in delay time and transition time (rows of "Max. error"), and the ratio of nodes where the error is over 5% (rows of "$> 5\%$"). The ladder extracted at DC tends to underestimate the delay and transition time, and the ladder extracted at significant frequency f_{sig} overestimates. In the case of the ladder extracted at DC, the error in delay exceeds 5% at the 12% of all nodes and the maximum error is -88.1%. In transition time, the error at 28% of nodes exceeds 5% and the maximum error is -71.9%. In the case of significant frequency, the error in delay at about 12% of all nodes is over 5% and the maximum is 110.0%, and the error in transition time at about 35% of all nodes is over 5% and the maximum is over 160%. Those errors are serious problem for evaluating the circuit behavior, such as timing analysis. On the other hand, the proposed method achieves the error less than 10% in both delay and transition time. The results above confirm the RLC ladder extracted at the proposed frequency provides accurate modeling of frequency-dependent interconnects.

V. CONCLUSION

The frequency that should be used to extract RL values is discussed. When we use frequency-independent equivalent circuits for circuit design, the extraction frequency must be carefully determined to maximize the fidelity in interconnect characteristics. We propose an RL extraction scheme that uses the frequency determined by interconnect length. We experimentally verify that the proposed frequency achieves the most accurate estimation in signal propagation delay and transition time. The maximum error is within 10% in delay and in transition time in our experiments. With the proposed representative frequency, RL extraction at a single frequency becomes accurate enough to model interconnect characteristics, and hence we can exploit many effective design and analysis techniques developed ignoring frequency-dependence.

TABLE II
STATISTICAL SUMMARY OF OVERALL EXPERIMENTS.

Extraction Frequency	delay		transition time	
	Max. error	$> 5\%^*$	Max. error	$> 5\%^*$
DC	-88.1 %	11.5 %	-71.9 %	27.8 %
proposed	-9.9 %	5.4 %	-9.8 %	12.5 %
f_{sig}	110.0 %	12.2 %	160.3 %	35.2 %

($*$: The ratio of the experiments that the error is over 5%.)

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