Si-substrate Modeling toward Substrate-aware Interconnect Resistance and Inductance Extraction in SoC Design

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Abstract

This paper proposes a simple yet sufficient Si-substrate modeling for interconnect resistance and inductance extraction. The proposed modeling expresses Si-substrate as four filaments in a filament-based extractor. Although the number of filaments is small, extracted loop inductances and resistances show accurate frequency dependence resulting from the proximity effect. We experimentally prove the accuracy using FEM (Finite Element Method) based simulations of electromagnetic fields. We also show a method to determine optimal size of the four filaments. The proposed model realizes substrate-aware extraction in SoC design flow.

1 Introduction

With advances in LSI fabrication technology, circuit operating frequency is predicted to increase continuously, and local clock frequency will be 15GHz at 45nm technology node[1]. Furthermore, even with the current generations of wafer process, recent trends of embedding radio-frequency/mixed-signal blocks in SoC[2] require local oscillator frequencies of over 10GHz. In such high speed LSIs, on-chip interconnect inductance gives impact on circuit design including timing[3]. At the same time, frequency dependence of interconnect inductance and resistance resulting from the substrate skin and proximity effects should be taken into account[4].

Figure 1 shows circuit simulation examples with and without frequency dependence of interconnect resistance due to the proximity effect on substrate loss. The simulated device under test (DUT) is the micro-strip line discussed in the next section, which is driven by inverters having 260(P-ch) and 130(N-ch) of W/L ratios. Resistivity of the substrate is set to 10mΩcm. The actual measured RLC values, shown in the next section, are set in the W-element table[5]. The input slew rate t_r is 20 psec./V_{dd}, whose significant frequency$f_s = 0.35/t_r$[6] is 18GHz. In this case, the 50% rising time at the far-end of DUT varies by around 30% due to the frequency dependence of the resistance value.

However, it is hard to extract such inductance and resistance and analyze a whole circuit. One reason for the difficulty is that Si-substrate with the skin and proximity effects are generally considered to require a large number of filaments in filament-based extractors commonly used for on-chip interconnects[7]. This paper shows that a much simpler model well reproduces the frequency dependence resulting from the substrate. The contribution of this work is to reveal that dividing Si-substrate into a small number of segments enables us to perform extraction with considering the proximity effect on the substrate.

In this paper, we first survey the actually measured frequency dependence of interconnect resistance and inductance with different substrate resistivities of 10Ωcm and 10mΩcm in order to see the proximity effect of substrate. Then, we introduce a new Si-substrate model for filament-based extractors and a method to determine optimal dimension of the filaments. We experimentally prove accuracy of the proposed model, adopting the FEM-based electromagnetic simulation as the reference.

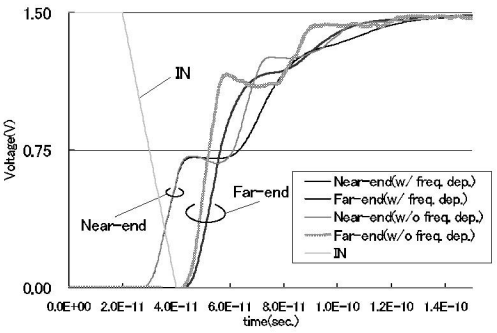

Figure 1: Influence of substrate loss.

2 Measured Frequency-dependence of Interconnect Resistance and Inductance

In order to observe interconnect characteristics resulting from the properties of Si-substrate, we have designed test element groups (TEG), which have been built in a 130nm CMOS technology. After examining the characteristic by measurement, we discuss an effective simulation model for substrate-aware extraction.

Figure 2 shows cross-sectional view of the TEG we studied, where a part of DUT is a micro-strip (MSL) line. As can be seen in the both sides of the figure, there are ground (GND) lines for DC return, whose DC resistances are negligibly small. Thus, in all TEGs, the loop DC resistance is almost determined by the resistance of a signal line. The GND lines for DC return are connected to the substrate by via arrays. There is no M1 ground plane even in the MSL configuration. Figure 3 shows each DUT layout pattern. Figures 4-7 show the frequency dependence of the interconnect resistance and inductance, converted from measured S-parameters. The frequency range is up to 20GHz. Regardless of the substrate resistivities, the micro-strip line has the same characteristic as the co-planer line with a far GND return. Similarly, the co-planer with a near GND return has the same tendency as the co-planer with near and far returns.

The largest difference between the two substrate resistivities is found in the ohmic loss above 5GHz (Figures 4 and 6). That is, on the low resistivity substrate of 10mΩcm, the micro-strip and the co-planer with a far GND return involve large ohmic loss above 5GHz. It is considered to originate in

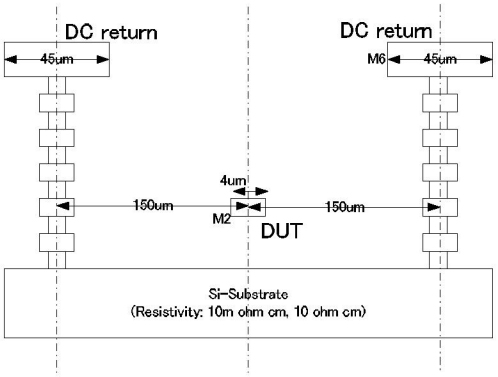

Figure 2: Cross-sectional view of TEG.

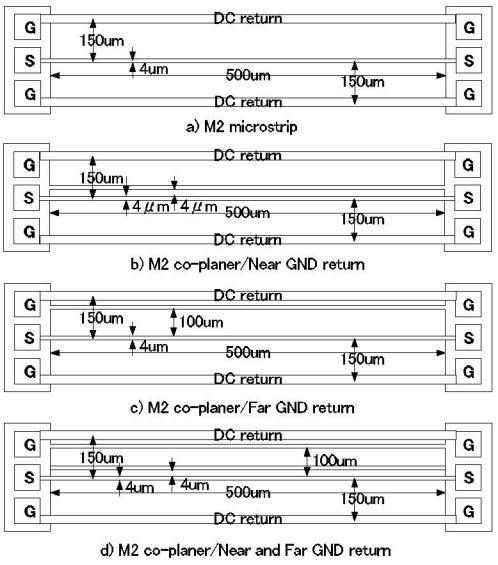

Figure 3: Layout pattern of DUT.

the proximity effect of the substrate. In the next section, we discuss an effective substrate modeling for the partial element equivalent circuit (PEEC) and the loop inductance and resistance extraction[9][10], that can consider the proximity effect observed in the measurement.

3 Si-substrate Modeling Approach

In the PEEC model, a Si-substrate is discretized into filaments[11]. The frequency dependence due to the skin and the proximity effects can be taken into account by forming multiple return paths (Fig. 8). The current flows to minimize the total impedance. At higher frequency, it crowds through the conductors that are closest together, and here the resistance increases but the inductance decreases. At low frequency, it spreads out to minimize the resistance. If the substrate is not discretized into multiple filaments, the major frequency dependence does not occur. Figure 9 shows that single filament substrate model does not reproduce the frequency dependence very well. At 10GHz, there appears 36% discrepancy from measured resistance as for 10mΩ cm substrate. The resistance increase observed in the simulation results at higher frequency comes from the skin and proximity effect of the signal line, not the

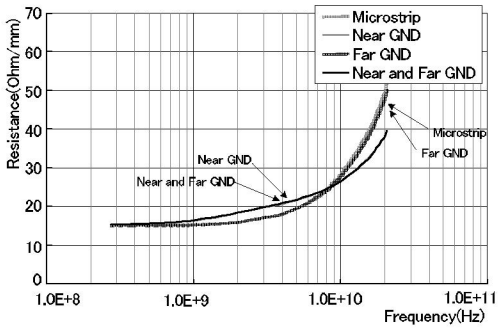

Figure 4: Measured resistances.(10mΩcm substrate)

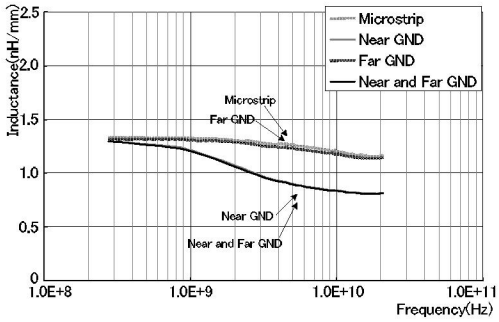

Figure 5: Measured inductances.(10mΩcm substrate)

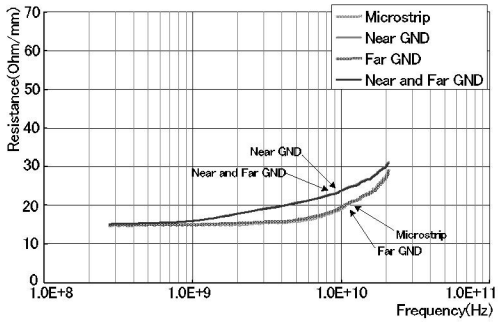

Figure 6: Measured resistances.(10Ωcm substrate)

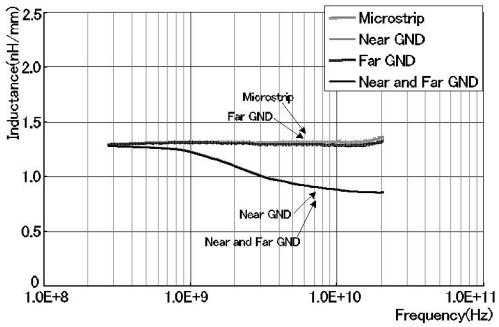

Figure 7: Measured inductances.(10Ωcm substrate)

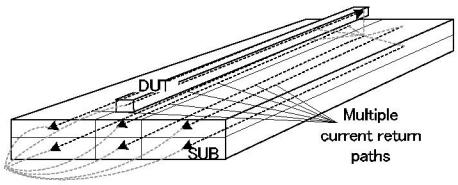

Figure 8: Multiple current return paths.

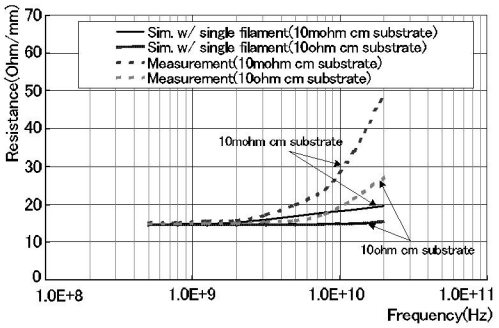

Figure 9: Resistance of MSL. (PEEC w/ single filament substrates)

substrate. It means that the major factor to the frequency dependences is the proximity effect of the substrate.

The general approach to model the substrate using PEEC is dividing the substrate into thousands of filaments, since the substrate has large volume[7]. However, current flow in the substrate, simulated by FEM, is highly concentrating near the signal at frequencies where resistance and inductance are changing due to the proximity effect (Fig. 10). We can hence expect that much fewer filaments reproduce the frequency dependence of resistance and inductance. We examined several number of substrate filaments as for the most remarkable case, that is the micro-strip line on the 10mΩcm substrate. We will show the relationship between the number of filaments and the corresponding extraction accuracy in the next section. Each set of substrate filaments is optimized along with the following steps. To simplify the explanations, let us assume six substrate filaments shown in Fig. 11 here.

Step.1: Set the size of the top middle filament, consist of $Hssc$ and $Wssc$ of $SF12$ in Fig. 11. The total height of the substrate (e.g. $400\mu m$) is determined by the fabrication. Here, the total width is set to the distance between the DC return lines.

Step.2: Calculate root mean square (RMS) error between resistances and inductances computed by the filament-based extraction and a reference field solver, over the target range of frequencies.

Step.3: Change the size of the top middle filament. Calculate RMS as same as Step.2.

Step.4: Repeat Step.3, and adopt a size of the top middle filament, which provides the minimum RMS error.

When there are more than six filaments, the procedure is the same though the number of variables increases. In the next section, we discuss the detailed experimental results and validness of this flow.

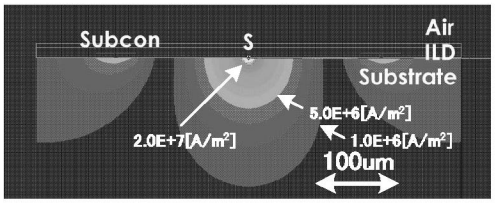

Figure 10: Current distribution in 10mΩcm substrate of MSL at 10GHz, simulated by FEM.

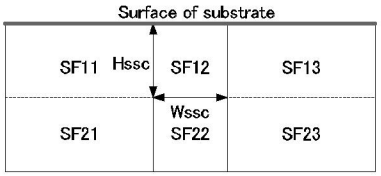

Figure 11: Cross-section of six filaments substrate.

4 Experimental Results

To discuss the correctness of the proposed method with referring to current distribution in the substrate, we use a FEM filed solver, Maxwell[12] as the reference. The resistances and inductances simulated by FEM have been correlated with the measured values within root-mean-square (RMS) error of 8.3% and 12.9% in the measured frequency range of 50MHz-20GHz, respectively. On the other hand, we use Raphael[8] RI3-mode as a filament-based extractor. Partial inductances and resistances are converted to the loop inductances and resistances inside Raphael. Since MSL on 10mΩcm substrate involves the most remarkable frequency dependence, we show only the results from MSL on 10mΩcm substrate although evaluation was performed also to other structures.

In order to clarify the number of filaments required to consider the substrate effect, we examined several number of substrate filaments as for the most remarkable case, that is the micro-strip line on the 10mΩcm substrate.

Figure 12 shows the relationship between computing time on Enterprise[TM] 450 Server-300 and the corresponding RMS error. Sizes of the filaments are optimized by the method discussed in the previous section. nh and nw in the figure captions stand for the vertical and the horizontal number of the substrate filaments, respectively. In the cases of $nw = 2$, the RMS error becomes 12%, and it is double compared with the other cases that nw is larger than 2. In other words, although it is generally thought that the large extraction resources are needed to consider the substrate effects, $nw = 3$, which consuming only less than 1 second of CPU time, reproduces the characteristic. The reason why $nw = 2$ cases do not reproduce the characteristics is that the horizontal distribution of the substrate current can not be expressed by the two horizontal filaments, because the vertical boundary of two filaments corresponds to the center of the signal line.

Taking into account these results, we propose to adopt 3×2 filaments as a general model. Furthermore, we can reduce three downward segments to one segment, without increasing the errors. The reduced filaments are shown in Fig. 13. We confirmed

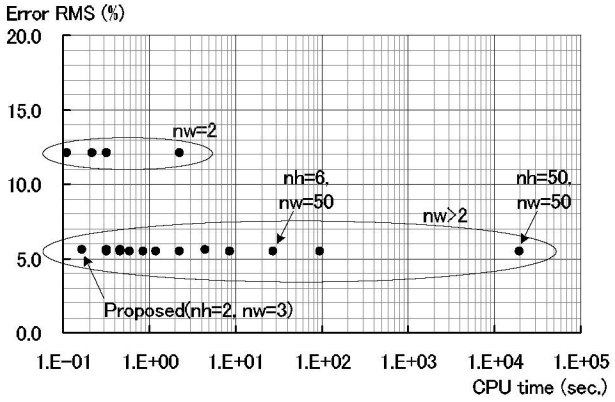

Figure 12: Relationship between computing time and the RMS error. (10mΩcm substrate).

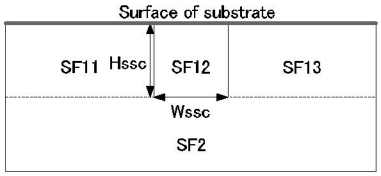

Figure 13: Cross-section of proposed four filaments substrate.

that the sizes of the four filaments, optimized to the micro-strip DUT, also reproduce the characteristics of the co-planer DUT. The results are shown in Figs. 14- 15. The frequency range is set from 50MHz up to 50GHz. Both of the resulting values of $Hssc$ and $Wssc$ in Fig. 13 have been set to 10μm for 10Ωcm substrate. The RMS errors are less than 7.0% to all patterns and parameters. Then, we confirmed robustness of the obtained filament size, changing height and width of the signal line. The sizes of the substrate filaments have been kept throughout this experiment. The results are shown in Table 1. The errors are below 10% if width of the signal line is less than 10μm, that is the size of $Wssc$ in Fig. 13.

5 Conclusion

In this paper, we experimentally proved that a small set of PEEC filaments can reproduce the frequency dependence of interconnect resistance and inductance caused by the substrate

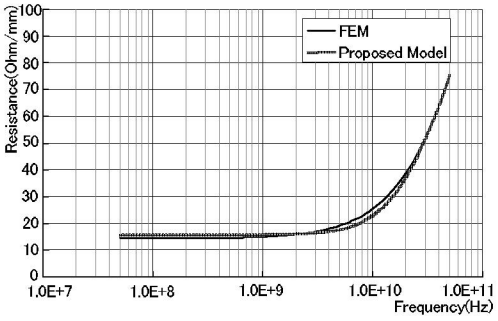

Figure 14: Resistance of MSL.(10mΩcm substrate, four filaments)

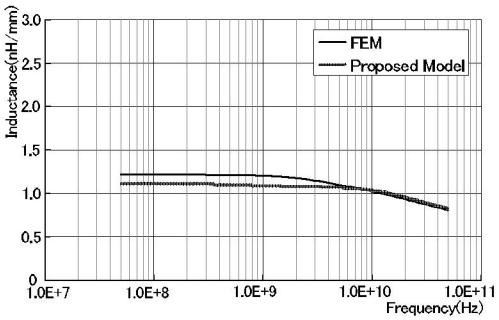

Figure 15: Inductance of MSL.(10mΩcm substrate, four filaments)

RMS error (%)		Resistance W(um)				Inductance W(um)			
		2	4	8	16	2	4	8	16
Metal	4	4.7	5.7	8.1	11.4	5.2	5.7	6.4	7.2
Layer	2	4.7	6.1	8.5	11.8	5.4	7.0	6.0	7.2

Table 1: Robustness of the proposed model

proximity effect. We also introduced a method to optimize the filaments. One promising application of the proposed modeling is interconnect process characterization for SoC chip-level RLC extraction tools, that use filament-based extractors during the characterization.

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