1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy

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Abstract

1.5x energy-efficient and 1.4x operation-speed, nonvolatile via-switch (VS) FPGA with atom switch and a-Si/SiN/a-Si varistor is demonstrated in a 65nm-node for various basic applications. For rapid and low-cost migration from VS-FPGA to ASIC, "hard-via" to replace VS with "ON", named VS-copy (VSC), is newly proposed. The VSC-ASIC is fabricated by sharing all the photo masks with VS-FPGA excepting one via mask revise and three VS masks skip, realizing an exact design copy with minimum NRE cost and TAT. The VS-FPGA equipped with the VSC gives energy-efficient edge device, e.g., for up-to-date AI inference algorithms, covering a wide range of chip volume with extremely low cost.

Keywords: Atom switch, Via-switch, Programmable logic, Cross-point, Non-volatile, FPGA, ASIC.

Introduction

Nowadays, FPGAs are widely used in up-to-date Internet of Things (IoT) solutions, serving for network gateway, data center, and edge devices thanks to their short design turn-around time (TAT) and hardware flexibility [1]. After rapid prototyping and early production using FPGAs at the sacrifice of relatively higher chip and programming costs, customers desire a quick transition to ASICs pursuing lower unit and NRE costs for high-volume production [2]. A nonvolatile atom-switch FPGA (AS-FPGA) has achieved 78.5% area [3], 66% delay and 60% energy reductions [4] by replacing a CMOS switch composed of an SRAM and a pass transistor (Tr.) to the atom switch with a cell Tr. (Fig.1). Recently, a via-switch FPGA (VS-FPGA) successfully uses a varistor in BEOL instead of the cell Tr. with further 61.4% area reduction [5].

In this paper, we precisely evaluate the energy and delay of VS-FPGA and newly propose an ASIC migration scheme named VS-copy ASIC (VSC-ASIC). Simply, we use "hard-via" to replace VS with "ON" for migrating to the VSC-ASIC. The smaller size and higher energy-efficiency of the VS-FPGA is advantageous, e.g., for in-situ AI inference and training in edge devices. We fabricate a 65-nm VS-FPGA with VSC and demonstrate the performance.

Evaluation of a 65-nm Via-Switch FPGA

All the AS-FPGA, VS-FPGA and VSC-ASIC with the same architecture consist of a configurable logic block (CLB) array (Fig.2). Each CLB has an input multiplexer (IMUX), a switch multiplexer (SMUX) and a logic block (LB). Crossbar switches are used in the IMUX and SMUX for a data transfer, and in a look-up table (LUT) for a function configuration. A one cell-Tr. and one complementary-atom-switch (1T1CAS) used in the AS-FPGA is replaced with the VS composed of two varistors and two ASs. Area reduction is obtained since the VSs are fabricated between M4 and M5 above a CMOS layer (Fig.3). TiN/a-Si/SiN/a-Si/TiN layers of the varistor are deposited on Ru-alloy/polymer-solid-electrolyte/Cu layers of the AS [6]. The VS is configured as ON- or OFF-state (Fig.4).

We evaluate the energy per cycle, delay and energy-delay product (EDP) of the AS- and VS-FPGAs by mapping three basic applications (a 16-bit counter, a 24-bit linear feedback shift register, a 4-bit multiplier) (Fig.5). The wider range of low-EDP (EDP < $1.1 \times \mathrm{EDP_{min}}$) of 0.8V-1.2V is attained by the smaller capacitance of the VS-FPGA (Fig.6). Totally, the VS-FPGA achieves reductions of 34% in energy, 29% in delay and 53% in EDP at VDD=1.2V (Table 1). These improvements mainly originate from the shorter interconnect length.

Via-Switch-Copy ASIC

The most ideal migration from an FPGA to an ASIC is an exact design copy with minimized additional verification time and cost. To migrate a VS crossbar switch to a VSC one, the vertical and horizontal signal lines (T1 and T2 in Fig.7) connected with ON-state VSs are replaced by "hard-vias", otherwise they are cut off. Since the data transfer delay in the VSC decreases with the reduced resistance from an ON-state VS to a "hard-via", a delay adjust scheme is newly introduced to realize an exact design copy and avoid timing violations, in which the voltage level of VCE in the VSC is tuned to make its delay the same as that of the VS one.

In the cell layout modification for VSC, the ASs and varistors, and the via4s (V4s) connecting to the VS are removed and a new V4 between T1 (M5) and T2 (M4) is added for an ON-state VS (Fig. 8). Both the VS-FPGA and VSC-ASIC share the CMOS logic and interconnects, while only the differences are VS process (three mask layers) skip and the V4 mask layer modification in the VSC-ASIC.

In evaluation of an SMUX chain, a data signal transfer through 36 SMUXs without any LBs maximizes the effect of the VS to V4 conversion (Fig.9(a)). The die of an SMUX-chain VSC-ASIC includes 6x6 CLBs (Fig.9(b)). The energy per cycle of the VSC-ASIC is reduced by 9% compared to that of the VS-FPGA at standard VDD=1.2V (Fig.10). Both the VS-FPGA and VSC-ASIC tuned by VCE have the same delay 18ns at 1.2V (Fig.11) and output waveforms (Fig.12). Table 2 summarizes performance comparison. Note that customers may choose another option of higher performance with higher VCE.

Summary

Thanks to programmable cross-point via-switches, a 65-nm nonvolatile low-energy high-speed FPGA is demonstrated. To achieve low unit cost for high-volume production, its via-switch-copy ASIC migration is fabricated sharing the same basic mask layers with the VS-FPGA for low cost.

Acknowledgement

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References

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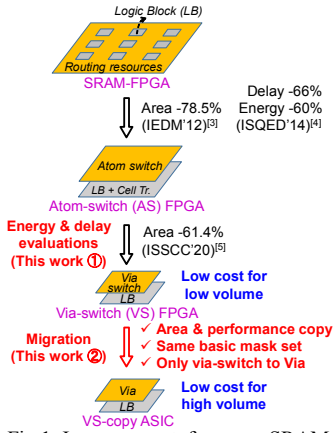

Fig.1 Improvement from an SRAM-FPGA to atom-switch (AS) and via-switch (VS) FPGAs, and migration to a via-switch-copy ASIC (VSC-ASIC).

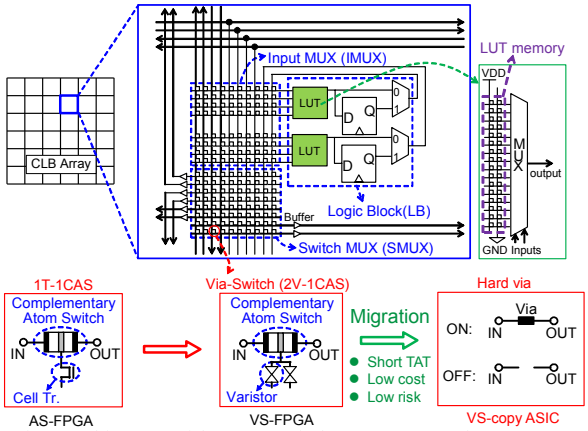

Fig.2 Architecture of the atom-switch FPGA. VSs replace 1T-1CASs for small area[5] and high performance. Furthermore, "hard-vias" replace VSs to migrate the VS-FPGA to the VSC-ASIC simply.

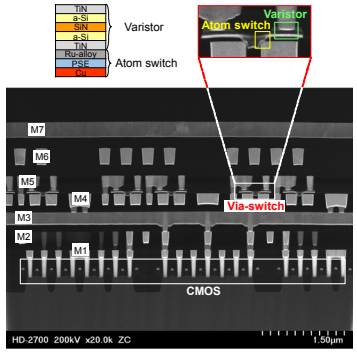

Fig.3 Cross-sectional TEM images. VSs are fabricated between M4 and M5.

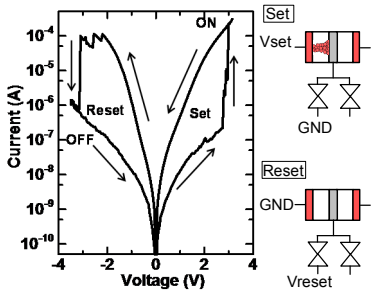

Fig.4 Set/reset I/V characteristics of a VS [6].

CNT16: 16-bit counter
LFSR24: 24-bit linear feedback shift register
MPY4: 4-bit multiplier

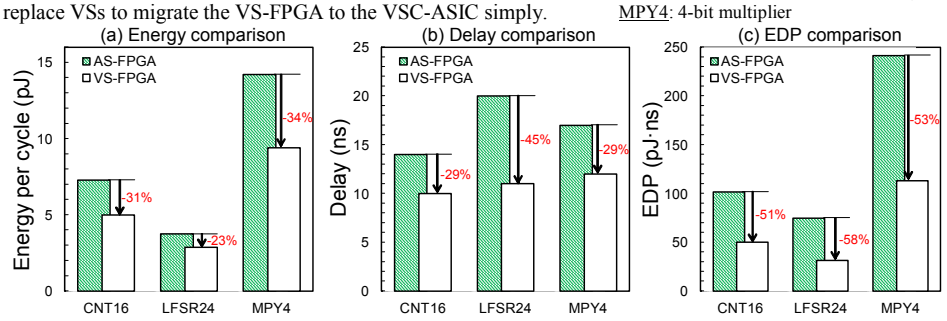

Fig.5 (a) Energy, (b) delay and (c) energy-delay product (EDP) comparisons between the AS- and VS-FPGAs. Operation voltage (VDD) is 1.2V for CNT16/MPY4 and 0.8V for LFSR24.

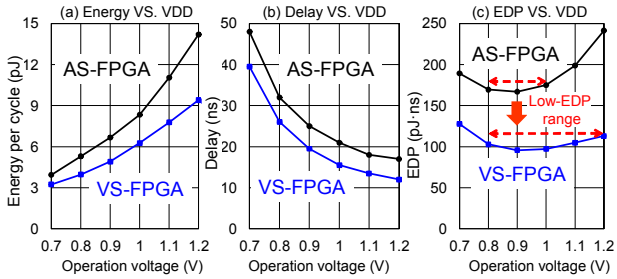

Fig.6 (a) Energy, (b) delay and (c) EDP versus VDD of the MPY4 in the AS- and VS-FPGAs.

Table 1 Performance comparison
(Application: a 4-bit multiplier)

	AS-FPGA	VS-FPGA (This work)
Switch	Atom switch + Cell Tr.	Via-switch
Process node	65 nm	65 nm
CLB Area (um²)	2,827	-61 % [5] 1091
Operation voltage(V)	1.2	1.2
Delay(ns)	17	-29 % 12
Energy per cycle(pJ)	14.20	-34 % 9.41
EDP(pJ·ns)	241	-53 % 113

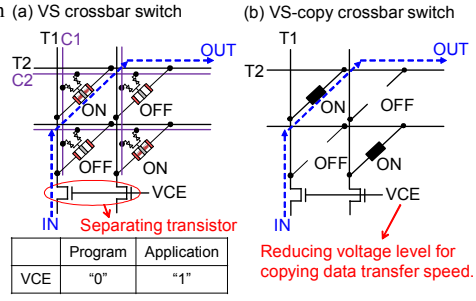

Fig.7 Migration from a VS crossbar switch to a VSC one. Separating transistors adjust the VSC crossbar switch's delay to match that of the VS one.

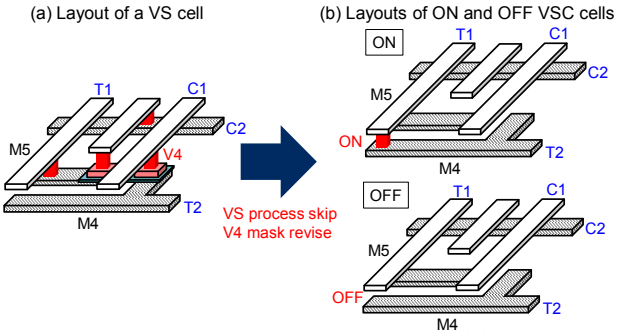

Fig.8 ON and OFF VS-copy by revising one via mask layer (V4).

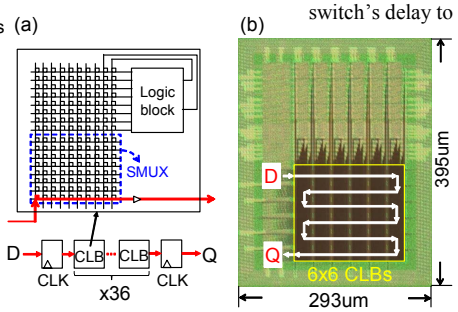

Fig.9 (a) An SMUX chain composed of 36 CLBs. (b) Die photo of an SMUX chain VSC-ASIC.

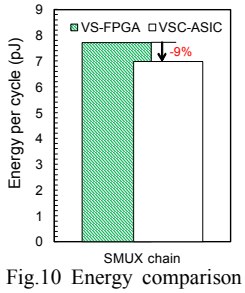

Fig.10 Energy comparison between the VS-FPGA and VSC-ASIC at VDD=1.2V.

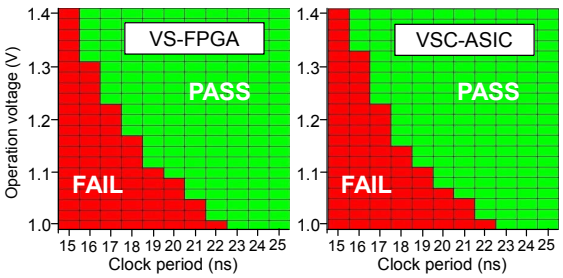

Fig.11 Shmoo plots of the VS-FPGA and VSC-ASIC.

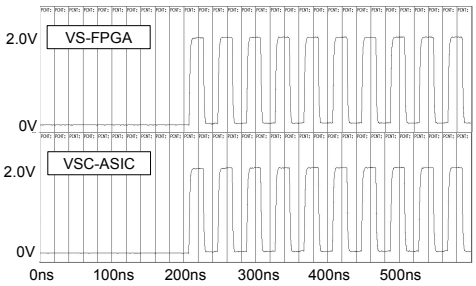

Fig.12 Waveforms of the VS-FPGA and VSC-ASIC.

Table 2 Performance comparison.
(Application: an SMUX chain)

	VS-FPGA	VSC-ASIC
Switch	Via-switch	Via
Process node	65 nm	65 nm
Operation voltage(V)	1.2	1.2
Delay(ns)	18	0 % 18
Energy per cycle(pJ)	7.7	-9 % 7.0
EDP(pJ·ns)	138.6	-9 % 126