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Measurement results of delay degradation due to power supply noise well correlated with full-chip simulation

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***Abstract*— Power integrity is an crucial design issue in nanometer technologies because of lowered supply voltage and current increase. This paper focuses on gate delay variation due to power/ground noise, and demonstrates measurement results in a 90nm technology. For full-chip simulation, a current model with capacitance and variable resistor is developed to accurately model current dependency on voltage drop. Measurement results are well correlated with simulation, and verify that gate delay depends on average voltage drop.**

I. INTRODUCTION

Power supply noise has become a critical design issue in current VLSI design. Power consumption of high-performance chips is still increasing, though supply voltage is lowered, which results in rapid increase in current. Current increase makes power distribution more difficult, and nowadays power supply noise can not be ignorably eliminated. Moreover, even with the same amplitude of power supply noise, the impact on timing becomes more and more significant because of lowered supply voltage. Delay degradation due to power supply noise must be considered for a successful chip design.

Recently, to study on-chip power supply noise, circuits to observe waveforms of power supply noise have been proposed and several measurement results of noise waveforms are reported [1]–[6]. On the other hand, effect of noise on timing is mainly discussed with simulation [7], and measurement results focusing on timing have been infrequently reported. Discussion on correlation between simulation and measurement results is found only in a few papers [3].

This paper discusses gate delay variation due to power supply noise based on measurement and simulation results in a CMOS 90nm technology. Contributions of this paper are:

1) verification of correlation between measurement and full-chip simulation results,
2) construction of a full-chip simulation model that can accurately reproduce switching current depending on noise-induced supply voltage,
3) confirmation that gate delay is mainly dependent on average supply voltage, not on peak voltage.

The remaining of this paper is organized as follows. Section 2 discusses impact of peak and average voltage drop on gate delay. Section 3 describes measurement circuit structure. Section 4 presents a full-chip simulation model that translates transistors to linear elements. Section 5 presents measurement results and discussion. Finally section 6 concludes this paper.

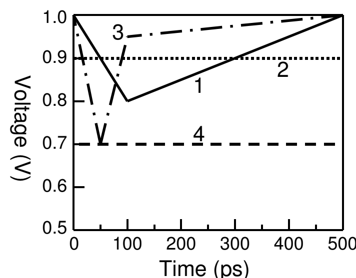

Fig. 1. Pseudo V_{dd} noise waveforms.

TABLE I
AVERAGE OF GATE DELAY WITH NOISES IN FIG 1.

	noise 1	noise 2	noise 3	noise 4
average gate delay (ps)	14.8	14.5	12.0	129.8

II. POWER SUPPLY NOISE EFFECT ON TIMING

In designing a power distribution network, peak voltage drop is widely considered as a serious concern. On the other hand, from the viewpoint of timing, where timing is the most principal issue for digital circuit design, average of power supply voltage is more important than peak noise voltage, because timing distortion is more dependent on average supply voltage during gate switching, not on peak voltage [8].

We here show an example that impact of power supply noise on timing is well estimated with average of supply voltage. We assume four pseudo V_{dd} noise waveforms shown in Fig. 1. V_{ss} waveforms are set to be upside down to V_{dd} waveforms. A 90nm CMOS process is assumed and ideal supply voltage is 1.0V. Table I shows the average gate delay under the pseudo waveforms. In the case of noise 1, the peak voltage drop is 0.2V and supply voltage recovers to 1.0V in 500ps. The voltage drop of noise 2 is set to the average drop of noise 1 from 0 to 500ps. We can see that the average gate delay of noise 1 is almost the same with that of noise 1 and the error is only 2.0%.

On the other hand, as for noise 3, though its peak voltage drop is 0.3V and is larger than that of noise 1, the average gate delay under noise 3 is smaller, because recovery to 1.0V is faster and then the average supply voltage of noise 3 is higher than that of noise 2. If we give the voltage of the worst case drop (noise 4), the estimated delay becomes too pessimistic. The timing estimation with the average supply voltage is more effective than that with peak voltage drop.

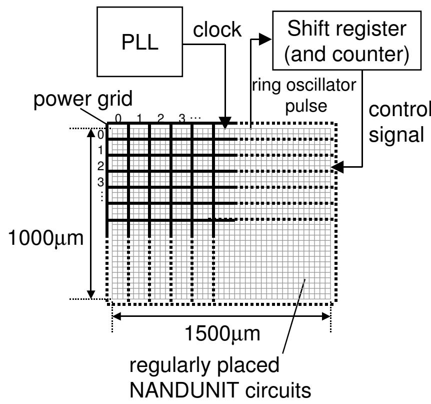

Fig. 2. Overview of measurement circuit.

TABLE II
PARAMETERS OF THE POWER GRID.

	Horizontal lines	Vertical lines
Metal layer	M6	M5
Width	2.5μm	7.5μm
Pitch	50μm	75μm
Thickness	0.9μm	0.3μm

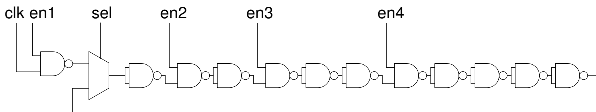

Fig. 3. NANDUNIT circuit.

III. MEASUREMENT CIRCUIT STRUCTURE

The objective of test chip design is to verify the correlation between circuit simulation and measurement results. We designed a test circuit that can control power supply noise flexibly and measure gate delay variation due to power supply noise.

Figure 2 roughly explains the layout of the measurement circuitry that consists of PLL, shift registers, grid power lines, ring oscillators, and NANDUNIT circuits. The design parameters of power grid is listed in table II, and 1000$\times$1500μm area is divided into 20$\times$20 areas by the power grid. We represent the location of grids as (x,y) in this paper; 0$\leq$x$\leq$19, 0$\leq$y$\leq$19, leftmost rectangles are x=0, uppermost rectangles are y=0, as indexed in Fig. 2.

NANDUNIT circuits (Fig. 3) are placed regularly and densely in every grid, and they operate to cause power supply noise. The operating time period, operation (active) ratio, and operating frequency of NANDUNIT can be controlled, which means that the noise waveform is changed in time, amplitude, and frequency.

NANDUNIT can operate both as a chain and as a ring oscillator. When NANDUNIT operates as a chain, clock signal generated by PLL is input as 'clk' signal in Fig. 3. PLL can generate 100MHz-1GHz clock signal delivered to NANDUNIT circuits with H-tree clock lines. Number of active gate stages can be changed with 'en2'-'en4' signals, i.e. operation time period of noise source is variable(Fig. 4). When NANDUNIT operates as a ring oscillator, NANDUNIT circuits run continuously. 17$\times$4 NANDUNIT circuits are located in each grid. 75% of 1000$\times$1500μm area is occupied by the NANDUNIT circuits. Operation ratio of the NANDUNIT circuits is selected from 100%, 50%, 25%, and 0%, which controls noise amplitude (Fig. 4). Control signals of NANDUNIT circuits, 'en1'-'en4' and 'sel', are input to each 4$\times$4 grid.

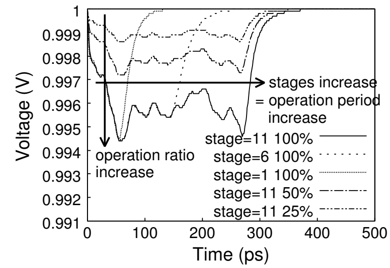

Fig. 4. Power line noise waveform. Numbers of active gate stage are changed.

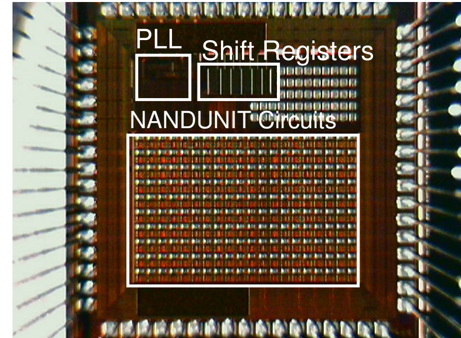

Fig. 5. Micrograph of the fabricated test chip.

Control signals of NANDUNIT and PLL are stored in the shift register. The counters are included in the shift register and operate both as the shift register and as the counter. Values of shift register and the counters are serially set/read externally.

In order to measure the delay variation caused by power supply noise, 100 ring oscillators are uniformly placed at the center of (2n+1,2m+1) grids (0$\leq$n$\leq$9, 0$\leq$m$\leq$9). The time cycle of ring oscillator is counted by the counters.

Figure 5 is the micrograph of the test chip, and location of the elements, such as PLL, NANDUNIT area, and shift registers, are indicated. DC transistor TEGs are placed at upper right area. The measured I-V characteristics are considered in circuit simulation.

IV. SWITCHING CURRENT MODEL FOR FULL-CHIP SIMULATION

Full-chip simulation for power/ground noise has a difficulty in CPU time and memory because there exists tremendous number of elements on a chip. To efficiently perform a full-chip simulation, we develop a switching current model with capacitance and variable resistor, so called "variable switch model" that well reproduces switching current depending on noise-induced supply voltage.

To accelerate the simulation, transistor elements are generally replaced with linear circuit models such as current source model and switching model [9]. The current source model represents a switching gate consisting of transistors as

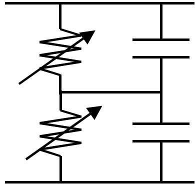

Fig. 6. variable switch model of an inverter.

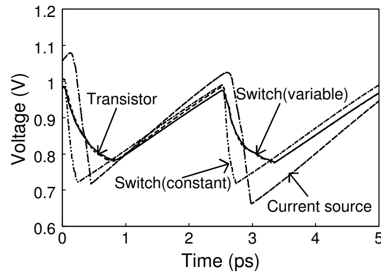

Fig. 7. Supply noise waveform with transistor model, current source model, and two switch models.

TABLE III

NORMALIZED SIMULATION TIME.

transistor	current source	constant switch	variable switch	variable switch(merged)
100%	2.1%	4.3%	6.3%	0.59%

a voltage independent current source. The switching model replaces a switching gate with resistance and capacitance [9]. The resistance value is ∞ or on-resistance of the corresponding transistor. The switching model, however, does not consider dependency of switching current on noise-induced supply voltage explicitly, and the current consumption is not well reproduced, because the gate delay degradation due to power supply noise is not modeled.

We here develop "variable switch model" in Fig. 6 that has finely-defined variable resistance depending on the supply voltage and the gate input voltage. Gate switching delay is accurately modeled in the developed model, which contributes to accurate full-chip simulation. To distinguish models, the conventional model with a constant resistance is called "constant switch model".

Figure 7 shows power supply noise waveforms simulated with the transistor model, the current source model, and two switch models. The circuit corresponds to a single grid of the measurement circuit, and 400 times of the package inductance are attached, which emulates voltage drop of the whole chip with the power consumption of a single grid. The V_{dd} waveform at the center of the grid is shown. The current source model and the constant switch model shows the sharper voltage drop waveform than transistor model, and the noise waveform of variable switch model nicely follows that of transistor model, because only variable switch model can reproduce the gate delay deterioration due to the voltage drop.

Table III shows normalized simulation time using the transistor model, current source model, and switch models. The simulation time in variable switch model is reasonably reduced. Integration of multiple cells to a single cell can also reduce the simulation cost. When 68 cells in a grid is merged into to 4 cells, simulation cost is decreased to 0.59%, though the average voltage error of the waveform is only 1.8mV. The reasonable simulation cost and accurate noise waveform estimation are achieved by the "variable switch model", which enables full-chip simulation in the next section.

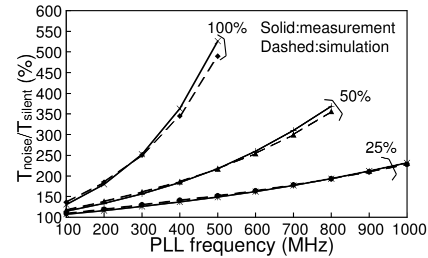

Fig. 8. T_{noise}/T_{silent} ratio in measurement results and simulation results. 100%/50%/25% of NANDUNITs is uniformly activated with 100MHz-1GHz PLL clock.

V. MEASUREMENT RESULT AND DISCUSSION

A. Simulation setup

We first explain simulation setup. In circuit simulation, NANDUNIT circuits are replaced by "variable switch model" discussed in Section IV. The power/ground wires are modeled carefully as resistance based on the layout pattern. Well junction capacitance is also attached. As the test chip is mounted on a QFP package, package and bonding inductance is also attached between ideal power/ground and chip power/ground pads.

B. Verification of simulation model

The ring oscillator cycle is computed from measured counter value. Average of five-times measurement is adopted for the cycle time. The standard deviation of 200 measurement results is 0.186ps, and the reproductivity is good enough.

We evaluate T_{noise}/T_{silent} ratio; T_{silent} is the cycle when all NANDUNITs are inactive and T_{noise} is the cycle under power supply noise caused by NANDUNITs.

Figure 8 shows T_{noise}/T_{silent} ratio of (9,9) ring oscillator, which is at the center of the power grid. The T_{noise}/T_{silent} ratio is compared between simulation and measurement result. The output clock frequency are changed from 100MHz to 1GHz. Ratio of active NANDUNITs is also varied. Simulation results are well correlated with measurement results, and the maximum error is 7.0%. In the range over 600MHz with 100% activity and over 900Mhz with 50% activity, the counter does not work well due to severe power supply noise, and hence the results are not plotted in the figure. The good correlation between simulation and measurement indicates that the simulation model is expected to finely reproduce the power supply noise on the real chip.

We next evaluate spatial distribution of power supply noise. NANDUNITs in $0 \leq x \leq 3$ are operated, and the cycles of the ring oscillators at (1,9), (5,9), (9,9), (13,9), (17,9) are observed. Figure 9 shows that T_{noise}/T_{silent} in simulation is close to that in measurement result at all PLL clock frequencies, and the maximum error is 6.3%. The consistency between simulation results and measurement results implies that the spatial distribution of the power supply noise is well reproduced in circuit simulation.

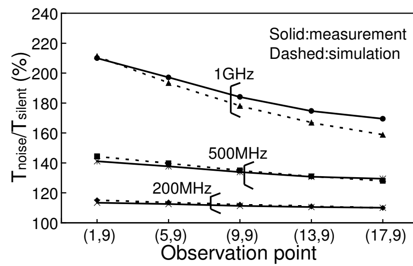

Fig. 9. T_{noise}/T_{silent} ratio at (1,9), (5,9), (9,9), (13,9), (17,9). NANDUNITs in $0 \leq x \leq 3$ area is activated with 200MHz, 500MHz, 1GHz PLL clock.

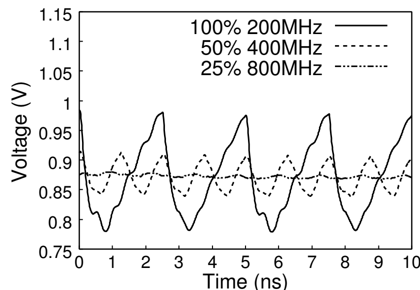

Fig. 10. Three simulation waveforms whose PLL clock frequency(MHz) × operation ratio values are equal.

C. Dependency of gate delay on average voltage drop

This subsection verifies the discussion in Section II based on measurement result: the gate delay variation mainly depends on the average of supply voltage.

Figure 10 shows noise waveforms in simulation, The average voltage values of three waveforms are 0.867V, 0.868V, and 0.870V with 100%, 50%, 25% activity respectively, and they are almost equal, while the noise shapes are different. These waveforms are selected such that the product of PLL clock frequency and the operation ratio of NANDUNITs becomes the same. Roughly speaking, as long as the product is identical and clock distribution is ignored, the power consumption is the same because it is proportional to frequency and number of active gates, and hence the average of the supply voltage are expected to be almost the same as shown in Fig. 10.

Figure 11 plots T_{noise}/T_{silent} with 100%, 50%, and 25% activity based on measurement results. X-axis is the product of frequency and activity.

When the product is the same, T_{noise}/T_{silent} values are almost the same, as we expected, even though the operating conditions in frequency and activity differ, and the peak voltage is estimated to be much different. T_{noise}/T_{silent} value of 100% operation ratio agrees with that of 50% and 25%, and the maximum error is 8.7%. This measurement result confirms the discussion based on simulation in Section II, i.e., gate delay strongly depends on the average of the supply voltage, not on the shape of noise waveform.

VI. Conclusion

In this paper, based on the measurement result, we verified the fidelity of full-chip circuit simulation model, and confirmed the dependency of gate delay on the average voltage drop.

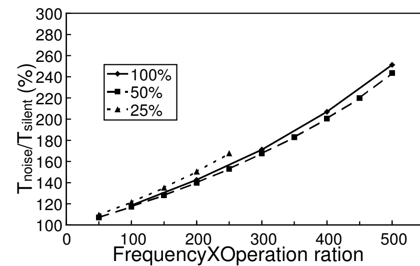

Fig. 11. T_{noise}/T_{silent} at (9,9) in measurement result. Stage of NANDUNIT is set to 6. X-axis is PLL clock frequency(MHz) × operation ratio.

To perform full-chip simulation, we developed a switching current model with capacitance and variable resistor that well reproduces switching current, and it saves simulation time by 94%

A measurement circuitry was designed to measure that delay degradation due to power supply noise, and the test chip was fabricated in a 90nm CMOS technology. Measurement results are well correlated with simulation results, and the simulation model is validated. Measurement results also confirm that gate delay mainly depends on the average voltage drop.

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