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A Sampling Switch Design Procedure for Active Matrix Liquid Crystal Displays

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SUMMARY In the design of an active matrix LCD (Liquid Crystal Display), the ratio of the pixel voltage to the video voltage (RPV) of a pixel is an important factor of the performance of the LCD, since the pixel voltage of each pixel determines its transmitted luminance. Thus, of practical importance is the issue of how to maintain the admissible allowance of RPV of each pixel within a prescribed narrow range. This constraint on RPV is analyzed in terms of circuit parameters associated with the sampling switch and sampling pulse of a column driver in the LCD. With the use of a minimal set of such circuit parameters, a design procedure is described dedicatedly for the sampling switch, which intends to seek an optimal sampling switch as well as an optimal sampling pulse waveform. A number of experimental results show that an optimal sampling switch attained by the proposed procedure yields a source driver with almost 18% less power consumption than the one by manual design. Moreover, the percentage of the RPVs within 100±1% among 270 cases of fluctuations is 88.1% for the optimal sampling switch, but 46.7% for the manual design.

key words: *active matrix LCD, CAD tool, column driver, sampling pulse, sampling switch*

1. Introduction

LCDs (Liquid Crystal Displays) have established a firm foothold on the market as flat panel displays, first for calculators, subsequently for personal computers, mobile appliances, digital cameras, and so forth, and at present with increasing importance for TVs. Thus, development is continuing further on improving the picture quality as well as on the picture function of LCDs, and hence the design automation has to be enhanced more and more for column drivers which affect most the performance of LCDs [1], [2].

In a *TFT* (Thin Film Transistor)-addressed LCD, usually called an *active matrix LCD*, as illustrated in Fig. 1, the grey shade of each pixel is controlled individually by a designated pixel voltage. In each column driver, a pair of nMOS TFT and pMOS TFT connected in parallel constitutes a sampling switch, as shown in Fig. 2, which is to sample the video signal and then to transmit the signal to the source line.

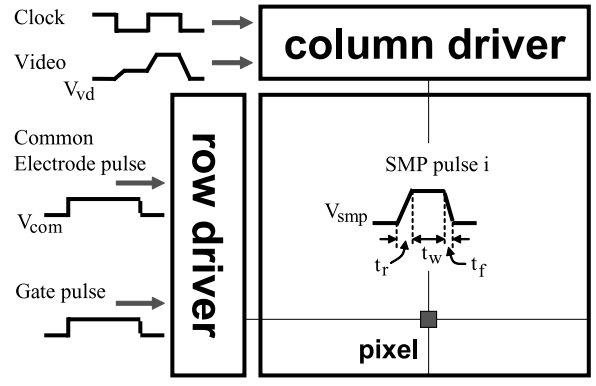

Fig. 1 Active matrix LCD.

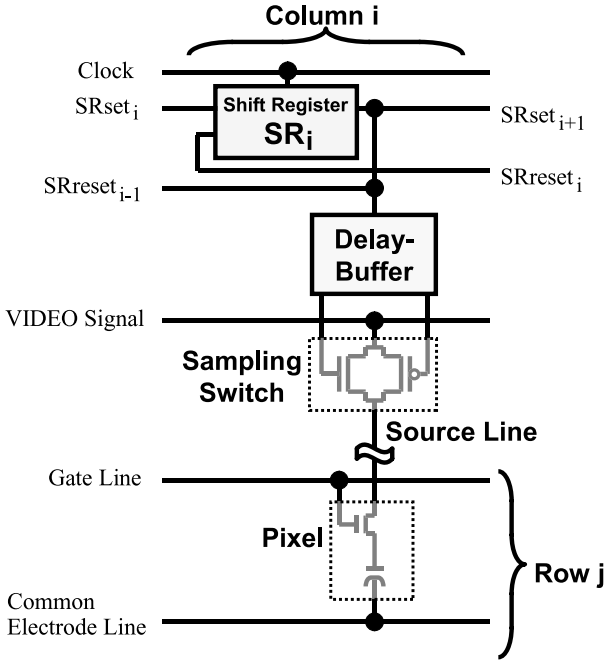

Fig. 2 Column driver in active matrix LCD.

During the period when all pixels in a row are activated by a gate line, a video voltage is fed to each pixel in the row from column to column so as to display a designated gray shade, whereas all pixels in other rows are blocked by grounding their gate lines. Thus, during this period each column driver has to transmit a designated voltage to a pixel in the row, one at a time from left to right, and hence the

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operation speed of a column driver is far greater than that of a row driver. This implies that the column driver plays a principal role to determine RPV (Ratio of Pixel voltage to Video voltage) of each pixel.

Given a pixel, let V_{vd} denote the video voltage to be fed to it, and let V_{px} represent the pixel voltage. Thus for this pixel we have RPV = $(V_{px}/V_{vd}) \times 100[\%]$. Our ideal goal is to make this RPV approach 100[%], or in other words, to make each pixel attain the designated grey shade.

Recently, with the rapid advance of LCD technologies, the column and row drivers have to be integrated more and more finely on the same substrate as the picture plane [2]–[4]. However, in such integration there occur considerable fluctuations in circuit parameters, which make the design of a column driver complicated, mainly from the aspect of the functional capability as well as the reduction of the area and power consumption.

This paper intends to construct a CAD tool for the column driver, aiming at the following objectives:

- Given a specified number B, maintain RPV within $100 \pm B[\%]$.
- Minimize the power consumption.
- Minimize the delay and fluctuation of the sampling pulse from the system clock.
- Integrate each column driver within a given width.

To achieve these objectives, the most intensive work is to construct a design procedure to determine the size of each transistor in the column driver.

Since sampling switch and sampling pulse waveform are most important in the column driver in order to achieve the target RPV, we focus on them in this paper. The sub-circuit consisting of a sampling switch and a pixel is a kind of a sample-and-hold circuit [5] and has been considered in the various applications [6]–[11] and also from the viewpoint of modeling and analysis methods [12]. However, as far as we know, there is no specific report treating a sampling switch from the viewpoint of the quality of display. Hence, in what follows, we consider a design procedure for determining the size of sampling switch and the waveform of sampling pulse with the use of a full transistor model (a SPICE model) for a CMOS switch.

This paper first analyzes how the design parameters associated with the sampling switch and sampling pulse waveform are related to RPV, and then selects a minimal set of parameters which contributes most to the behavior of RPV, by taking into consideration various types of video signal feeding to a pixel and fluctuations of design parameters. With the use of such a set of parameters, a design procedure is described for seeking an optimal TFT size and sampling pulse waveform. In order to find an optimal size and waveform, a circuit simulator such as SPICE simulation must be repeated for the sub-circuit consisting of a sampling switch and a column of pixels, but the number of repetitions can be reduced by using the minimal number of parameters. Experimental results are also shown to reveal that an optimal sampling switch attained by this procedure gives rise to a column driver with almost 18% less power consumption and 41.4 point better performance in fluctuations than the one by manual design.

The proposed procedure requires some input values such as ratios of fluctuations of design parameters, timing relations between video signals and sampling pulses, and minimum and maximum possible widths of pMOS and nMOS TFTs. If the design of a column driver starts from scratch, it may be hard to give appropriate values to them, although the procedure can be used in a cut-and-try manner. Therefore, the procedure would be most effective for the redesign of column drivers.

2. Preparations

2.1 Definitions of Symbols

First, design parameters associated with sampling switch and sampling pulse waveform are discussed. Let W_n be the gate width of an nMOS TFT, and let *SMP* denote a sampling pulse which is input to the gate of this nMOS TFT, for which the rising time, falling time, and intermediate time between them are denoted by t_r, t_f, and t_w, respectively (see Fig. 1). Similarly, let W_p be the gate width of a pMOS TFT, and let *SMPB* designate a sampling pulse input to the gate of this pMOS TFT. For simplicity, let both of SMP and SMPB be of the piece-wise linear waveforms, reverse to each other. Thus, W_n, W_p, t_r, t_f, and t_w can be regarded as the basic design parameters associated with sampling switch and SMP (SMPB).

2.2 Types of Feeding

Although t_r, t_f, and t_w are common to SMP and SMPB, RPV changes differently according to the combination of video voltage V_{vd} and common electrode voltage V_{com}, as outlined below.

First, it should be remarked that the common electrode voltage V_{com} for a row of pixels alternates between a high voltage level $V_{com-high}$ and a low voltage level $V_{com-low}$, frame by frame. Hence, if signal V_{com} is at $V_{com-high}$ when a pixel receives a video signal, then next time it receives a video signal when V_{com} is at $V_{com-low}$, and vice versa. If V_{com} of a row of pixels is set to the low level $V_{com-low}$, then the pixel voltage of each pixel in the row is lowered, and it is raised to a given video voltage when the sampling switch corresponding to a pixel in the row is open. This type of feeding of a video signal to a pixel is designated as the *plus* feeding. On the other hand, if V_{com} is set to the high level $V_{com-high}$, then the pixel voltage of the row is raised, and it is lowered to a given video voltage when the sampling switch is open. This type of feeding is referred to as the *minus* feeding.

Usually one type of feeding is more *difficult* than another to make a pixel voltage equal to a designated video voltage. Such a *difficult* feeding case can be found by applying the SPICE simulation to the sub-circuit consisting of a sampling switch and a column of pixels with respect to a

few typical values of circuit parameters. In fact, according to experimental results, the minus feeding can happen to be the *difficult* case, that is, the time from the beginning of t_r to the instance when pixel voltage V_{px} approaches enough video voltage V_{vd} in the minus feeding is longer as compared with the plus feeding. This *difficult* feeding case can play an important role in determining the minimum values W_{p-min} and W_{n-min} of W_p and W_n, respectively, as follows: If widths W_p and W_n are less than W_{p-min} and W_{n-min}, respectively, then RPV may be less than $100 - B[\%]$ in a *difficult* feeding case.

Note that the minimum values W_{p-min} and W_{n-min} depend on the lengths of t_r, t_w, and t_f, and it can be seen that the task to find these minimum values is not an easy task. However, the lower bound of the widths of TFTs in the sampling switch can be estimated by repeated application of the SPICE simulation to typical combinations of video voltage V_{vd} and common electrode voltage V_{com}.

2.3 Charge Injection

Even if pixel voltage V_{px} reaches to a designated video voltage before the sampling switch turns off, V_{px} may change by the so-called *channel charge injection* after the sampling switch turns off [7]–[11]. This voltage change ΔV_{px} depends on W_n, W_p, and source-gate voltage V_{gs} of TFT. If V_{gs} is constant, then ΔV_{px} can be made equal to zero by imposing a relation $W_p = a \cdot W_n + b$ for widths W_p and W_n. This relation holds for practical ranges of W_p and W_n, and b is usually small compared to the range of W_p. However, the coefficients a and b are constants depending on V_{gs}, and moreover this V_{gs} varies with video voltage V_{vd}. Hence it is impossible to make ΔV_{px} equal to zero for any value of V_{vd} without changing the circuit structure of the sampling switch.

The effect of charge injection has been considered in various applications and proposed many techniques to reduce the effect [9]–[11]. However, our sampling switch is assumed to be a simple CMOS switch, and only the widths of TFTs can be changed. Therefore, we use the effect of charge injection actively and effectively as shown below.

As described above, ΔV_{px} can be made equal to zero for a particular voltage of V_{vd} by using an explicit relation for W_n and W_p. Noting the nonlinear relation between the transmitted luminance and pixel voltage V_{px}, we can see that there exists a pixel voltage V_{px-mdl} which changes the transmitted luminance most steeply. If we reduce the change ΔV_{px} of the pixel voltage to zero at this voltage V_{px-mdl}, then the difference of the transmitted luminance caused by the charge injection can be reduced as small as possible. Therefore, we seek this voltage V_{px-mdl}, and by using the source-gate voltage V_{gs} attained by V_{px-mdl}, we find constants a and b which reduce ΔV_{px} to 0.

The values a and b are obtained by finding two pairs (W_n, W_p) satisfying $\Delta V_{px} = 0$ for large and small values of W_n. For a given W_n, W_p satisfying $\Delta V_{px} = 0$ can be calculated by a binary search. Namely, if ΔV_{px} calculated for a pair (W_n, W_p) is negative, then W_p must be increased, and otherwise, it is decreased. The voltage change ΔV_{px} is computed by SPICE by turning off the sampling switch with a fully charged pixel. Since the relation $W_p = a \cdot W_n + b$ is imposed on W_p and W_n, a set of basic design parameters for the sampling switch can be reduced to $\{W_n, t_r, t_f, t_w\}$.

Since ΔV_{px} is zero only at this V_{px-mdl}, at another video voltage V_{vd} which does not attain the pixel voltage V_{px-mdl}, pixel voltage V_{px} may change after the sampling switch turns off. Therefore, due to the charge injection, it becomes harder to satisfy the constraints on RPV for any video voltage V_{vd}. Moreover, it should be noted that ΔV_{px} may be larger than 0 at a certain video voltage V_{vd}, and hence it may happen that RPV exceeds $100 + B[\%]$. This type of violation can occur in the case when a pixel voltage is *easy* to reach to a designated video voltage, that is, pixel voltage V_{px} approaches V_{vd} more quickly than that in the *difficult* feeding case.

Such an *easy* feeding case can play an important role to determine the maximum value W_{n-max} of width W_n. Namely, if width W_n is increased to satisfy the constraint on RPV to be over $100 - B[\%]$ in the *difficult* feeding case, and if it exceeds W_{n-max}, then RPV may exceed $100 + B[\%]$ in the *easy* feeding case. Similarly as the minimum value W_{n-min} of W_n, the maximum value W_{n-max} of W_n depends on the lengths of t_r, t_w, and t_f, and hence is hard to compute. But the upper bound of W_n can be estimated by repeated application of the SPICE simulation.

2.4 Fluctuations

As mentioned above, a variety of fluctuations in the design parameters must be taken into account in the design of the column driver for active matrix LCDs [2]–[4]. Hence, of practical importance is the technical capability of how to cope with these fluctuations, such as transistor performances (SPICE parameters), voltage sources, etc., in the design task of the sampling switch. Henceforth, we assume the following situations.

- Gate widths W_n and W_p fluctuate within $W_n \pm \sigma_n$ and $W_p \pm \sigma_p$, respectively.
- High and row voltage levels V_{high} and V_{low} of SMP (SMPB) fluctuate within $V_{high} \pm \upsilon_{high}$ and $V_{low} \pm \upsilon_{low}$, respectively. Although supply voltage V_{dd} and V_{ss} also fluctuate, these voltages do not appear explicitly in the sampling switch, and hence fluctuations of V_{dd} and V_{ss} are not treated directly in this paper.
- SPICE parameters of nMOS and pMOS TFTs fluctuate among *best*, *typical*, and *worst* cases, and the following five combinations of fluctuations occur: nBpB, nTpT, nWpW, nBpW, and nWpB, where n and p denote nMOS and pMOS, respectively, and B, T, and W represent best, typical, and worst cases, respectively.

Due to the fluctuations of supply voltages and transistor performances in Delay-Buffer, the waveforms of SMP and SMPB also fluctuate. Now, assume that t_r, t_f, and t_w of SMP (SMPB) fluctuate within $t_r \cdot (1 \pm \varepsilon_r)$, $t_f \cdot (1 \pm \varepsilon_f)$, and $t_w \cdot (1 \pm \varepsilon_w)$,

respectively, where ε's are positive decimals between 0 and 1. Moreover, SMPB delays from SMP and the delay fluctuates within $\pm\delta$. In addition to these fluctuations, a time parameter T indicating the time interval during which the video signal keeps a voltage for a pixel, fluctuates within $T \cdot (1 \pm \varepsilon_T)$, where ε_T is also a positive decimal between 0 and 1. Note that T is the half of the period of the system clock.

These ε's and δ are determined by the performance of Delay-Buffer generating SMP and SMPB. On the other hand, the purpose of this paper is to find the conditions of SMP and SMPB for the constraints on RPV to be satisfied, and Delay-Buffer is designed with the use of these conditions. Therefore, it seems to be a conflict to assume that these ε's and δ are given in this paper. However, these values can be estimated from design experiences or can be set as design targets. Thus, we assume these ε's and δ.

Due to the fluctuations, there arise various cases to be considered, which are totally $270 = 2 \times 3 \times 3 \times 3 \times 5$ cases, where 2 types of feeding (plus and minus), 3 video voltages (high, middle, and low), 3 high voltages of SMP ($V_{\text{high}} - \upsilon_{\text{high}}$, V_{high}, and $V_{\text{high}} + \upsilon_{\text{high}}$), 3 low voltages of SMP ($V_{\text{low}} - \upsilon_{\text{low}}$, V_{low}, and $V_{\text{low}} + \upsilon_{\text{low}}$), and 5 combinations of TFT fluctuations (nBpB, nTpT, nWpW, nBpW, and nWpB). Hence the classification of *difficult* and *easy* feeding cases stated above ceases to be definite. Thus, let us introduce extended definitions of them as follows: For given W_{n} and $W_{\text{p}} = a \cdot W_{\text{n}} + b$, the case where RPV is the lowest or highest value among all cases is called *Case D* or *Case E*, respectively. *Case D* occurs when

- ΔV_{px} is negative, or
- SMP and SMPB do not swing fully (i.e., V_{high} is $V_{\text{high}} - \upsilon_{\text{high}}$ and V_{low} is $V_{\text{low}} + \upsilon_{\text{low}}$), and
- SPICE parameters are in the worst case,

and is used to determine $W_{\text{n-min}}$. On the other hand, *Case E* occurs when

- ΔV_{px} is positive, and
- SPCIE parameters are in the best case,

and is used to determine $W_{\text{n-max}}$.

Case D or C*ase E* is not necessarily unique, and may vary depending on W_{n}. Hence, in order to identify these cases, RPVs are computed for 270 cases for the largest and smallest values of W_{n}, and the top and bottom 10 cases for each value of W_{n} are chosen and checked, from which candidates for *Case D* and C*ase E* are selected. The largest and smallest values of W_{n} can be obtained by using the width of a column circuit of the column driver and the process technology, respectively. Since only the order of RPV values is considered, the waveforms of SMP and SMPB do not affect the selection of candidates for *Case D* and C*ase E*.

2.5 Sampling Methods

As described before, when a row of pixels is activated by a row driver, common electrode voltage V_{com} of the row is either raised or lowered, and in according with V_{com}, pixel voltage V_{px} is also raised or lowered, respectively. In order to make V_{px} of a pixel be close to the video voltage level as quickly as possible, the so-called *double sampling* is used, which opens the sampling switch of a pixel before the video signal for the pixel is input. The ordinary sampling method is called *simple sampling*, and the timing charts of these sampling methods are shown in Fig. 3.

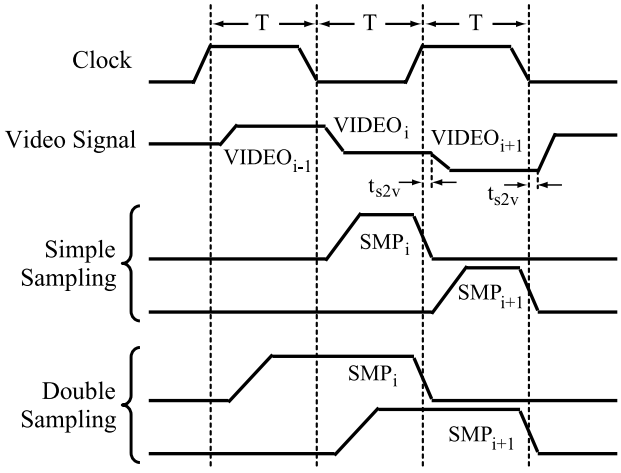

Fig. 3 Timing charts of simple and double samplings.

As can be seen from the figure, the *simple sampling* opens the sampling switch for the *i*th pixel only during the time interval of T when the video signal holds voltage VIDEO_{i} for the *i*th pixel; whereas the *double sampling* opens the sampling switch for the *i*th pixel during the time interval when the video signal holds $\text{VIDEO}_{\text{i}-1}$ for the $(i-1)$th pixel and keeps open during when the video signal holds VIDEO_{i} for the *i*th pixel.

3. Design Procedure

A design procedure for the sampling switch and sampling pulse SMP (SMPB) is described in what follows.

3.1 Waveforms of SMP and SMPB

First, it should be noticed that the longer is the opening period of the sampling switch, the shorter W_{n} and W_{p} can be made, and moreover shortening W_{n} and W_{p} can contribute greatly to the area and power reduction of a column driver. Hence, the pulse width of SMP (SMPB) should be made as long as possible. Noting that t_{r} and t_{f} are regulated by Buffer sub-circuit of Delay-Buffer but t_{w} by Delay sub-circuit, let us determine t_{w} with the use of the following equations in order that the total pulse width $t_{\text{r}} + t_{\text{w}} + t_{\text{f}}$ of SMP (SMPB) can be made as long as possible.

⟨*The case of simple sampling*⟩

$$(1+\varepsilon_{\text{r}}) \cdot t_{\text{r}} + (1+\varepsilon_{\text{w}}) \cdot t_{\text{w}} + (1+\varepsilon_{\text{f}}) \cdot t_{\text{f}} = T \cdot (1-\varepsilon_{\text{T}}) \quad (1)$$

⟨*The case of double sampling*⟩

$$(1+\varepsilon_{\text{r}}) \cdot t_{\text{r}} + (1+\varepsilon_{\text{w}}) \cdot t_{\text{w}} + (1+\varepsilon_{\text{f}}) \cdot t_{\text{f}} = 2T \cdot (1-\varepsilon_{\text{T}}) \quad (2)$$

Using these equations, design parameters W_{n}, t_{r}, t_{f}, and

t_w associated with the sampling switch and SMP (SMPB) can be reduced to a basic set $\{t_r, t_f, W_n\}$ of three elements. Thus the remaining task is to seek an optimal 3-tuple (t_r, t_f, W_n) which satisfies the constraints on RPV. To devise an algorithm for seeking such an optimal 3-tuple, we consider the ranges of t_r and t_f.

Let t_{r-min} and t_{f-min} denote the minimum possible values of t_r and t_f, respectively, which can be determined from the case when a sampling switch with the minimal widths TFTs is driven by Buffer with the maximal widths TFTs. With the use of t_{r-min} and t_{f-min}, the lower bounds of t_r and t_f are set by $t_{r-min}/(1-\varepsilon_r)$ and $t_{f-min}/(1-\varepsilon_f)$, respectively.

Let t_{s2v} be the time interval between the instance at which SMP falls 50% down from V_{high} and the instance at which the video signal begins to change to the next pixel video voltage (see Fig. 3). Since video signal is an input of column driver, t_{s2v} is specified by designers. Since SMP must fall down to the bottom and SMPB must rise up to the top before the video signal begins to change to the next pixel video voltage, $t_f/2$ and $\delta+t_f/2$ must be smaller than t_{s2v}. From them, the upper bound of t_f is obtained as $2(t_{s2v}-\delta)$.

The upper bound of t_r can be obtained from the condition that $t_r + t_f$ should not exceed T. If $t_r + t_f$ becomes larger than T, SMP can not fully swing in the case of simple sampling, and two consecutive sampling switches turn on simultaneously in the case of double sampling. In such cases, it is very hard to satisfy the constraints on RPV. From these observations, we have the ranges of t_r and t_f as follows:

$$t_{f-min}/(1-\varepsilon_f) \le t_f \le 2\cdot(t_{s2v}-\delta)/(1+\varepsilon_f). \quad (3)$$

$$t_{r-min}/(1-\varepsilon_r) \le t_r \le \{T\cdot(1-\varepsilon_r) - t_f\cdot(1+\varepsilon_f)\}/(1+\varepsilon_r). \quad (4)$$

3.2 Optimal Solution

Remark that the shorter is W_n, the greater is the area and power reduction of the sampling switch, and hence W_n of an optimal 3-tuple (t_r, t_f, W_n) must be minimal. On the other hand, note that the longer are t_r and t_f, the smaller are transistor widths in Delay-Buffer, contributing to its area reduction, and hence t_r and t_f of an optimal 3-tuple (t_r, t_f, W_n) must be maximal. However, in order to satisfy the constraints on RPV, shorter W_n requires longer t_w, and hence by Eq. (1) or (2), t_r and t_f should be shorter. Therefore, there arises a trade-off among t_r, t_f, and W_n. Moreover, since t_r, t_f and t_w must satisfy Eq. (1) or (2), there exists a trade-off between t_r and t_f, too. Namely, if t_r is shortened, then t_f can be longer, and vice versa.

To resolve these trade-offs precisely, Delay-Buffer, a sampling switch, and a pixel must be considered all at once. In this case, however, the number of design parameters becomes too large to pursue an optimal solution. Therefore, in this paper only the sampling switch and SMP (SMPB) are taken into account, for which a heuristic algorithm is devised to seek an optimal 3-tuple (t_r, t_f, W_n).

For given SMP and SMPB, that is, for given t_r, t_w, t_f, and δ, let W_{n-min} and W_{n-max} be the minimum and maximum values of W_n such that if $W_{n-min} \le W_n \le W_{n-max}$ then RPV is within $100 \pm B[\%]$ in any case. These W_{n-min} and W_{n-max} are calculated by means of SPICE simulation with the use of candidates for *Case D* and *Case E*, respectively. In fact, such values of W_{n-min} and W_{n-max} are sought as shown in Fig. 4, where the upper and lower surfaces at small t_r represent sets of feasible values of (t_r, t_f, W_{n-max}) and (t_r, t_f, W_{n-min}), respectively. The space between these two surfaces indicates a set of feasible values (t_r, t_f, W_n), which satisfy the constraint on RPV in any case. Thus there exists an optimum 3-tuple (t_r, t_f, W_n) in this space.

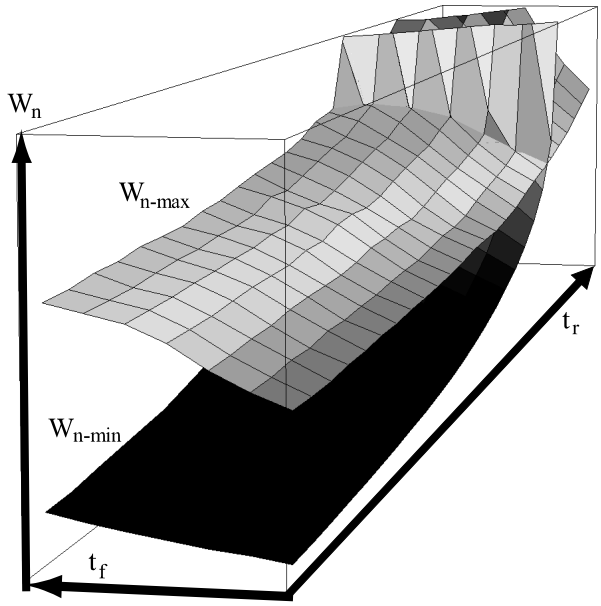

Fig. 4 Typical values of W_{n-min} and W_{n-max}.

Figure 4 shows that both W_{n-max} and W_{n-min} increase according as t_r increases, and two surfaces cross each other when t_r becomes large. Their reasons are as follows: For a given t_f, if t_r becomes large, then t_w is shortened, and hence it becomes hard for RPV to be raised to 100%. Therefore, in *Case D*, W_{n-min} must be widened so as to increase RPV over $100-B[\%]$. Moreover, in *Case E*, even if ΔV_{px} due to charge injection becomes large, RPV does not exceed 100%, so that W_{n-max} increases according as t_r increases, since the larger is W_n, the greater is ΔV_{px}. However, this increase of W_{n-max} is not so large as W_{n-min}, and hence W_{n-min} increases more steeply than W_{n-max}. Thus, according as t_r increases, the difference $W_{n-max} - W_{n-min}$ decreases monotonically, until it reaches to zero.

In active matrix LCDs, RPV of a pixel is more sensitive to the change of t_f than t_r, and the range of t_f is much smaller than that of t_r. Therefore, we set t_f to be as large as possible, that is, $t_f = 2\cdot(t_{s2v}-\delta)/(1+\varepsilon_f)$, in order to make the design of Delay-Buffer easier. Then, the problem to be considered becomes the one to resolve the trade-off between t_r and W_n. By taking into account the current technology of LCD and tendency shown in Fig. 4, this trade-off is resolved as follows.

Since W_n and $W_p = a \cdot W_n + b$ fluctuate within $\pm\sigma_n$ and $\pm\sigma_p$, respectively, the optimal value of W_n must satisfy $W_{n-max} - W_{n-min} \geq 2\sigma_n$ and $W_{n-max} - W_{n-min} \geq 2\sigma_p/a$. Hence, in this paper, we determine W_n by the following equations.

$$W_n = (W_{n-max} + W_{n-min})/2 \quad (5)$$

$$W_{n-max} - W_{n-min} = \max[2\sigma_n, 2\sigma_p/a] \quad (6)$$

Namely, W_n is set to be maximal so as to make the design of Delay-Buffer easier by making t_r as long as possible. Thus, an optimal 3-tuple (t_r, t_f, W_n) is defined as a 3-tuple such that

- $t_f = 2 \cdot (t_{s2v} - \delta)/(1 + \varepsilon_f)$,
- W_{n-max} and W_{n-min} determined from t_r satisfy (6),
- $W_n = (W_{n-max} + W_{n-min})/2$.

3.3 Design Procedure

For given t_f, t_w, and t_r, W_{n-max} and W_{n-min} can be found by a binary search with the use of candidates for *Case D* and *Case E*, as illustrated in Fig. 5. Let two curves in Fig. 5 denote the surfaces of W_{n-min} and W_{n-max} in Fig. 4 at $t_f = 2 \cdot (t_{s2v} - \delta)/(1 + \varepsilon_f)$, and consider points X and Y at t_r = L. If RPVs are calculated for pairs (t_r, W_n) corresponding to X and Y with the use of candidates for *Case E*, then the maximum RPVs for X and Y become over $100 + B$[%] and below $100 + B$[%], respectively. Hence, for a pair (t_r, W_n) corresponding to point Z which is located in the middle of X and Y, RPVs are calculated again for the candidates for *Case E*, and Z is regarded as new X, if the maximum RPV is larger than $100 + B$[%]. Otherwise, Z is regarded as new Y. Repeating such a process until points X and Y are close each other, W_{n-max}=MAX_L at $t_r = L$ can be found. By repeating similar process for the candidates for *Case D*, W_{n-min}=MIN_L at $t_r = L$ can be found, but in the process, the minimum RPV is compared with $100 - B$[%].

To seek t_r such that W_{n-max} and W_{n-min} determined for t_r satisfy (6), a binary search can be used again, as illustrated in Fig. 5. If W_{n-max} and W_{n-min} are calculated for $t_r = L$ and $t_r = U$, then $W_{n-min} = MIN_L < W_{n-max} = MAX_L$ and $MAX_L - MIN_L > \max[2\sigma_n, 2\sigma_p/a]$ at $t_r = L$, and $W_{n-min} = MIN_U > W_{n-max} = MAX_U$ at $t_r = U$. Hence, for $t_r = C = (U + L)/2$, $W_{n-min} = MIN_C$ and $W_{n-max} = MAX_C$ are calculated, and C is regarded as new L if $MIN_C < MAX_C$ and $MAX_C - MIN_C > \max[2\sigma_n, 2\sigma_p/a]$. Otherwise, C is regarded as new U, and this process is repeated until L and U are close each other.

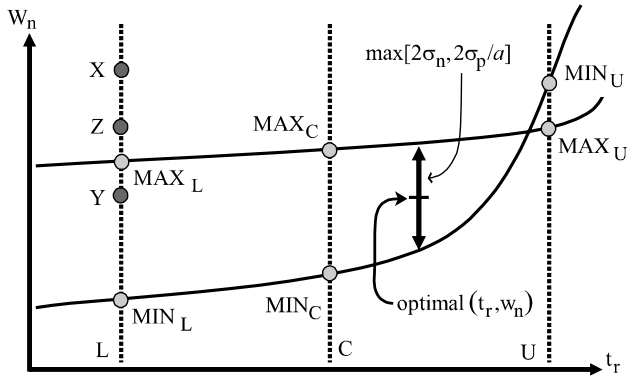

Fig. 5 Illustrated example to find an optimal W_n.

The proposed overall design procedure is outlined as follows.

Step 1: For the video voltage which makes the transmitted luminance of a pixel change most steeply, seek constants a and b in the equation $W_p = a \cdot W_n + b$ which reduces ΔV_{px} to 0.

Step 2: Compute $t_f = 2 \cdot (t_{s2v} - \delta)/(1 + \varepsilon_f)$, then select candidates for *Case D* and *Case E* by applying the following steps.

2.1 Let t_{r-U} be the upper bound of t_r, and repeat **2.2.1** for the largest and smallest values of W_n.

2.2.1 Given (t_{r-U}, t_f, W_n), calculate t_w by (1) or (2), and for (t_{r-U}, t_w, t_f, W_n, $W_p = a \cdot W_n + b$) compute RPVs for all 270 cases. By sorting these RPVs, select top and bottom 10 cases.

2.2 By checking top 20 cases, chose candidates for *Case E*.

2.3 By checking bottom 20 cases, chose candidates for *Case D*.

Step 3: Seek an optimal pair (t_r, W_n) satisfying (5) and (6) by applying the following steps.

3.1 Let t_{r-L} and t_{r-U} be the lower and upper bounds of t_r, respectively.

3.2 While $t_{r-U} - t_{r-L}$ is not smaller than a specified limit, set $t_r = (t_{r-U} + t_{r-L})/2$, and conduct the following to find W_n satisfying (5).

3.2.1 Compute t_w by (1) or (2) for t_r and t_f.

3.2.2 For (t_r, t_w, t_f), calculate the maximum value W_{n-max} of W_n which makes RPV equal to $100 + B$[%] with the use of candidates for *Case E*.

3.2.3 For (t_r, t_w, t_f), calculate the minimum value W_{n-min} of W_n which makes RPV equal to $100 - B$[%] with the use of candidates for *Case D*.

3.2.4 Replace t_{r-L} or t_{r-U} by t_r so that W_n satisfying (5) exists in between t_{r-L} and t_{r-U}.

Step 4: From 3-tuple (t_r, t_f, W_n) obtained in **Steps 2** and **3**, calculate 5-tuple (t_r, t_w, t_f, W_p, W_n) which determines the sizes of sampling switch and the waveform of SMP pulse.

4. Experimental Results

In order to see the validity and the effectiveness of the proposed procedure, it was applied to a sampling switch of a column driver which has been designed in manual already. The manual design was done as follows: For a pre-designed

Delay-Buffer, the case of minus feeding is selected to determine W_n, and W_n is set so that RPV becomes larger than 99.5% at the time when t_w ends, that is, before charge injection starts. Then, by using the case of plus feeding, W_p is determined so as to reduce the voltage change ΔV_{px} due to charge injection, within the range such that RPV at the time when t_w ends is larger than 99.5%. Hence, the manually designed circuit has the same topology as the column driver considered in this experiment, and has different transistor sizes.

Since the double sampling was used in the manual design, Eq. (2) was used in the procedure. The values of (t_r, t_f, W_{n-max}) and (t_r, t_f, W_{n-min}) for this sampling switch are shown in Fig. 4, where the limit B is set to 1.8. CPU times for **Steps 1**, **2**, and **3** were 10 min, 30 min, and 15 min, respectively, by Sun Blade 2000 computer and Smart SPICE [14].

The values of W_n and W_p obtained by our procedure have been reduced by 28% and 20%, respectively, in comparison with those obtained by manual design, although t_f and t_r were not changed. As a result, the load of Delay-Buffer was lightened so that the total power consumption can be reduced. In fact, after designing Delay-Buffer by the method in [13], the total power consumptions were computed for all 270 cases of combinations of feeding types and fluctuations. Then, the average power reduction was found to be 18%. This reduction was achieved by reducing the total transistor sizes of Delay-Buffer, which was enabled by the reduction of W_n and W_p.

RPVs were also evaluated for all 270 cases so as to check the robustness of the column driver designed by using our procedure. The histograms of RPVs obtained by our design procedure and by manual design are shown in Fig. 6, where most of the objectives set up for RPVs have been achieved by our procedure, but in manual design there occur the cases in which the constraints for RPV are not satisfied due to the insufficient treatment of charge injection. Strictly speaking, the percentage of the RPVs within 100±1% among 270 cases of fluctuations was 88.1% in our design, but 46.7% in the manual design.

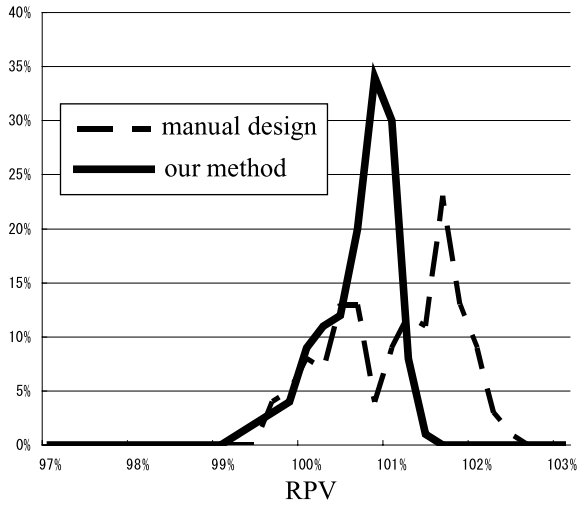

Fig. 6 Histograms of RPVs.

The same driver was redesigned in a different technology with larger mobility of SPICE parameters of nMOS and pMOS TFTs. Then, smaller W_n and larger t_r were obtained so that the average of the total power consumption could be reduced by 30% and the percentage of the RPVs within 100±1% among 270 cases of fluctuations was increased to 100%.

If we want to use an optimizer such as the one provided in Smart SPICE [14] to design the same sampling switch, we must input 270 different sets of parameters which represent 270 cases of fluctuations. In order to compare our procedure to the Smart SPICE optimizer, we input these parameters and optimized the values of t_r, W_n, and W_p so as to make RPVs 100%. Then, we obtained smaller W_n and W_p than those obtained by our procedure, but t_r became the minimum possible value which makes the design of Delay-Buffer hard. Moreover, it took 3.5 hours by Windows machine, DELL DIMENSION 9150 Pentium4 3.2 GHz, which is 2 times faster than Sun Blade 2000. Therefore, we can see that our procedure optimizes both sampling switch and sampling pulse simultaneously within a practical time.

In order to check whether W_n and W_p obtained by our procedure are optimum, we conducted the Smart SPICE optimizer by setting t_r to the value obtained by our procedure. Then, W_n and W_p became larger by 5% and 10%, respectively, than our results after 3 hours run on the Windows machine. Hence, we can see that our procedure finds appropriate sampling switch sizes in a shorter time.

5. Conclusions

In this paper, we proposed a practical design procedure dedicatedly for the sampling switch of active matrix LCDs, which satisfies the required constraint for RPV, the Ratio of Pixel voltage to Video voltage. To do this, we first analyzed how the design parameters of sampling switch and sampling pulse are related to the RPV, and then sought a minimal number of parameters which contribute most to the behavior of RPV. By selecting two most proper design parameters from 5 original parameters, we could truncate the solution space of design parameters to be explored, so that we can reduce the number of SPICE simulations. Hence, the proposed procedure could optimize sampling switch sizes and a sampling pulse waveform with the use of a full transistor model by taking various fluctuations into account.

Experimental results show that an optimal sampling switch attained by this procedure gives rise to a column driver with almost 20% less power consumption than the one by manual design. The time needed to obtain an optimal solution was around 1 hour, since various fluctuations were taken into consideration. However, the proposed design procedure provides a useful tool which contributes to the design automation of column drivers.

The main drawback is that Delay-Buffer and the sampling switch are considered separately. If Delay-Buffer can-

not be designed so as to generate SMP and SMPB with t_r and t_f specified by the proposed procedure, then the proposed procedure must be re-executed for a little larger value of B. Therefore, devising a procedure to design the sampling switch and the delay-buffer circuit simultaneously is a remaining future work. Development is continuing on constructing a full set of design tools for column drivers.

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