IEICE TRANSACTIONS

on Fundamentals of Electronics, Communications and Computer Sciences

VOL. E103-A NO. 12
DECEMBER 2020

A PUBLICATION OF THE ENGINEERING SCIENCES SOCIETY
The Institute of Electronics, Information and Communication Engineers
Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3 chome, Minato-ku, TOKYO, 105-0011 JAPAN

PAPER Special Section on VLSI Design and CAD Algorithms

A Fault Detection and Diagnosis Method for Via-Switch Crossbar in Non-Volatile FPGA

Ryutaro DOI[†a)], ***Student Member***, **Xu BAI**[††], ***Member***, **Toshitsugu SAKAMOTO**[††], ***Nonmember***, ***and*** **Masanori HASHIMOTO**[†b)], ***Member***

SUMMARY FPGA that exploits via-switches, which are a kind of non-volatile resistive RAMs, for crossbar implementation is attracting attention due to its high integration density and energy efficiency. Via-switch crossbar is responsible for the signal routing in the interconnections by changing on/off-states of via-switches. To verify the via-switch crossbar functionality after manufacturing, fault testing that checks whether we can turn on/off via-switches normally is essential. This paper confirms that a general differential pair comparator successfully discriminates on/off-states of via-switches, and clarifies fault modes of a via-switch by transistor-level SPICE simulation that injects stuck-on/off faults to atom switch and varistor, where a via-switch consists of two atom switches and two varistors. We then propose a fault diagnosis methodology for via-switches in the crossbar that diagnoses the fault modes according to the comparator response difference between the normal and faulty via-switches. The proposed method achieves 100% fault detection by checking the comparator responses after turning on/off the via-switch. In case that the number of faulty components in a via-switch is one, the ratio of the fault diagnosis, which exactly identifies the faulty varistor and atom switch inside the faulty via-switch, is 100%, and in case of up to two faults, the fault diagnosis ratio is 79%.

key words: *via-switch, non-volatile FPGA, crossbar, fault diagnosis*

1. Introduction

Field programmable gate arrays (FPGAs) are gaining their popularity because of the lower development cost than application specific integrated circuits (ASICs). However, conventional FPGAs are still inferior to ASICs regarding operating speed and power consumption [1], [2]. These drawbacks originate from a large number of static random access memory (SRAM)-based programmable switches that are equipped in FPGAs to acquire reconfigurability. To overcome the drawbacks of conventional FPGAs, FPGAs that utilize via-switches, which are a kind of resistive RAMs (RRAMs), as programmable switches instead of SRAM-based ones are drawing attention due to their higher integration density and energy efficiency [3]–[5]. In the via-switch FPGA, the crossbar, which has a via-switch at each intersection of horizontal and vertical interconnections, is responsible for the signal routing by changing on/off-states of via-switches. Meanwhile, for ensuring arbitrary routings at FPGA user side, the via-switch FPGA manufacturer needs to verify the via-switch crossbar functionality before the shipment. For this verification, fault testing that checks whether we can turn on/off via-switches normally is essential. However, testing of via-switch FPGA has not been studied so far.

This work is the first one to investigate the fault testing and diagnosis of via-switch crossbar*. We confirm that a general differential pair comparator successfully discriminates on/off-states of via-switches, and clarify fault modes of a via-switch using transistor-level SPICE simulation that injects stuck-on/off faults to atom switch and varistor, where a via-switch consists of two atom switches and two varistors. We then propose a fault diagnosis methodology for via-switches in the crossbar that diagnoses the fault modes according to the comparator response difference between the normal and faulty via-switches. The additional circuit required for the proposed fault testing method is only one comparator for one chip, and hence the area overhead is negligible. Besides, we can check the via-switch fault by programming each via-switch only once. The proposed method achieves 100% fault detection by checking the comparator responses after turning on/off the via-switch. In case that the number of faulty components in a via-switch is up to two, the successful ratio of the fault diagnosis, which exactly identifies the faulty varistor and atom switch inside the faulty via-switch, is 79%. The fault diagnosis ratio reaches 100% in case that there is up to one faulty component in a via-switch.

2. Via-Switch FPGA

2.1 Via-Switch

The via-switch is a non-volatile, rewritable, and compact switch that is developed to implement a crossbar switch by Banno et al. [7], and it is composed of atom switches and varistors. Here, we explain the device structure, functionality, and characteristics in the following.

The atom switch consists of a solid electrolyte sandwiched between copper (Cu) and ruthenium (Ru) electrodes as shown in Fig. 1(a). By applying a positive voltage to the Cu electrode, a Cu bridge is formed in the solid electrolyte, and the switch turns on and becomes low resistance state.

Manuscript received March 11, 2020.
Manuscript revised July 14, 2020.

[†]The authors are with the Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University, Suita-shi, 565-0871 Japan.
[††]The authors are with the NEC Corporation, Kawasaki-shi, 211-8666 Japan.
a) E-mail: doi.ryutaro@ist.osaka-u.ac.jp
b) E-mail: hasimoto@ist.osaka-u.ac.jp

DOI: 10.1587/transfun.2020VLP0005

*A preliminary version of this work is presented in [6].

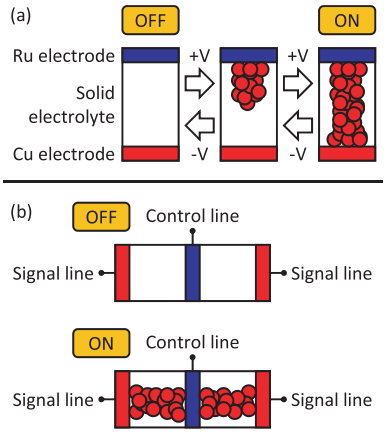


Fig. 1 Structure and operation of (a) atom switch and (b) CAS.

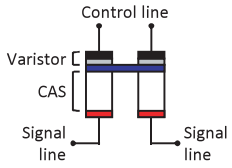


Fig. 2 Via-switch structure.

On the other hand, when a negative voltage is applied, Cu atoms in the bridge are reverted to the Cu electrode, and then the switch turns off and becomes high resistance state. The switching between the on-state and off-state is repeatable, and each state is non-volatile [8]. For improving the device reliability, the complementary atom switch (CAS) is devised [9], where it consists of two atom switches connected in series with opposite direction as shown in Fig. 1(b). In programming a CAS, a pair of signal line and control lines supply a programming voltage to each atom switch, and two atom switches are programmed sequentially. During normal operation, on the other hand, only signal lines are used for routing [10].

To accurately provide the programming voltage only to the target atom switch in a switch array, the varistor is introduced into the via-switch. Figure 2 shows the structure of via-switch, where the varistor is connected to the control terminal of CAS. When a voltage higher than the threshold value (programming voltage) is applied between a signal line and a control line, the varistor supplies programming current to an atom switch. On the other hand, the varistor isolates the control lines from the signal lines during normal operation [7].

Here, the main features of via-switches are summarized. The footprint, on-resistance, and capacitance are 18 F^2, 200 Ω, and 0.14 fF respectively [3], [7]. Thanks to these characteristics, the area efficiency and performance of via-switch FPGA are dramatically improved compared to SRAM-based one. Ochi et al. report that the crossbar density is improved by 26x, and the delay and energy in the interconnection are reduced by 90% or more at 0.5 V operation [3]. Also, Hashimoto et al. achieve 12 times

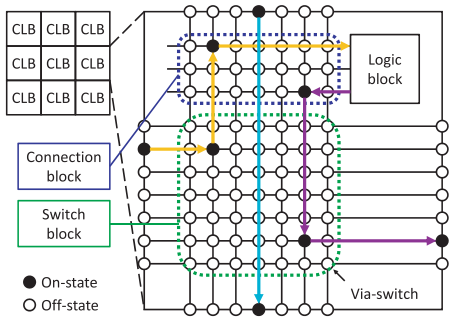


Fig. 3 Structure of via-switch FPGA.

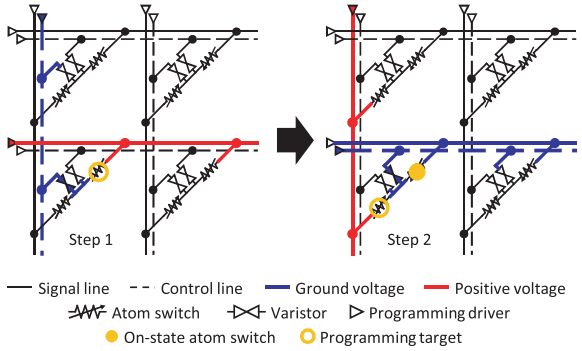


Fig. 4 Via-switch based crossbar structure and switch programming steps.

higher area efficiency in a fabricated chip [5]. A via-switch can be reprogrammed about 1,000 times [10]. Therefore, the fault testing method with a small number of reprogramming is desirable for maximizing the number of reprogramming at the FPGA user side after the shipment. The proposed method programs each via-switch only once as detailed in Sect. 4.

2.2 Via-Switch FPGA

The structure of via-switch FPGA is an array of configurable logic blocks (CLBs), and each CLB is composed of a logic block and a crossbar where a via-switch is placed at each intersection of signal lines as shown in Fig. 3 [3]. The via-switch in the crossbar is responsible for connection and disconnection between the horizontal and vertical signal lines. Besides, the top half of the crossbar serves as input and output multiplexers to the logic block and corresponds to the connection block in conventional FPGAs. On the other hand, the bottom half of the crossbar, which corresponds to the switch block, routes global interconnections. The logic block organizes combinational and sequential circuits.

Figure 4 illustrates the via-switch based crossbar structure and switch programming steps. Both signal and control lines are aligned horizontally and vertically. Figure 4 exemplifies programming steps in 2x2 crossbar where an atom switch is turned on at each step. A pair of the perpendicular signal and control lines crossing at the via-switch of inter-

est are used for switch programming. Two programming drivers are activated at each step, and a positive voltage is given to one of the signal lines, and a ground voltage is given to one of the control lines. Other lines are floated. We can see that the via-switch at the bottom left is successfully turned on at steps 1 and 2.

3. Fault Mode Analysis of Via-Switch

To verify the via-switch crossbar functionality after manufacturing, fault testing that checks whether via-switches can be securely turned on and off is indispensable. Aiming at developing a fault testing method, Sect. 3.1 first analyzes fault modes of a via-switch and confirms that a general comparator can distinguish on/off-states of via-switches in the crossbar. Section 3.2 then investigates and identifies fault modes of a via-switch by transistor-level SPICE simulation. Based on the discussion in this section, the next section will propose a fault diagnosis method.

3.1 Discriminating Via-Switch On/Off-States with Comparator

To discriminate via-switch on/off-states in the crossbar, this work adds a differential pair comparator that connects to every programming driver through a transistor switch as shown in Fig. 5. This figure illustrates the connection between the comparator, programming drivers, an array that contains four 2x2 crossbars. Here, all the crossbars can share the programming driver by using NMOS pass transistors while Fig. 4 depicts a driver for each wire. The comparator can also be shared by all the crossbars. Therefore, the proposed fault testing method is feasible by adding only one comparator, and the peripheral circuit for testing is negligibly small for a practically large CLB array.

The read operation applies a voltage to the target atom switch in the same manner as programming operation and turns on only the transistor switch that connects the comparator with the driver that is outputting a ground voltage, which is illustrated in Fig. 5. In this read operation, the comparator observes the voltage drop in the target atom switch and compares it with a given reference voltage. Here, the applied voltage in the read operation is lower than the programming voltage, and therefore this operation never changes the on/off-states of the target switch. By giving an appropriate reference voltage that makes the comparator output different depending on the on/off-states of the target switch, the comparator can read the switch states. The reference voltage is provided as an analog voltage from a large scale integration (LSI) tester outside the chip. In this read method, two programming drivers apply the voltage to a pair of an atom switch and a varistor, and therefore this work calls this operation as atom switch-varistor read (ASV-read) operation.

Table 1 summarizes the comparator output simulated by transistor-level SPICE simulation in both cases that the target atom switch is on-state and off-state varying the reference voltage. In this work, the crossbar size is set to 90x127 for practical use. Table 1 shows that the comparator output changes from 0 to 1 according to an increase in the reference voltage, and the reference voltage at the boundary between 0 and 1 differs depending on the on/off-states of the target atom switch. The boundary reference voltage for the on-state atom switch is higher than that for off-state atom switch, and the voltage difference is about 50 mV as shown in the row of ASV-read in Table 2. General LSI testers can provide the analog voltage with millivolt accuracy, and therefore the comparator can discriminate the on/off-states by exploiting the boundary difference between on and off states. For example in Table 1, the atom switch state can be distinguished by choosing 0.56 V as the reference voltage.

In addition to the above ASV-read, this work introduces two read methods, namely complementary atom switch read (CAS-read) operation and two varistors read (TVR-read) operation. CAS-read applies a read voltage to the CAS by activating a pair of drivers that drive the perpendicular two signal lines crossing at the target intersection. On the other hand, TVR-read uses perpendicular two control lines to apply a read voltage to two varistors connected in series in a via-switch. Figure 6 illustrates each path to apply a read voltage in ASV-read, CAS-read, and TVR-read.

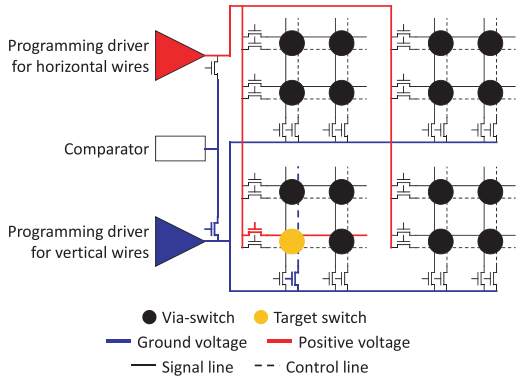


Fig. 5 Connection between comparator, programming drivers, and crossbar array.

Table 1 Comparator output when reference voltage is varied in read operation of atom switch.

Reference voltage [V]	Comparator output	
	Atom switch is on	Atom switch is off
0.50	0	0
0.52	0	0
0.54	0	1
0.56	0	1
0.58	0	1
0.60	1	1

Table 2 Boundary reference voltage in ASV-, CAS-, and TVR-read.

Read type	Target switch state	
	On-state	Off-state
ASV-read	0.58 V	0.53 V
CAS-read	0.70 V	0.53 V
TVR-read	0.58 V	0.58 V

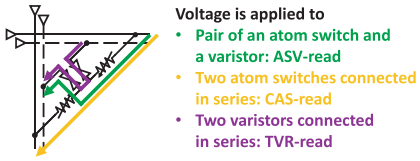


Fig. 6 Path to apply read voltage in ASV-, CAS-, and TVR-read.

Here, this work does not use the signal path using parallel signal and control lines at the target intersection, where the signal also passes through an atom switch and a varistor, due to the sneak path problem. In both CAS-read and TVR-read, one driver gives a positive voltage and the other applies a ground voltage. Both the operations turn on only the transistor switch that connects the comparator with the driver outputting a ground voltage such that the voltage of interest is delivered to the comparator. The applying voltage in CAS-read is lower than the programming voltage. On the other hand, in TVR-read, the drivers apply a voltage of the same level as the programming voltage to check the varistors state correctly.

The SPICE simulation has confirmed that the comparator response in CAS-read is similar to ASV-read except for the absolute value of the reference voltage. The comparator output changes from 0 to 1 as the reference voltage elevates, and the boundary reference voltage for the on-state CAS is higher than that for off-state CAS, where on-state CAS and off-state CAS mean both of atom switches in the CAS are on-state and off-state, respectively. The row of CAS-read in Table 2 shows the values of the boundary reference voltage. The SPICE simulation also confirms that the comparator response for a CAS containing one on-state atom switch and one off-state atom switch is the same as the response to off-state CAS. Meanwhile, the boundary in TVR-read does not change regardless of on/off-states of atom switches as shown in Table 2 since there is no atom switch in the signal path in TVR-read.

ASV-read uses both an atom switch and a varistor, whereas CAS-read uses only atom switches and TVR-read uses only varistors. By combining the comparator responses in these three read operations, this work can improve the fault diagnosis capability. The details will be explained in Sect. 4.

3.2 Via-Switch Fault Modes

This subsection discusses how the comparator response varies when a via-switch includes faulty atom switch or varistor. This work injects stuck-on/off faults to atom switch and varistor, and evaluates the comparator response by SPICE simulation. Here, stuck-on/off faults mean that the two terminals of atom switch or varistor are shorted/opened.

First, this paragraph studies the case where the atom switch is stuck-on/off. When an atom switch is stuck-on, the boundary reference voltage is unchanged from the non-faulty on-state case even after the drivers apply a programming voltage to turn off the atom switch. Then, this observation indicates that there is a fault. The same discussion holds for the stuck-off case. The CAS can be in a state where one atom switch is on-state and the other is off-state in addition to the states that both atom switches are on-state or off-state. As mentioned in the previous subsection, when at least one atom switch is stuck-off in a CAS, the boundary reference voltage is identical to the boundary of CAS-read for off-state CAS. Stuck-on/off faults of atom switches do not affect the boundary in TVR-read as explained in the previous subsection.

Table 3 Boundary reference voltage in ASV- and CAS-read with faulty varistor.

Read type	Target switch state	Varistor fault type	
		Stuck-on	Stuck-off
ASV-read	On-state	0.77 V	0.53 V
	Off-state	0.53 V	0.53 V
CAS-read	On-state	0.70 V	0.70 V
	Off-state	0.53 V	0.53 V

Table 4 Boundary reference voltage in TVR-read with normal and faulty varistors.

Varistors state	Boundary reference voltage
No fault	0.58 V
If either varistor is stuck-off	0.53 V
Else if either varistor is stuck-on	0.72 V

Next, the following discusses the case where the varistor is stuck-on/off. Table 3 summarizes the boundary reference voltage in ASV-read and CAS-read with faulty varistor. Focusing on ASV-read with stuck-on varistor in Table 3, the boundary for the on-state switch changes from that of the normal case, specifically from 0.58 V in Table 2 to 0.77 V in Table 3. Therefore, this observation can know there is a fault. On the other hand, when reading the off-state atom switch, the boundary is the same for normal and stuck-on cases. In ASV-read with stuck-off varistor, the boundary is fixed to 0.53 V, which is the boundary in the normal case with off-state switch, regardless of on/off-states of the target switch.

The row of CAS-read in Table 3 indicates that the boundary reference voltage for faulty varistor does not change from the normal case. The CAS-read operation applies a read voltage only to the CAS, and hence stuck-on/off faults of the varistor do not affect the comparator response.

Table 4 shows the boundary reference voltage of TVR-read in normal and faulty cases. When either varistor in a via-switch is stuck-off, the boundary voltage drops from the normal boundary. On the other hand, when both varistors are not stuck-off and either varistor is stuck-on, the boundary voltage rises compared to the normal case.

This work utilizes these differences in the boundary reference voltage between normal and faulty cases for the fault diagnosis method proposed in the next section. It should be noted that the comparator response for a via-switch with multiple faulty components is a combination of the above fault modes.

4. Proposed Fault Diagnosis Method

This section proposes a fault diagnosis method for the via-switch crossbar exploiting the comparator response difference between normal and faulty via-switches explained in the previous section. First, Sect. 4.1 clarifies prerequisites in the proposed method. Then, Sect. 4.2 proposes a fault diagnosis method.

4.1 Prerequisites

The proposed method assumes the following prerequisites.

- Even when a varistor is stuck-on, the drivers can program the corresponding atom switch normally. This can be achieved by a current-limiting circuit that restricts the programming current appropriately.
- When a varistor is stuck-off, the drivers cannot program the corresponding atom switch since the programming current cannot be provided to the target atom switch.
- Initial state of non-faulty atom switch is off-state, which is a feature of via-switch.
- There is no fault in the comparator, programming drivers, and interconnect wires.

4.2 Fault Diagnosis

This subsection proposes a fault diagnosis method that identifies faulty components in a via-switch on the crossbar. The proposed method utilizes the difference of the boundary reference voltage of the comparator in read operation discussed in Sect. 3.

The proposed method enumerates all the combinations of stuck-on/off faults of two atom switches and two varistors in a via-switch. Then, the proposed method makes a look-up table beforehand that summarizes the boundary reference voltage of ASV-read, CAS-read, and TVR-read after turning on/off the target switch for each fault combination. When actually diagnosing faults in a via-switch, the proposed method investigates the boundary of three read operations after programming the target switch, performs a pattern matching with the look-up table prepared above, and identifies the faults.

Table 5 enumerates all the patterns of comparator response when the number of faulty components in a via-switch is up to two, which correspond to the left half of the table. A via-switch has four components and each component can be stuck-on/off. Then, supposing the number of faulty components is n, the number of combinations of fault components is given by ${}_4\mathrm{C}_n \times 2^n$. Therefore, the number of combinations in case of up to n faulty components can be calculated by $\sum_{k=0}^{n} {}_4\mathrm{C}_k \times 2^k$. When n is 2, there are 33 combinations listed in Table 5.

The proposed method performs ASV-read operations for both cases after turning on and off the target atom switch, where this operation corresponds to “US”/“LS” and “UR”/“LR” in Table 5, respectively. For example, “US” and “LR” stand for “Upper atom switch is Set” and “Lower atom switch is Reset”, respectively. For a CAS, there are four combinations to turn on (S) and off (R) both upper and lower atom switches, and hence the proposed method evaluates the boundary reference voltage in all four cases, which are “SS”, “SR”, “RS”, and “RR” in Table 5. The proposed method also uses TVR-read operation in the proposed method. For each via-switch, the above read operations can be attained by reprogramming the via-switch only once. The following steps exemplify a procedure of read operations.

1. Initial state of upper and lower atom switches is (upper: off-state, lower: off-state).
2. Turn on the upper atom switch [switch state is (on, off)].
3. Perform the upper ASV-read operation (“US”).
4. Perform the CAS-read operation (“SR”).
5. Turn on the lower atom switch [switch state is (on, on)].
6. Perform the lower ASV-read operation (“LS”).
7. Perform the CAS-read operation (“SS”).
8. Turn off the upper atom switch [switch state is (off, on)].
9. Perform the upper ASV-read operation (“UR”).
10. Perform the CAS-read operation (“RS”).
11. Turn off the lower atom switch [switch state is (off, off)].
12. Perform the lower ASV-read operation (“LR”).
13. Perform the CAS-read operation (“RR”).
14. Perform the TVR-read operation.

There are six characters that represent the state of the boundary reference voltage in Table 5. “N” means that the component has no fault and the boundary is normal. When there are faulty components but the boundary is the same as normal, it is expressed as “M”, e.g., when the comparator reads a stuck-on switch after turning on the switch. When the boundary is expected to be that of the off-state switch but is the same as the on-state switch, this work categorizes this case as “H”. For example, “H” arises when the comparator reads a stuck-on switch after turning off the switch. “L” is the opposite situation to “H”. “R” and “D” correspond to the cases that the boundary rises and drops from the normal, respectively. After obtaining the pattern of these six characters with ASV-read of upper and lower atom switches, CAS-read, and TVR-read, the proposed method diagnoses faulty components in a via-switch.

The following paragraphs discuss fault detectability and diagnosability. Here, the fault detection only evaluates whether the via-switch has faulty components, while the fault diagnosis identifies faulty components in the via-switches and their fault types. First, this paragraph evaluates fault detectability. The ASV-read of an upper atom switch uses the upper atom switch and the lower varistor. Here, ID #1-9 in Table 5 cover all combinations of non-faulty and stuck-on/off upper atom switch and lower varistor. In this case, the response of the ASV-read, which corresponds to the column of “U-ASV”, becomes (“N”, “N”) only

Table 5 Comparator response difference and diagnosability in case of up to two faulty components in a via-switch.

ID	Fault states of via-switch components												Read operation results									Diag.	
	Upper VR			Lower AS			Lower VR			Upper AS			U-ASV		L-ASV		CAS				TVR	1F	2F
	NF	SN	SF	NF	SN	SF	NF	SN	SF	NF	SN	SF	US	UR	LS	LR	SS	SR	RS	RR			
1	✓			✓			✓			✓			N	N	N	N	N	N	N	N	N	Yes	Yes
2	✓			✓			✓				✓		M	H	N	N	M	M	H	M	N	Yes	Yes
3	✓			✓			✓					✓	L	M	N	N	L	M	M	M	N	Yes	Yes
4	✓			✓				✓		✓			R	M	N	N	N	N	N	N	R	Yes	Yes
5	✓			✓				✓			✓		R	R	N	N	M	M	H	M	R	—	Yes
6	✓			✓				✓				✓	L	M	N	N	L	M	M	M	R	—	Yes
7	✓			✓					✓	✓			L	M	N	N	L	M	M	M	D	Yes	No[1]
8	✓			✓					✓		✓		L	M	N	N	M	M	H	M	D	—	Yes
9	✓			✓					✓			✓	L	M	N	N	L	M	M	M	D	—	No[1]
10	✓				✓		✓			✓			N	N	M	H	M	H	M	M	N	Yes	Yes
11	✓				✓		✓				✓		M	H	M	H	M	H	H	H	N	—	Yes
12	✓				✓		✓					✓	L	M	M	H	L	M	M	M	N	—	Yes
13	✓				✓			✓		✓			R	M	M	H	M	H	M	M	R	—	Yes
14	✓				✓				✓	✓			L	M	M	H	L	M	M	M	D	—	Yes
15	✓					✓	✓			✓			N	N	L	M	L	M	M	M	N	Yes	Yes
16	✓					✓	✓				✓		M	H	L	M	L	M	M	M	N	—	Yes
17	✓					✓	✓					✓	L	M	L	M	L	M	M	M	N	—	Yes
18	✓					✓		✓		✓			R	M	L	M	L	M	M	M	R	—	Yes
19	✓					✓			✓	✓			L	M	L	M	L	M	M	M	D	—	No[2]
20		✓		✓			✓			✓			N	N	R	M	N	N	N	N	R	Yes	Yes
21		✓		✓			✓				✓		M	H	R	M	M	M	H	M	R	—	Yes
22		✓		✓			✓					✓	L	M	R	M	L	M	M	M	R	—	Yes
23		✓		✓				✓		✓			R	M	R	M	N	N	N	N	R	—	Yes
24		✓		✓					✓	✓			L	M	R	M	L	M	M	M	D	—	Yes
25		✓			✓		✓			✓			N	N	R	R	M	H	M	M	R	—	Yes
26		✓				✓	✓			✓			N	N	L	M	L	M	M	M	R	—	Yes
27			✓	✓			✓			✓			N	N	L	M	L	M	M	M	D	Yes	No[3]
28			✓	✓			✓				✓		M	H	L	M	L	M	M	M	D	—	Yes
29			✓	✓			✓					✓	L	M	L	M	L	M	M	M	D	—	No[2]
30			✓	✓				✓		✓			R	M	L	M	L	M	M	M	D	—	Yes
31			✓	✓					✓	✓			L	M	L	M	L	M	M	M	D	—	No[2]
32			✓		✓		✓			✓			N	N	L	M	M	H	M	M	D	—	Yes
33			✓			✓	✓			✓			N	N	L	M	L	M	M	M	D	—	No[3]

VR: varistor, AS: atom switch, NF: no fault, SN/SF: stuck-on/off
U-ASV/L-ASV: ASV-read of upper/lower atom switch
US/UR/LS/LR: read after turning on/off/on/off upper/upper/lower/lower atom switch
SS/SR/RS/RR: read after turning on/on/off/off upper atom switch and turning on/off/on/off lower atom switch
N: normal response, M: fault is masked, H/L: boundary is the same as on-state/off-state switch, R/D: boundary rises/drops
Diag.: diagnosability, 1F/2F: up to one/two faulty components in a via-switch
Rows that have the same superscript number of "No" in diagnosability column share the same comparator response.

when both upper atom switch and lower varistor have no fault. The response of the remaining eight cases is different from ("N", "N"). By utilizing this difference, the proposed method can detect whether a pair of upper atom switch and lower varistor are faulty. The same discussion holds in the ASV-read of lower atom switch with the upper varistor. Therefore, the proposed method can achieve 100% fault detection of a via-switch by using ASV-read for both upper and lower atom switches.

On the other hand, in terms of fault diagnosability, the above observation cannot identify the faulty components in a via-switch uniquely only with the ASV-read. The column of "U-ASV" in Table 5 indicates that ID #3 and 6-9 have the same response of ("L", "M"), and hence ASV-read cannot distinguish these patterns. This is mainly because the boundary reference voltage of ASV-read for stuck-off varistor is fixed to that in the normal case explained in Sect. 3. For improving fault diagnosability, the proposed method combines the responses of ASV-read, CAS-read, and TVR-read. The column of "Diag." shows that fault diagnosability using these three read methods in cases that there are up to one and up to two fault components in a via-switch. When the comparator response is unique in the table, the corresponding fault is diagnosable. The table demonstrates that the proposed method can identify the fault component perfectly when there is up to one fault component in a via-switch. When there are up to two faulty components, the diagnosability ratio is $26/33 \times 100 = 79\%$. On the other hand, when only AVS-read is used, this ratio decreases to 33%. CAS-read and TVR-read help elevate the fault diagnosability by 46%.

Table 6 summarizes the fault diagnosis ratio when the maximum number of faulty components in a via-switch is varied from 1 to 4. When the maximum number of fault is 1, the proposed method can discriminate the faulty component and fault type no matter which component is stuck-on/off. The table also indicates that the diagnosis ratio diminishes as the maximum number of faulty components increases. This is because the number of fault patterns that have the same response of read operations increases. Fortunately, the probability that there are 3 or 4 faulty components in a via-switch is low. The next section discusses a relation between the number of faulty components and the fault rate of via-switch components in a practically-sized crossbar,

Table 6 Diagonosable faults ratio.

Maximum number of faults	Number of fault patterns	Number of diagnosable patterns	Diagnosis ratio [%]
1	9	9	100
2	33	26	79
3	65	34	52
4	81	34	42

and confirms that the proposed method is effective for practical use.

5. Discussion

5.1 Relation between the Fault Rate and the Number of Faulty Components

This subsection investigates the relation between a fault rate of via-switch components, a percentage of faulty via-switches, and the number of faulty components in a via-switch in a practical-sized crossbar. Then, this subsection confirms that identifying the faulty component in via-switches where there is one faulty component in the via-switch is the most important in the crossbar for practical use, and, from this point of view, the proposed method is suitable.

Figure 7 shows a percentage of faulty via-switches in a 100x100 crossbar when a fault rate of via-switch components is varied from 0.01 to 0.25. This evaluation randomly injects faults assuming that four components in a via-switch have the same fault rate, and plots the average value of 10,000 trials. Note that the fault rates of via-switches may have spatial correlation, but it is not considered here since there is not measurement data enough to discuss the spatial correlation yet. This figure also categorizes faulty via-switches according to the number of faulty components. We can see that the number of via-switches with multiple faulty components increases when the fault rate is 0.25. However, in this case, the percentage of faulty via-switches in the crossbar is close to 70%, i.e., only 30% of the via-switches can be used for programming, and such a crossbar can no longer be used in practice. On the other hand, as the manufacturing technology of the via-switch matures, the fault rate is expected to decrease. When the fault rate of each component is 0.05, the percentage of faulty via-switches becomes less than 20%. Figure 7 demonstrates that via-switches with a single faulty component are dominant, especially when the fault rate is low. Therefore, in the crossbar that has a practical percentage of faulty via-switches, it is important to identify the faulty component in via-switches that have only one faulty component.

Next, this paragraph evaluates how the percentage of diagnosable via-switches in a 100x100 crossbar changes when the supposed maximum number of faulty components in a via-switch varies. Figure 8 shows the evaluation result. In case of lower fault rates, the highest diagnosability can be achieved by supposing that there is up to one fault in a via-switch. For example, the percentage of diagnosable

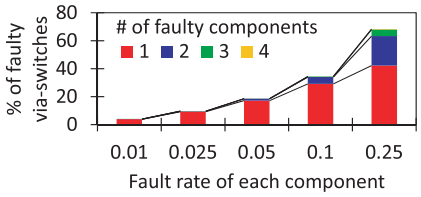


Fig. 7 Percentage of faulty via-switches in 100x100 crossbar when fault rate of each component in a via-switch varies.

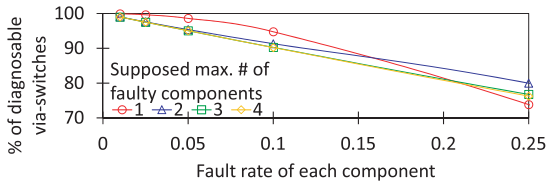


Fig. 8 Percentage of diagnosable via-switches in 100x100 crossbar when the fault rate of each component in a via-switch and the supposed maximum number of faulty components are varied.

via-switches is 99% when the fault rate is 0.05. The result also indicates that it is better to suppose multiple faults in a via-switch and diagnose faulty components when the fault rate becomes high.

The high diagnosability of the proposed method is useful for yield analysis. In novel devices such as via-switches, it is important to investigate the cause of faults in detail for improving the yield. The proposed method can identify which component is faulty and also discriminate the fault type with high diagnosability. Therefore, the proposed method helps the manufacturer to increase the yield rate. Besides, the proposed method also contributes to the efficient use of programmable resources. This is because, even when a crossbar has faulty via-switches, it is possible to utilize the same crossbar normally by identifying faulty switches with the proposed method and avoiding the faulty part with sophisticated signal routings.

5.2 Effect of Variation

The discussion above has supposed that the resistances of stuck-on/off atom switch and varistor are fixed to certain values. On the other hand, the resistance value is anticipated to vary due to device variation and programming condition in practice. This subsection evaluates the boundary reference voltage under the variation and confirms that the proposed method is available even in such a case.

First, we evaluate the boundary reference voltage when the resistance of a stuck-on atom switch varies. Figure 9 shows the evaluation result obtained with SPICE simulations. We can see that the boundary reference voltage depends on the on-resistance of the atom switch. On the other hand, even when the on-resistance varies from 1 kΩ to 10 kΩ, the voltage difference between on and off states is still tens of millivolts. As explained in Sect. 3.1, general LSI testers have millivolt accuracy to provide the analog voltage, and hence the comparator can distinguish between the on

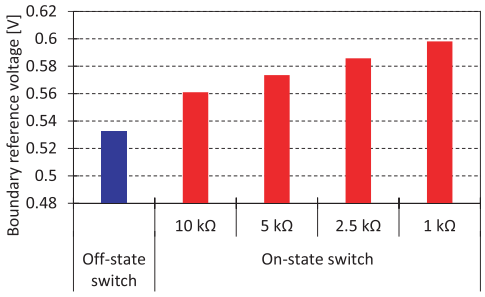


Fig. 9 Boundary reference voltage in ASV-read in case that on-resistance of atom switch is varied.

Table 7 Boundary reference voltage in TVR-read with stuck-on varistor under resistance variation.

Varistor resistance	Boundary reference voltage
-50%	0.7250 V
Typical	0.7235 V
+50%	0.7214 V

and off states correctly.

In the same manner, we evaluate the variation effect of the resistances of a stuck-off atom switch and stuck-on/off varistors. Table 7 shows the boundary reference voltage in TVR-read when the resistance value of stuck-on varistor increases or decreases by 50% from the typical value used so far. We can see that the variation effect on the boundary reference voltage is limited. There is a significant difference of the boundary voltage between stuck-on varistor and no fault or stuck-off varistor, which is found by comparing Table 7 and Table 4. We have confirmed that in the other cases, i.e., when the resistances of a stuck-off atom switch and a stuck-off varistor vary, the boundary reference voltage is almost unchanged, and its variation is within 0.1 mV. Thus, the proposed fault diagnosis method works fine.

Another variation source could be the location of the target via-switch in the CLB array because the interconnect resistance varies depending on the via-switch location. However, the interconnect resistance is about one order of magnitude lower than the via-switch resistance, and hence the impact of the via-switch location on the boundary reference voltage is relatively small. SPICE simulations have confirmed that the comparator successfully discriminates the on/off states of via-switches at different locations with more than 50 mV difference of the boundary reference voltage.

5.3 Testing Time

This subsection discusses the testing time of the proposed fault diagnosis method. As explained in Sect. 4.2, the proposed method tests a via-switch by turning on and off two atom switches that compose the via-switch, i.e., 4-time programming is required for each via-switch testing. According to Ref. [3], 2 ns is necessary to program one atom switch, and therefore the minimum programming time for testing one via-switch is estimated to be 8 ns. Also, we need to perform driver and comparator configurations for programming and reading, which correspond to turning on and off the NMOS pass transistors in Fig. 5. Let us suppose 1 ns is necessary for each configuration. In this case, the testing time of one via-switch is 21 ns, where 8 ns for programming, 4 ns for programming configurations and 9 ns for reading configurations. This estimation is based on the 14 steps described in Sect. 4.2. Here, comparation time of ASV-, CAS-, and TVR-read is ignored since it is smaller than the configuration time.

The testing time for each crossbar is 21 ns multiplied by the number of via-switches. For example, the testing time of a 100x100 crossbar is 210 μs. When all the via-switch crossbars share the programming drivers and one comparator as shown in Fig. 5, we need to test each crossbar sequentially. If the number of crossbars is large and the testing time is not acceptable, the via-switch FPGA can adopt parallel programming and testing scheme by increasing the number of drivers and comparators. Although the area overhead slightly increases due to the additional drivers and comparators, the parallel programming and testing scheme can reduce the testing time. We can choose the sequential scheme and the parallel scheme considering a tradeoff between testing time and testing circuit area.

6. Conclusion

This work has confirmed that a general comparator can discriminate on/off-states of via-switches in the crossbar-based FPGA and clarified fault modes of a via-switch by SPICE simulation. Then, this work has proposed a fault diagnosis method that exploits three read modes and identifies faulty via-switch components according to the comparator response difference between normal and faulty cases. The proposed method achieves 100% fault detection. As for the diagnosability, the successful ratios of the fault diagnosis are 100% and 79% in cases that the number of faulty components in a via-switch is up to one and up to two, respectively. The number of reprogramming in the proposed fault testing method is very small, i.e., each via-switch is reprogrammed only once.

Acknowledgments

This work was supported by JSPS KAKENHI Grant Number JP17J10008 and JST CREST Grant Number JPMJCR1432, Japan.

References

[1] I. Kuon and J. Rose, "Measuring the gap between FPGAs and ASICs," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol.26, no.2, pp.203–215, Feb. 2007.

[2] M. Lin, A.E. Gamal, Y.C. Lu, and S. Wong, "Performance benefits of monolithically stacked 3-D FPGA," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol.26, no.2, pp.216–229, Feb. 2007.

[3] H. Ochi, K. Yamaguchi, T. Fujimoto, J. Hotate, T. Kishimoto, T. Higashi, T. Imagawa, R. Doi, M. Tada, T. Sugibayashi, W. Takahashi, K. Wakabayashi, H. Onodera, Y. Mitsuyama, J. Yu, and

M. Hashimoto, "Via-switch FPGA: Highly dense mixed-grained reconfigurable architecture with overlay via-switch crossbars," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.26, no.12, pp.2723–2736, Dec. 2018.

[4] N. Banno, K. Okamoto, N. Iguchi, H. Ochi, H. Onodera, M. Hashimoto, T. Sugibayashi, T. Sakamoto, and M. Tada, "Low-power crossbar switch with two-varistors selected complementary atom switch (2V-1CAS; via-switch) for nonvolatile FPGA," IEEE Trans. Electron Devices, vol.66, no.8, pp.3331–3336, Aug. 2019.

[5] M. Hashimoto, X. Bai, N. Banno, M. Tada, T. Sakamoto, J. Yu, R. Doi, Y. Araki, H. Onodera, T. Imagawa, H. Ochi, K. Wakabayashi, Y. Mitsuyama, and T. Sugibayashi, "Via-switch FPGA: 65 nm CMOS implementation and architecture extension for AI applications," IEEE International Solid-State Circuits Conference (ISSCC), pp.502–503, Feb. 2020.

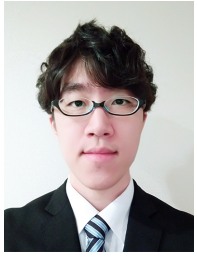
[6] R. Doi, X. Bai, T. Sakamoto, and M. Hashimoto, "Fault diagnosis of via-switch crossbar in non-volatile FPGA," Design, Automation, and Test in Europe Conference and Exhibition (DATE), 2020.

[7] N. Banno, M. Tada, K. Okamoto, N. Iguchi, T. Sakamoto, M. Miyamura, Y. Tsuji, H. Hada, H. Ochi, H. Onodera, M. Hashimoto, and T. Sugibayashi, "A novel two-varistors (a-Si/SiN/a-Si) selected complementary atom switch (2V-1CAS) for nonvolatile crossbar switch with multiple fan-outs," International Electron Devices Meeting (IEDM), pp.2.5.1–2.5.4, Dec. 2015.

[8] K. Okamoto, M. Tada, T. Sakamoto, M. Miyamura, N. Banno, N. Iguchi, and H. Hada, "Conducting mechanism of atom switch with polymer solid-electrolyte," International Electron Devices Meeting (IEDM), pp.12.2.1–12.2.4, Dec. 2011.

[9] M. Tada, T. Sakamoto, M. Miyamura, N. Banno, K. Okamoto, N. Iguchi, and H. Hada, "Improved off-state reliability of nonvolatile resistive switch with low programming voltage," IEEE Trans. Electron Devices, vol.59, no.9, pp.2357–2362, Sept. 2012.

[10] M. Miyamura, T. Sakamoto, M. Tada, N. Banno, K. Okamoto, N. Iguchi, and H. Hada, "Low-power programmable-logic cell arrays using nonvolatile complementary atom switch," International Symposium on Quality Electronic Design (ISQED), pp.330–334, March 2014.



Ryutaro Doi received B.E. and M.E. degrees in Information Systems Engineering from Osaka University, Japan, in 2015 and 2017, respectively. He is currently a doctoral student in the Department of Information Systems Engineering at Osaka University. His research interest includes reconfigurable architecture and its test. He is a Research Fellow of Japan Society for the Promotion of Science.

Xu Bai received the B.E. degree in Communication Engineering from Southwest Jiaotong University, Chengdu, China in 2008, M.S. and Ph.D. degrees in Information Sciences from Tohoku University, Sendai, Japan in 2011 and 2014, respectively. He is a senior researcher in System Platform Research Laboratories of NEC Corporation, Japan. His research interests include programmable logic device, nonvolatile memory, new concept VLSI including multiple-valued VLSI computing. He received the IEEE Sendai Student Award in 2010, the Excellent Student Poster Award at 22nd International Workshop on Post-Binary ULSI Systems in 2013 and SSDM Young Researcher Award in 2016. He is a member of IEEE.

Toshitsugu Sakamoto received the MSEE (1991) and Ph.D. (1996) degrees from Osaka University, Osaka, Japan. After joining NEC Corporation in 1991, he worked on nano-electronic devices such as hot electron transistors, single electron devices, and nano-electromechanical devices. His current focus is on solid-electrolyte devices used in switching elements of programmable logic. From 1999 to 2000 he was also a visiting researcher in California Institute of Technology, Pasadena, CA. He served as a program committee of IEEE Silicon Nanoelectronics Workshop in 2007&2009 and IEEE International Electron Devices Meeting in 2008&2009.

Masanori Hashimoto received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Now, he is a Professor in Department of Information Systems Engineering, Osaka University. His current research interests include design for manufacturability and reliability, timing and power integrity analysis, reconfigurable computing, soft error characterization and low-power circuit design. Dr. Hashimoto was on the technical program committees of international conferences including DAC, ICCAD, ITC, Symposium on VLSI Circuits, ASP-DAC and DATE. He serves/served as an associate editor for IEEE TVLSI, TCAS-I, and ACM TODAES.