A Frequency-Dependent Target Impedance Method Fulfilling Voltage Drop Constraints in Multiple Frequency Ranges

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***Abstract*— Target impedance plays a critical role in guiding a robust power delivery network (PDN) design. However, the traditional methodology has difficulty in associating time-domain information, such as current profile and voltage drop constraints, with frequency-domain PDN impedance. Existing works try to derive frequency-dependent target impedance, but the average voltage drop is not explicitly taken into account, and the dynamic voltage drop constraints are not considered separately in middle and high-frequency ranges. Such limitations can result in under- or over-designed PDN. This article proposes a frequency-dependent target impedance methodology, which determines the target impedance shape from the given constraints in multiple frequency ranges. The key idea is to exploit a concept of magnitude equivalent frequency to bridge the time-domain behavior and frequency-domain target impedance. Experiment results show that the proposed frequency-dependent target impedance tightly satisfies the given voltage drop constraints.**

***Index Terms*— Frequency dependent, magnitude equivalent frequency (MEF), target impedance, voltage drop constraints.**

I. Introduction

HIGH-QUALITY low-noise power delivery network (PDN) is highly demanded by modern VLSI design to ensure the performance, and the target impedance methodology is a common practice to guide PDN impedance design [1]. In tradition, target impedance Z_{target}, which serves as the maximum allowed self-impedance seen from chip load side, is defined as

$$Z_{\text{target}} = \frac{V_{\text{max\_drop}}}{I} \tag{1}$$

where $V_{\text{max\_drop}}$ is the maximum allowable voltage drop, and I is the current requirement. The resultant Z_{target} appears to be a flat line determined by the maximum current requirement, and hence, the PDN impedance is usually overconstrained. On the other hand, researchers try to derive frequency-dependent target impedance by associating time-domain information, such as current profile and dynamic voltage drop constraints, with frequency-domain impedance shape. However, existing efforts could result in over- or under-designed PDN because of the following problems.

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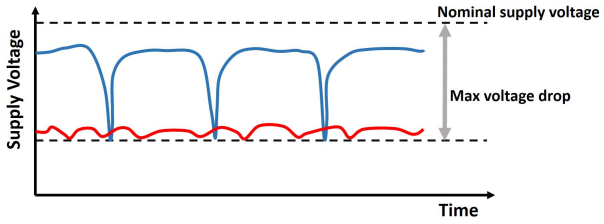

Fig. 1. Two voltage profiles with the same maximum voltage drop.

A. Main Problems and Related Work

The main problem for deriving the frequency-dependent target impedance is the design gap between the time-domain current/voltage information and the frequency-domain target impedance. Although the current spectrum tells us that dynamic power noise distributes within certain frequency ranges, how to determine the detailed frequency-dependent target impedance remains a difficult open problem. Researchers [2]–[7] try to approximate the time-domain current profile as a triangle or ramp so that the $L(di/dt)$ noise becomes a constant value and the PDN design flow is simplified. However, such approximation methods suffer from the fact that the real current waveform may not be easily simplified to the simple ramp or triangle shape. Oh and Shim [8] use the current spectrum for deriving frequency-dependent target impedance. However, the constraint of the worst voltage drop, which is defined in the time domain, is difficult to convert into the frequency domain. Without a clear interpretation between the time domain and frequency domain, PDN designers have to rely on empirical methods, such as iteration over the various resistor and capacitor configurations [9], [10].

On the other hand, the frequency-domain target impedance should consider the voltage drop constraints in multiple frequency ranges, but this requirement is not well handled in previous work. For example, in the dc frequency range, the average voltage drop should be considered since it can have a greater impact on the chip performance than the dynamic noise [11]–[13]. Let us take the voltage profiles in Fig. 1 to show the impact. Here, given a current load profile, suppose two PDNs that have different target impedance yet satisfy the same maximum voltage drop constraint. Two voltage profiles

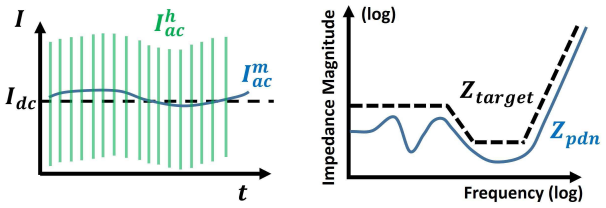

Fig. 2. Z_{target} for high-frequency noise dominated current.

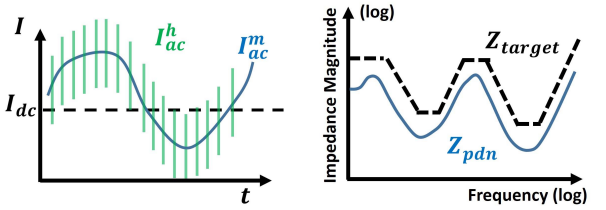

Fig. 3. Z_{target} for middle- and high-frequency noise dominated currents.

corresponding to the different PDNs are shown in red and blue. The red profile has lower average voltage and smaller ripple, which means the chip performance is lower, and the PDN of the red profile is overdesigned in the high-frequency range but underdesigned in the low-frequency range.

Besides, the target impedance should also consider voltage drop constraints in the middle-high-frequency range. While load current profiles are typically dominated by clock switching in the high-frequency range, current variation in the middle-frequency range can be triggered by workload transition or operation mode variation. For example, Mao *et al.* [14] reported that a stressful workload could cause a near 20-A load current ramp within 70 clock cycles for a GPU application, which suggests a significant middle-frequency component. Such middle-frequency current variation can impact chip timing performance [8]. Let us take two examples in Figs. 2 and 3 as illustration. Here, the two current profiles have the same magnitude and the same average value. Supposing the current profile in Fig. 2 is dominated by high-frequency clock switching current I^h_{ac} shown as the green lines and the PDN is designed to reduce the target impedance Z_{target} in the high-frequency range, the derived Z_{target} can be diagramed as the right part of Fig. 2. In Fig. 3 case, on the other hand, the VLSI operation mode or workload transition may introduce current fluctuation I^m_{ac} in the middle-frequency range. In such a case, additional efforts are needed to reduce the PDN impedance in the middle-frequency range, as shown in the right part of Fig. 3. The target impedance considering the multiple voltage drop constraints helps PDN designers to mitigate the under- or over-designed PDN.

B. Contribution and Organization

The main contribution of this article is to propose a frequency-dependent target impedance methodology that considers voltage drop constraints in multiple frequency ranges. For bridging the design gap between frequency- and time-domain information, a concept of magnitude equivalent frequency (MEF) is devised to simplify the frequency-dependent target impedance design. The transient

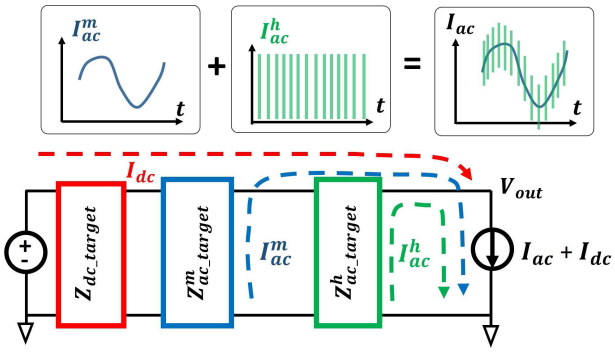

Fig. 4. Overall PDN structure for multistage target impedance.

simulation results show a close correlation between the time-domain voltage drop and the proposed frequency-domain target impedance.

The work in this article is an extension of our preliminary article [15]. In this article, we extend the preliminary work to support voltage drop constraints in multiple frequency ranges. The proposed target impedance is categorized into four basic shapes according to the time-domain information, and the proposed method derives one of them with concrete shape parameters. In addition, each shape of the target impedance is synthesized as a multistage equivalent circuit for validating the proposed method. Finally, we carry out additional experiments with multicore RISC-V [16] to verify the methodology.

The rest of this article is organized as follows. Section II presents the overall structure and the derivation flow of the frequency-dependent target impedance. Section III introduces the conception of MEF, which bridges the time-domain and frequency-domain information. Section IV presents a synthesis method of the target impedance and discusses the feasibility issue. Section V shows the experimental results, and Section VI draws the conclusion.

II. Overall Structure and Flow of Target Impedance Derivation

This section describes the overall structure and flow of target impedance derivation. The proposed methodology considers the voltage drop constraints from dc to high-frequency range. Here, it should be noted that many possible frequency-dependent target impedances exist since the degree of freedom is much larger than the number of the given constraints. Among them, it is necessary to provide simple frequency-dependent target impedance that has fewer parameters yet satisfies the constraints and has compatibility with the PDN design.

A. Overall Structure of Multistage Target Impedance

This section proposes a three-stage target impedance, which is shown in Fig. 4, to satisfy the voltage drop constraints in dc, middle-, and high-frequency ranges. Note that the target structure can be modified to support single-stage or more-stage structures with minor adaption work. In this article, the high-frequency range refers to MHz to GHz level, where the current spectrum is dominated by clock switching. The middle-frequency range refers to kHz to MHz, where the current fluctuation spectrum mainly originates from operation

mode or workload transitions. The actual frequency range is systematically determined in the proposed flow, which will be detailed in Sections II-B–II-D.

To derive the frequency-dependent target impedance, we first suppose that load current profile I consists of dc component $I_{\rm dc}$ and ac component $I_{\rm ac}$. Furthermore, the ac component consists of middle- and high-frequency components, which are $I_{\rm ac}^m$ and $I_{\rm ac}^h$, respectively. The relationship is diagramed in the upper part of Fig. 4 and can be expressed as

$$I = I_{\rm dc} + I_{\rm ac} = I_{\rm dc} + \left(I_{\rm ac}^m + I_{\rm ac}^h\right). \tag{2}$$

In a typical VLSI system, $I_{\rm ac}^h$ can be dominated by clock switching in each cycle, $I_{\rm ac}^m$ is dominated by operation mode or workload transition, and $I_{\rm dc}$ is the average current drawn by the chip load.

The three-stage target impedance structure is shown in the lower part of Fig. 4, where the high-frequency target impedance $Z_{\rm ac\_target}^h$ is derived for filtering $I_{\rm ac}^h$. The middle-frequency target impedance $Z_{\rm ac\_target}^m$ is derived for filtering $I_{\rm ac}^m$, and dc target impedance $Z_{\rm dc\_target}$ is derived such that $I_{\rm dc}$ can be supplied. Each target impedance stage is designed under the corresponding voltage drop constraint. Concatenating the target impedance of $Z_{\rm dc\_target}$, $Z_{\rm ac\_target}^h$, and $Z_{\rm ac\_target}^m$, designers can obtain the complete frequency-dependent target impedance $Z_{\rm target}$.

B. Overall Derivation Flow

Fig. 5 shows the overall flow deriving the proposed target impedance $Z_{\rm target}$. As the input to the flow, PDN designers shall provide one or multiple current profiles, denoted as $I_i(t)$ $(1 \le i \le N)$, where N is the number of the profiles. Then, designers shall determine, or be given, the maximum allowable voltage drops in each frequency range as the PDN design constraints. Here, we use $V_{\rm dc\_allow}$ to represent the maximum allowed average voltage drop, $V_{\rm ac\_allow}^h$ to represent the allowed ac voltage drop in the high-frequency range, and $V_{\rm ac\_allow}^m$ to represent the allowed ac voltage drop in the middle-frequency range.

With the given current profiles and voltage drop constraints, designers first derive and merge the target impedance in the dc frequency range for each current profile, which is Step 1 shown as the red block in Fig. 5. Then, the target impedance from the high-frequency to the low-frequency range is derived. In a three-stage target impedance scenario, $Z_{\rm ac\_target}^h$ and $Z_{\rm ac\_target}^m$ are derived and merged in sequence. These key steps are marked in red, green, and blue in Fig. 5. Next, in Step 7, we use the capacitance slope and inductance slope, which will be explained in Section II-C, to concatenate the target impedance components with each other. Finally, designers need to perform a feasibility check since the original voltage drop constraints might not be satisfied due to area, cost, or other design limitations. In such a case, designers need to refine their constraints and perform another iteration, which is Step 9 in the flow. If the result passes the feasibility check, designers can use $Z_{\rm target}$ for simulation purposes and guide actual PDN impedance design, which is Step 8 in the flow.

So far, we discussed the overall flow for the case where three voltage drop constraints specified in different frequency ranges were given. If additional voltage drop constraints are provided, the target impedance is derived from high frequency to low frequency in sequence, and accordingly, the process between Steps 4 and 6 needs to be performed with more steps. Note that the high-frequency impedance part is derived and synthesized before the lower frequency part because we use the high-frequency target impedance to bypass the high-frequency current component from the original current profile so that the target impedance in the lower frequency range can be derived without the interference from the higher frequency component. The run time of the derivation flow consists of two parts. The first part is the run time for parameter characterization that includes transient simulation (corresponding to Steps 2, 3, and 5–7). The second part is minor modification during target impedance synthesis (in Steps 4 and 8) so that the piecewise target impedance curve is closely tracked. These two run time parts will be presented in Section V.

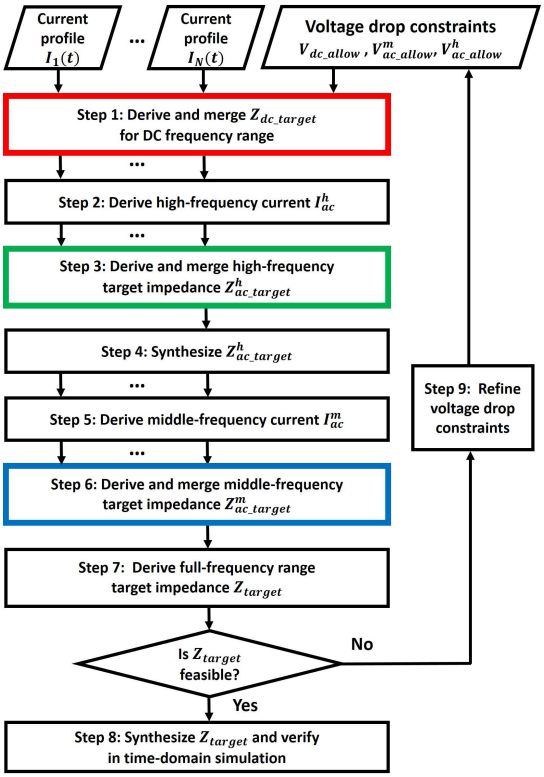

Fig. 5. Overall flow for deriving the three-stage target impedance.

On the other hand, when only one dynamic voltage drop constraint is provided, Steps 1, 3, and 7–9 of Fig. 5 are needed to derive the target impedance. The flow is diagramed in Fig. 6. Suppose PDN designers provided one or multiple current profiles $I_i(t)$, and the maximum allowable voltage drop constraints are given in dc and middle-high-frequency ranges. Here, we use $V_{\rm dc\_allow}$ to represent the maximum allowed average voltage drop, $V_{\rm ac\_allow}$ to represent the allowed ac voltage drop in the middle-high-frequency range. With the given current profiles and voltage drop constraints, designers first derive the target impedance in the dc frequency range, which is the red block in Fig. 6. Then, the target impedance in the middle-high frequency range is derived and merged, which is denoted as $Z_{\rm ac\_target}$ shown as the green box in Fig. 6.

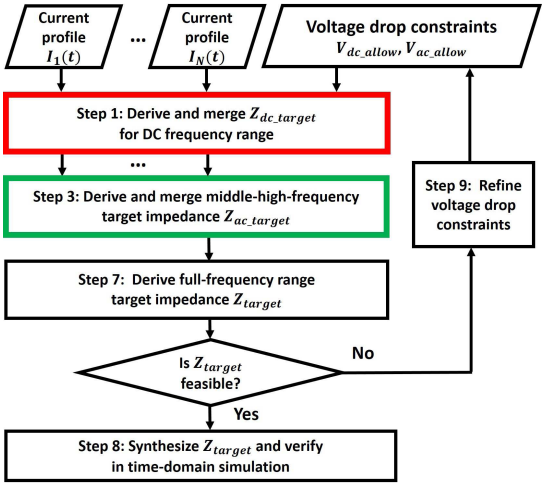

Fig. 6. Overall flow for deriving the target impedance with a single-dynamic voltage drop constraint.

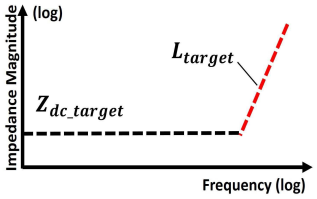

Fig. 7. Type I of Z_{target}.

Next, we derive overall target impedance Z_{target} by using the capacitance slope and inductance slope to concatenate the target impedance components with each other. Finally, designers need to perform a feasibility check before synthesizing the target impedance. If the feasibility check failed, the input voltage drop constraints need to be refined accordingly.

C. Basic Types of Target Impedance

The derived $Z_{\text{dc\_target}}$ can be either larger or smaller than $Z^{h}_{\text{ac\_target}}$ and $Z^{m}_{\text{ac\_target}}$. Therefore, four types of target impedance shape can be obtained, which are shown in Figs. 7–10. Each shape type may include multiple values of target impedance, which are shown as horizontal black dot lines. Then, capacitance and inductance slopes are used to concatenate the segments of the target impedance between frequency ranges. These slopes are marked in red dot lines and denoted as target inductance L_{target} and target capacitance C_{target}. The positions of these slopes are determined such that the design cost is minimized while the target impedance still satisfies the voltage drop constraints.

The type I of Z_{target} is shown in Fig. 7. In this case, the magnitude of $Z_{\text{dc\_target}}$ is less than or equal to that of the target impedance in other frequency ranges, which means that the average voltage drop is the severer constraint than the dynamic voltage drop. The main goal of type I is to optimize the dc current path to reduce $Z_{\text{dc\_target}}$.

The type II of Z_{target} is shown in Fig. 8. In this case, the magnitude of $Z_{\text{dc\_target}}$ is larger than one of the target impedance $Z_{\text{ac\_target}}$ in the middle- to high-frequency range, and mitigating the dynamic voltage drop in a certain frequency range is the main focus of PDN design.

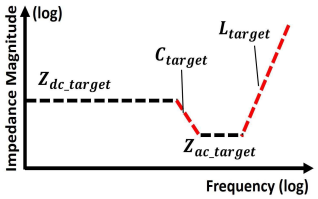

Fig. 8. Type II of Z_{target}.

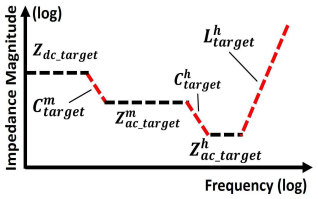

Fig. 9. Type III of Z_{target}.

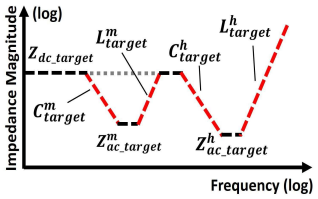

Fig. 10. Type IV of Z_{target}.

Fig. 9 shows type III of Z_{target}, and Fig. 10 shows type IV of Z_{target}. In these two cases, $Z_{\text{dc\_target}}$ is larger than the target impedance, marked as $Z^{h}_{\text{ac\_target}}$ and $Z^{m}_{\text{ac\_target}}$, in middle- to high-frequency range. In such types, mitigating dynamic voltage drops in two or more frequency ranges are the interest of PDN design. Furthermore, if the position of L_{target} in lower frequency overlaps with the C_{target} in the higher frequency range, we obtain type III. Otherwise, type IV is obtained.

In the following Section II-D, we first explain how to derive the target impedances for each frequency range, and then explain how to derive C_{target} and L_{target} to concatenate each impedance component using a concept of MEF in Section III.

D. Required Target Impedance in Each Frequency Range

To compose the frequency-dependent target impedance, the target impedance required in each frequency range should be determined. In a three-stage target impedance scenario, we need to derive $Z_{\text{dc\_target}}$, $Z^{h}_{\text{ac\_target}}$, and $Z^{m}_{\text{ac\_target}}$ in sequence, which has been discussed in Fig. 5.

First, to derive $Z_{\text{dc\_target}}$, let us suppose the average load current is I_{dc}, which can be calculated from the original current profile, and the maximum allowed average voltage drop is $V_{\text{dc\_allow}}$. The target impedance in the dc frequency range can be calculated as

$$Z_{\text{dc\_target}} = \frac{V_{\text{dc\_allow}}}{I_{\text{dc}}}. \tag{3}$$

Second, to derive high-frequency range target impedance $Z^{h}_{\text{ac\_target}}$, we define $I_{\text{pc}}(t)$, which is obtained by averaging

the load current profile $I(t)$ for each clock cycle and then holds a constant value within a clock cycle. Supposing the high-frequency current profile is dominated by clock switching current, the high-frequency current is expressed as

$$I^h_{\rm ac}(t) = I(t) - I_{\rm pc}(t). \tag{4}$$

Here, for given high-frequency dynamic current $I^h_{\rm ac}(t)$ and corresponding load voltage $V^h_{\rm ac}(t)$, we define the magnitude of $I^h_{\rm ac}(t)$ and $V^h_{\rm ac}(t)$ as follows:

$$\begin{aligned} {\rm Mag}\big(I^h_{\rm ac}(t)\big) &= I_{\rm max} - I_{\rm avg} \\ {\rm Mag}\big(V^h_{\rm ac}(t)\big) &= V_{\rm avg} - V_{\rm min} \end{aligned} \tag{5}$$

where $I_{\rm max}$ is the maximum value of $I^h_{\rm ac}(t)$, $I_{\rm avg}$ is the average value of $I^h_{\rm ac}(t)$, $V_{\rm avg}$ is the averaged $V^h_{\rm ac}(t)$, and $V_{\rm min}$ is the minimum load voltage. With this definition, the target impedance in the high-frequency range is

$$Z^h_{\rm ac\_target} = \frac{V^h_{\rm ac\_allow}}{{\rm Mag}\big(I^h_{\rm ac}(t)\big)} \tag{6}$$

where $V^h_{\rm ac\_allow}$ is the maximum allowed voltage drop of the high-frequency range, and the constraint of $V^h_{\rm ac\_allow}$ is satisfied if ${\rm Mag}(V^h_{\rm ac}(t)) \le V^h_{\rm ac\_allow}$.

The third step is to derive $Z^m_{\rm ac\_target}$. Supposing $V^m_{\rm ac\_allow}$ is the maximum allowed voltage drop of the middle-frequency range, the middle-frequency component is denoted as $I^m_{\rm ac}(t)$. Following the magnitude definition in (5), the target impedance in the middle-frequency range is expressed as.

$$Z^m_{\rm ac\_target} = \frac{V^m_{\rm ac\_allow}}{{\rm Mag}\big(I^m_{\rm ac}(t)\big)}. \tag{7}$$

Though theoretically, $I^m_{\rm ac}(t)$ can be calculated from (2), the actual circuit cannot completely filter out the high-frequency noise due to the existence of parasitic impedance. Therefore, in this article, we synthesize $Z^h_{\rm ac\_target}$ circuit, and the actual $I^m_{\rm ac}(t)$ is measured at the input port of synthesized $Z^h_{\rm ac\_target}$ circuit. Now, the required target impedance in each frequency range is derived through Steps 1–6.

III. Target Capacitance and Target Inductance

This section describes how to determine target capacitance and target inductance, which are necessary for Step 7 to concatenate $Z_{\rm dc\_target}$, $Z^m_{\rm ac\_target}$, and $Z^h_{\rm ac\_target}$ in the frequency domain. The capacitance slope and inductance slope connects the target impedance and determines the boundary of each frequency range. The following discussion in this section applies to all the red lines in Figs. 7–10.

First, when low-frequency target impedance $Z_{\rm low\_f\_target}$ is larger than high-frequency target impedance $Z_{\rm high\_f\_target}$, a capacitance slope is derived to concatenate the two frequency ranges, as is diagramed in Fig. 11. A larger capacitance can mitigate supply voltage noise better but result in a higher design cost. A smaller capacitance can save the design cost but may violate the voltage drop constraints. Therefore, designers need to derive the minimum required capacitance, or namely, the target capacitance $C_{\rm target}$, so that the target impedance can be satisfied between adjacent frequency ranges with the minimum capacitance value. In Fig. 11, the red dotted line exemplifies $C_{\rm target}$ slope, and $C_{\rm target}$ determines the corner frequency, denoted as $f_{\rm cap\_equ}$. We can also say $f_{\rm cap\_equ}$ determines $C_{\rm target}$ vice versa. Hereafter, we focus on $f_{\rm cap\_equ}$ to derive $C_{\rm target}$.

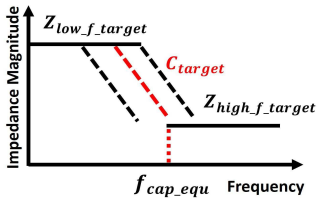

Fig. 11. Target capacitance.

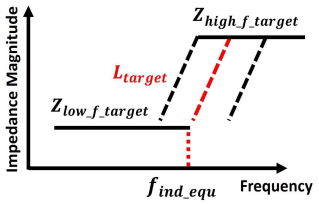

Fig. 12. Target inductance.

Similarly, as diagramed in Fig. 12, when low-frequency target impedance $Z_{\rm low\_f\_target}$ is smaller than high-frequency target impedance $Z_{\rm high\_f\_target}$, an inductance slope is derived to concatenate the two frequency ranges. The allowed inductance should be maximized to save the design cost. Such inductance is denoted as target inductance $L_{\rm target}$, which is exemplified as the red dotted line. To determine $L_{\rm target}$, we examine corner frequency $f_{\rm ind\_equ}$.

Sections III-A–III-C will derive $f_{\rm cap\_equ}$ and $f_{\rm ind\_equ}$ and then determine $C_{\rm target}$ and $L_{\rm target}$ accordingly by introducing a concept of MEF.

A. Magnitude Equivalent Frequency

The key idea of MEF is, instead of analyzing the detailed current waveform, to use a sine waveform current to reproduce the same magnitude of the voltage noise. The frequency of this sine waveform is defined as MEF. Once MEF is obtained for capacitance dominant impedance, such MEF can be regarded as the corner frequency $f_{\rm cap\_equ}$ to $C_{\rm target}$ in Fig. 11. Similarly, MEF for inductance dominant impedance is denoted as $f_{\rm ind\_equ}$, and it is used as the corner frequency to derive $L_{\rm target}$. The derivation of $C_{\rm target}$ and $L_{\rm target}$ will be discussed in Section III-A.1. The remaining of this section proves the existence of such MEFs and discusses the property of MEF.

1) MEF for Capacitance Dominant Impedance: For capacitance dominant impedance, supposing the magnitudes of original load current $I(t)$ and voltage $V(t)$ are bounded, which is always held in actual PDNs, it is necessarily to have a sine waveform current $I_s(t)$ that has the same magnitude, that is,

$${\rm Mag}(I_s(t)) = {\rm Mag}(I(t)). \tag{8}$$

Then, ${\rm Mag}(V_s(t))$ becomes a function of frequency for capacitance C dominant impedance

$${\rm Mag}(V_s(t)) = \frac{{\rm Mag}(I_s(t))}{2\pi C f_{\rm cap\_equ}}. \tag{9}$$

Therefore, there exists a frequency of sine waveform $f_{\text{cap\_equ}}$ that achieves

$$\text{Mag}(V_s(t)) = \text{Mag}(V(t)). \tag{10}$$

Hereafter, $f_{\text{cap\_equ}}$ is denoted as capacitance MEF of load current. The existence of this capacitance MEF can be summarized as follows.

Theorem 1: Let $I(t)$ be a load current profile and $V(t)$ be its corresponding PDN voltage profile. If $V(t)$ and $I(t)$ are bounded, $\text{Mag}(V(t))$ across the capacitance dominant impedance can be reproduced by current $I_s(t) = \text{Mag}(I(t)) \cdot \sin(2\pi f_{\text{cap\_equ}} \cdot t)$.
Such $I_s(t)$ is called magnitude equivalent current (MEC) of the capacitance dominant impedance. Furthermore, the MEF value is independent of capacitance value.

Theorem 2: Let $V(t)$ be the voltage profile for the original current profile, and $V_s(t)$ be the voltage profile for the MEC to the original current profile. Then, for all capacitance dominant impedances, $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$ hold.
With the definition of (5), the magnitudes of current and voltage satisfy the properties below, where N_A and N_B are arbitrary positive real numbers

$$\begin{aligned}\text{Mag}(N_A \cdot I(t)) &= N_A \cdot \text{Mag}(I(t)) \\ \text{Mag}(N_B \cdot V(t)) &= N_B \cdot \text{Mag}(V(t)).\end{aligned} \tag{11}$$

Supposing a sine MEC current $I_s(t)$ at MEF, then $\text{Mag}(I_s(t)) = \text{Mag}(I(t))$ and $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$ are satisfied for capacitance C dominant impedance. Then, for another capacitance C' dominant impedance

$$C' = N_C \cdot C \quad (N_C > 0) \tag{12}$$

the corresponding voltage magnitude for $I_s(t)$ is

$$\text{Mag}\big(V_s'(t)\big) = \frac{\text{Mag}(I_s(t))}{C' \cdot 2\pi f_{\text{cap\_equ}}} = \frac{\text{Mag}(V_s(t))}{N_C}. \tag{13}$$

In addition, $\text{Mag}(V(t))$ is inversely proportional to C, which can be explained using Fourier series of $V(t)$ and $V'(t)$, where $V'(t)$ is the voltage profile for C'. The coefficient for the same trigonometric function is N_C times different. Combining this relation with (11), $\text{Mag}(V'(t))$ becomes

$$\text{Mag}\big(V'(t)\big) = \text{Mag}\left(\frac{V(t)}{N_C}\right) = \frac{\text{Mag}(V(t))}{N_C} = \frac{\text{Mag}(V_s(t))}{N_C}. \tag{14}$$

Since the rightmost terms of (13) and (14) are identical, $\text{Mag}(V_s'(t)) = \text{Mag}(V'(t))$ still holds for different capacitances with the same MEC. Therefore, Theorem 2 is proven.

2) MEF for Inductance Dominant Impedance: For inductance dominant impedance, supposing the magnitudes of original load current $I(t)$ and voltage $V(t)$ are bounded, which is always held in actual PDNs, there must be a sine waveform current $I_s(t)$ that has the same magnitude, that is,

$$\text{Mag}(I_s(t)) = \text{Mag}(I(t)). \tag{15}$$

Then, $\text{Mag}(V_s(t))$ becomes a function of frequency for inductance L dominant impedance

$$\text{Mag}(V_s(t)) = 2\pi L f_{\text{ind\_equ}} \text{Mag}(I_s(t)). \tag{16}$$

Therefore, there exists a frequency of sine waveform $f_{\text{ind\_equ}}$ that achieves

$$\text{Mag}(V_s(t)) = \text{Mag}(V(t)). \tag{17}$$

Let us denote $f_{\text{ind\_equ}}$ as inductance MEF of load current. The existence of this inductance MEF can be summarized by the following.

Theorem 3: Let $I(t)$ be a load current profile, $V(t)$ be its corresponding PDN voltage profile. If $I(t)$ and $V(t)$ are bounded, $\text{Mag}(V(t))$ across the inductance dominant impedance can be reproduced by current $I_s(t) = \text{Mag}(I(t)) \cdot \sin(2\pi f_{\text{ind\_equ}} \cdot t)$.
Such $I_s(t)$ is called MEC of inductance dominant impedance. Furthermore, the MEF value is independent of inductance value.

Theorem 4: Let $V(t)$ be the voltage profile for the original current profile, and $V_s(t)$ be the voltage profile for the MEC to the original current profile. Then, for all inductance dominant impedances, $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$ hold.
With the definition of (5), the magnitudes of current and voltage satisfy the following properties, where N_A and N_B are arbitrary positive real numbers:

$$\begin{aligned}\text{Mag}(N_A \cdot I(t)) &= N_A \cdot \text{Mag}(I(t)) \\ \text{Mag}(N_B \cdot V(t)) &= N_B \cdot \text{Mag}(V(t)).\end{aligned} \tag{18}$$

Supposing a sine MEC current $I_s(t)$ at MEF, then $\text{Mag}(I_s(t)) = \text{Mag}(I(t))$ and $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$ are satisfied for inductance L dominant impedance. Then, for another inductance L' dominant impedance

$$L' = N_L \cdot L \quad (N_L > 0) \tag{19}$$

the corresponding voltage magnitude for $I_s(t)$ is

$$\text{Mag}\big(V_s'(t)\big) = L' \cdot 2\pi f_{\text{ind\_equ}} \text{Mag}(I_s(t)) = N_L \cdot \text{Mag}(V_s(t)). \tag{20}$$

In addition, $\text{Mag}(V(t))$ is proportional to L, which can be explained using Fourier series of $V(t)$ and $V'(t)$, where $V'(t)$ is the voltage profile for L' dominate impedance. The coefficient for the same trigonometric function is N_L times different. Combining this relation with (18), $\text{Mag}(V'(t))$ becomes

$$\begin{aligned}\text{Mag}\big(V'(t)\big) &= \text{Mag}(N_L V(t)) = N_L \text{Mag} \cdot (V(t)) \\ &= N_L \cdot \text{Mag}(V_s(t)).\end{aligned} \tag{21}$$

Since the rightmost terms of (20) and (21) are identical, $\text{Mag}(V_s'(t)) = \text{Mag}(V'(t))$ still holds for different inductances with the same MEC. Therefore, Theorem 4 is proven.

So far, the existence of MEFs for capacitance and inductance dominant impedances have been proved, and MEFs are independent of capacitance and inductance values.

3) Bridging Time Domain and Frequency Domain With MEF: MEF can bridge the time-domain current waveform shape with a frequency-domain impedance shape. Here, we use a square waveform to illustrate the current shape correlation with capacitance MEF. The squared waveform shape is shown in Fig. 13, where the pulsewidth is represented as T_{pw}, the pulse height of the current profile is denoted

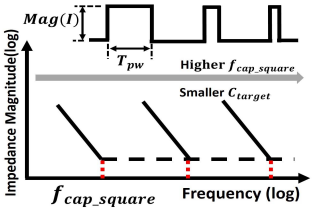

Fig. 13. Square waveform with capacitance MEF.

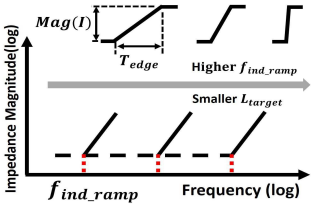

Fig. 14. Ramp waveform with inductance MEF.

as $\mathrm{Mag}(I)$. The magnitude of the dynamic voltage drop of capacitance C_{test} dominated impedance can be simplified as

$$\mathrm{Mag}(V) = \frac{\int \mathrm{Mag}(I)dt}{C_{\mathrm{test}}} = \frac{\mathrm{Mag}(I) \cdot T_{\mathrm{pw}}}{C_{\mathrm{test}}} \tag{22}$$

and MEF $f_{\mathrm{cap\_square}}$ can be simplified as

$$f_{\mathrm{cap\_square}} = \frac{\mathrm{Mag}(I)}{2\pi C_{\mathrm{test}} \mathrm{Mag}(V)} = \frac{1}{2\pi T_{\mathrm{pw}}}. \tag{23}$$

The relationship in (23) suggests that a narrower current pulsewidth results in larger capacitance MEF. To meet the dynamic voltage drop constraints, a smaller target capacitance is satisfactory, which means the capacitance slope shifts to the right side in the frequency domain, which is illustrated in the lower part of Fig. 13.

Similarly, we use a ramp waveform to illustrate the effectiveness of inductance MEF. The ramp waveform shape is shown in the upper part of Fig. 14, where the rising time is represented as T_{edge}, and the ramp height of the current profile is denoted as $\mathrm{Mag}(I)$. The magnitude of the dynamic voltage drop of inductance L_{test} dominated impedance can be simplified as

$$\mathrm{Mag}(V) = L\frac{d(\mathrm{Mag}(I))}{dt} = \frac{L_{\mathrm{test}}\mathrm{Mag}(I)}{T_{\mathrm{edge}}} \tag{24}$$

and MEF $f_{\mathrm{ind\_ramp}}$ can be derived as

$$f_{\mathrm{ind\_ramp}} = \frac{\mathrm{Mag}(V)}{2\pi L_{\mathrm{test}}\mathrm{Mag}(I)} = \frac{1}{2\pi T_{\mathrm{edge}}}. \tag{25}$$

The relationship in (25) indicates that the shorter rising time results in larger inductance MEF. To meet the dynamic voltage drop constraints, a smaller target inductance is demanded, which means the inductance slope shifts to the right side in the frequency domain, as shown in Fig. 14. These two illustrations exemplify the usefulness of MEF. Using the MEF and target impedance for each frequency range, we can bridge the time-domain current/voltage information with the frequency-domain target impedance shape.

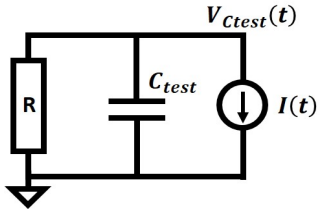

Fig. 15. RC characterization circuit.

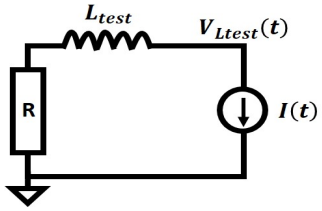

Fig. 16. RL characterization circuit.

B. Deriving Target Inductance and Target Capacitance

This section explains how to derive MEF and obtain target inductance and target capacitance.

MEF can be derived for any capacitance and inductance, as suggested in Theorem 2 and Theorem 4. Figs. 15 and 16 show circuits for characterizing capacitance MEF $f_{\mathrm{cap\_equ}}$ and inductance MEF $f_{\mathrm{ind\_equ}}$, respectively, where the values of R, C_{test}, and L_{test} can be arbitrarily set by designers. Given the load current profile $I(t)$, the voltage drop over pure resistance R is calculated as $V_{\mathrm{ref}}(t) = R \cdot I(t)$. The output voltage $V_{C_{\mathrm{test}}}(t)$, $V_{L_{\mathrm{test}}}(t)$, and their magnitudes $\mathrm{Mag}(V_{C_{\mathrm{test}}}(t))$ and $\mathrm{Mag}(V_{L_{\mathrm{test}}}(t))$ are obtained by simulation. Note that although the values of C_{test} and L_{test} do not impact MEF thanks to Theorems 2 and 4, designers still need to select sufficiently large capacitance and inductance to ensure that the circuit impedance is dominated by the capacitance or inductance. Here, the dominance means $\mathrm{Mag}(V_{C_{\mathrm{test}}}(t))$ is sufficiently smaller than $\mathrm{Mag}(V_{\mathrm{ref}}(t))$, and $\mathrm{Mag}(V_{L_{\mathrm{test}}}(t))$ is sufficiently larger than $\mathrm{Mag}(V_{\mathrm{ref}}(t))$.

When the impedance of RC characterization circuit is capacitance C_{test} dominant, $f_{\mathrm{cap\_equ}}$ is derived as

$$f_{\mathrm{cap\_equ}} = \frac{\mathrm{Mag}(I(t))}{\mathrm{Mag}\left(V_{C_{\mathrm{test}}}(t)\right)}\frac{1}{2\pi C_{\mathrm{test}}}. \tag{26}$$

Similarly, when the RL characterization circuit is dominated by inductance L_{test}, $f_{\mathrm{ind\_equ}}$ is derived as

$$f_{\mathrm{ind\_equ}} = \frac{\mathrm{Mag}\left(V_{L_{\mathrm{test}}}(t)\right)}{\mathrm{Mag}(I(t))}\frac{1}{2\pi L_{\mathrm{test}}}. \tag{27}$$

Then, the corresponding target capacitance and target inductance are

$$C_{\mathrm{target}} = \frac{1}{2\pi f_{\mathrm{cap\_equ}} Z_{\mathrm{ac\_target}}} \tag{28}$$

$$L_{\mathrm{target}} = \frac{Z_{\mathrm{ac\_target}}}{2\pi f_{\mathrm{ind\_equ}}}. \tag{29}$$

Algorithm 1 summarizes the derivation of target inductance L_{target} and target capacitance C_{target}, where the parameter α is set as 0.1 to ensure the dominance of inductance and capacitance in our experiment. Now, all the parameters to

Algorithm 1 Deriving Target Inductance and Target Capacitance

Input: $I(t)$

Main Routine:

Calculate $\text{Mag}(V_{\text{ref}}(t)) = \text{Mag}(R \cdot I(t))$.
Measure $\text{Mag}(V_{C_{\text{test}}}(t))$ of RC characterization circuit.
Measure $\text{Mag}(V_{L_{\text{test}}}(t))$ of RL characterization circuit.
if $\text{Mag}(V_{C_{\text{test}}}(t)) < \alpha \cdot \text{Mag}(V_{\text{ref}}(t))$ **then**
  Derive capacitance MEF $f_{\text{cap\_equ}}$ by (26)
  Derive target capacitance C_{target} by (28)
else
  Abort with a message "Select larger C_{test}".
end if
if $\text{Mag}(V_{L_{\text{test}}}(t)) > (1/\alpha) \cdot \text{Mag}(V_{\text{ref}}(t))$ **then**
  Derive inductance MEF $f_{\text{ind\_equ}}$ by (27)
  Derive target inductance L_{target} by (29)
else
  Abort with a message "Select larger L_{test}".
end if

define the proposed frequency-dependent target impedance have been derived, which are C_{target} in (28), L_{target} in (29), $Z_{\text{ac\_target}}$ in (6) and (7), and $Z_{\text{dc\_target}}$ in (3).

C. Merging Target Impedance

This section explains how to merge target impedance curves that are derived from multiple input current profiles. Multiple target impedance curves can be merged using an envelope method or a boundary method. Here, we use Fig. 17 to show these two merge methods. Suppose in a certain frequency range, two target impedance $Z_{\text{target\_}i}$ and $Z_{\text{target\_}j}$ are derived from current profiles $I_i(t)$ and $I_j(t)$, respectively. The envelope method is to concatenate all the envelope segments from the target impedance curves, which is shown as the red line in Fig. 17. However, the envelope method may cause extra complexity during the target impedance synthesis. On the other hand, the boundary method does not increase the number of segments, which is shown as the black line in Fig. 17, and it can be expressed as

$$\begin{aligned} Z_{\text{dc\_target}} &= \min_{1\le i\le N} Z_{\text{dc\_target\_}i} \\ Z_{\text{ac\_target}} &= \min_{1\le i\le N} Z_{\text{ac\_target\_}i} \\ C_{\text{target}} &= \max_{1\le i\le N} C_{\text{target\_}i} \\ L_{\text{target}} &= \min_{1\le i\le N} L_{\text{target\_}i} \end{aligned} \tag{30}$$

where $Z_{\text{dc\_target\_}i}$, $Z_{\text{ac\_target\_}i}$, $C_{\text{target\_}i}$, and $L_{\text{target\_}i}$ are target impedance parameters derived from current profile $I_i(t)$. $Z_{\text{dc\_target}}$, $Z_{\text{ac\_target}}$, C_{target}, and L_{target} are target impedance parameters merged from N current profiles. The boundary method can simplify the target impedance synthesis at the cost of tighter target impedance compared with the envelope method. In Section IV, we use the boundary method to simplify the synthesis process of target impedance since the transient simulation result in Section V shows a close correlation between the design expectation and the minimum load voltage level.

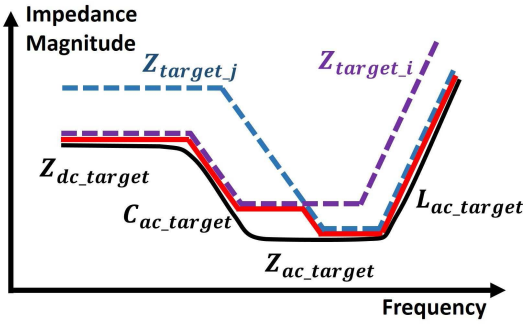

Fig. 17. Merging two target impedance curves from different current profile inputs. Red curve is derived by envelope method, and black curve is derived by boundary method.

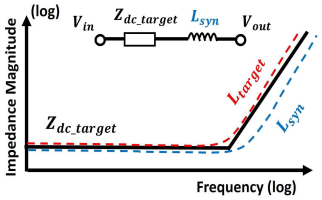

Fig. 18. Type I target impedance synthesis.

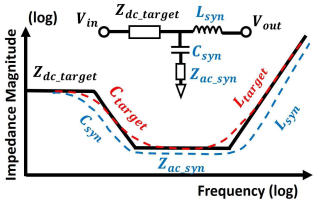

Fig. 19. Type II target impedance synthesis.

IV. Target Impedance Synthesis and Refinement of Voltage Drop Constraints

This section explains the synthesis method of the proposed target impedance, which are used in Steps 4 and 8. In addition, we discuss the refinement of voltage drop constraints in Step 9 according to the feasibility checking.

A. Synthesizing Frequency-Dependent Target Impedance

To validate the target impedance in the time domain, a simulatable PDN that traces the frequency-dependent target impedance is necessary. On the other hand, the derived target impedance is a piecewise curve in the frequency domain, and consequently, the exact PDN realization is difficult. In this article, we use lumped RLC components to track the piecewise target impedance. The type I target impedance is synthesized in Fig. 18. Similarly, type II, type III, and type IV target impedances are synthesized as the circuits shown in Figs. 19–21, respectively.

When the values of L_{target} and C_{target} are directly used in the circuits, the voltage drop constraints can be violated because the impedance of the circuits is larger at the corner frequencies than the piecewise target impedance, which is shown as the red dashed line in Figs. 18 and 19. To avoid this violation, we use larger capacitance C_{syn}, smaller inductance L_{syn}, or smaller

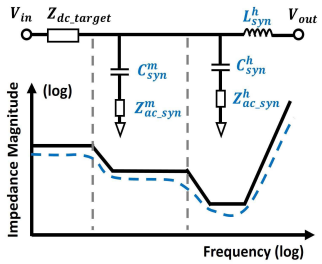

Fig. 20. Type III target impedance synthesis.

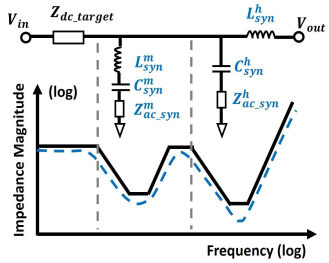

Fig. 21. Type IV target impedance synthesis.

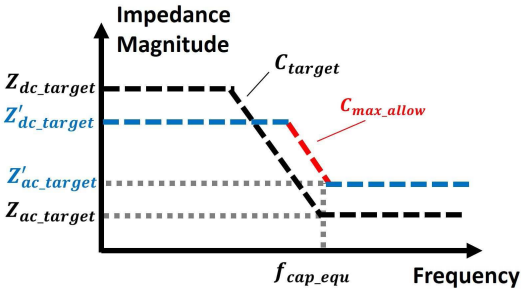

Fig. 22. Example of the refinement of voltage drop constraints for feasible target impedance.

resistance $Z_{\text{ac\_syn}}$ to ensure the actual impedance is close to $Z_{\text{ac\_target}}$ at the corner frequencies, which is plotted as the blue dashed line. It should be noted that this circuit synthesis is just one method, and various approaches could be adopted in the actual PDN design.

B. Refining Voltage Drop Constraints

Finally, we pay attention to the case that the circuit cannot be synthesized within the given design resource. A typical situation is that the decoupling capacitance budget $C_{\text{max\_allow}}$ is smaller than the required target capacitance C_{target}, which is shown as the red dotted line in Fig. 22.

In such a situation, even though PDN designers use the maximum allowed decoupling capacitance, the dynamic voltage drop cannot meet the design constraints. Therefore, the original voltage drop constraints need to be refined, for example, by applying smaller $V_{\text{dc\_allow}}$ and larger $V_{\text{ac\_allow}}$, which results in lower $Z'_{\text{dc\_target}}$ and higher $Z'_{\text{ac\_target}}$ shown as the blue dot lines in Fig. 22. On the other hand, if the dynamic voltage drop constraint is very strict, then the impedance of dc path requires aggressive refinement, which means $Z'_{\text{dc\_target}}$ is reduced to as low as $Z_{\text{ac\_target}}$ so that the impedance magnitude at MEF can be satisfied, and type I target impedance shape is obtained.

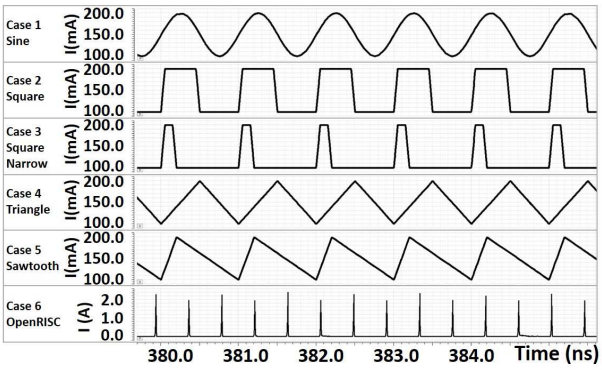

Fig. 23. Load current profiles at 1 GHz for experiments. From top to bottom: Sine, Square, Square narrow, Triangle, Sawtooth, and OpenRISC.

It should be noted that the voltage drop constraints depend on the actual performance requirement, and the refinement approach varies case by case. Several iterations may be needed before finding a proper set of voltage drop constraints.

V. Experimental Results

This section experimentally verifies whether the proposed target impedance can satisfy the voltage drop constraints under various current profiles and scenarios of voltage drop constraints. The first experiment is performed on current profiles having no middle-frequency variation, which means the dynamic current spectrum is distributed in a single-frequency range. In such a scenario, single-stage target impedance is derived for verification. The second experiment is performed for current profiles with fluctuations in both middle and high-frequency ranges. In such a scenario, multiple voltage drop constraints are given, and three-stage target impedance is synthesized for verification. The third experiment is performed with multiple input current profiles and multiple voltage drop constrains. In such a scenario, target impedance is derived in each frequency range and then merged, so that the voltage drop constraints are satisfied for all the input profiles.

A. Experiment for Dynamic Current in a Single-Frequency Range

To evaluate the applicability of the proposed methodology to a single-dynamic voltage drop constraint, this experiment prepared six current load profiles in Fig. 23. Cases 1–5 are artificial load waveforms. Cases 1–5 suppose 1-GHz operation, and their fluctuations range 100–200 mA. Case 6 is obtained from 32-b OpenRISC [17] core logic operation, where a CRC checksum program is given to OpenRISC as workload.

Case 1 of the sine waveform aims to confirm that the inductance MEF and capacitance MEF are 1.0 GHz as expected. In cases 2 and 3, square waveforms with different widths of 400 and 100 ps are used to mimic sudden and short-duration module activations. In cases 4 and 5, triangle waveforms with different rising times of 500 and 200 ps aim to mimic typical digital circuit load. In the experiments, the constraints of maximum allowable voltage drop is set as $V_{\text{avg\_allow}} = 70$ mV and $V_{\text{dyn\_allow}} = 10$ mV. Given the nominal voltage as 800 mV, the minimum allowable voltage is 720 mV.

Table I lists the derived values of $Z_{\text{dc\_target}}$, $Z_{\text{ac\_target}}$, C_{target}, and L_{target}, where these four parameters define the

TABLE I
DERIVED TARGET IMPEDANCE PARAMETERS, AND AVERAGE AND MINIMAL VOLTAGES

	Z_{dc_target} (mΩ)	Z_{ac_target} (mΩ)	C_{target} (nF)	L_{target} (pH)	V_{avg} (mV)	V_{min} (mV)
Case 1	466.6	200.0	0.8	31.8	730.0	722.5
Case 2	482.7	181.8	1.2	5.0	730.0	722.2
Case 3	608.7	117.6	0.7	5.0	729.9	720.9
Case 4	466.6	200.0	0.6	24.7	730.0	722.5
Case 5	466.6	200.0	0.5	19.8	730.0	722.5
Avg. Err	-	-	-	-	0.0003%	0.3%
Case 6	251.9	12.5	0.35	0.01	790.2	760.6
Avg. Err	-	-	-	-	0.02%	0.07%

TABLE II
EXPERIMENTAL SETUP OF ARTIFICIAL CURRENT PROFILE AND VOLTAGE DROP CONSTRAINTS

	Magnitude (mA)	Frequency (Hz)	Allowed V_{drop} (mV)
I^h_{ac}	50.0	1.0 G	1.0
I^m_{ac}	50.0	1.0 M	10.0
I_{dc}	200.0	-	80.0

proposed frequency-dependent target impedance. In the last two columns, the average and minimum load voltages V_{avg} and V_{min} are obtained from the simulation with the type II synthesized RLC circuit shown in Fig. 19. The average errors of V_{avg} and V_{min} are 0.0003% and 0.3%, which indicates the PDNs that satisfy the frequency-dependent target impedance meet the given constraints of the average and maximum voltage drops.

For case 6 of OpenRISC, the load circuit is designed with NanGate 15-nm open cell library at 1.2 GHz. The nominal voltage is 800 mV, and the constraints of $V_{\text{avg\_allow}} = 10$ mV and $V_{\text{dyn\_allow}} = 30$ mV are given. Then, the minimum allowable voltage is 760 mV. Type II target impedance is derived based on $Z_{\text{dc\_target}}$, $Z_{\text{ac\_target}}$, C_{target}, and L_{target}, which are listed in Table I. This target impedance circuit is synthesized as a type II circuit in Fig. 19 and simulated with the current source of the load current. The measured V_{min} and V_{avg} are 760.6 and 790.2 mV, respectively. These results indicate that the proposed frequency-dependent target impedance works well for the actual processor workload, including various frequency components.

B. Experiment for Multiple Dynamic Voltage Drop Constraints

This section performs two subexperiments; the first experiment validates the target impedance methodology with an artificial current profile consisting of two frequency components. The second experiment uses a four-core RISC-V current profile for validation.

First, we use an artificial current profile that includes two sine waveforms, denoted as I^h_{ac} and I^m_{ac}. The average current is denoted as I_{dc}. The voltage drop constraints are determined for dc, middle-frequency, and high-frequency ranges, and these setups are summarized in Table II.

Then, the overall current profile is the summation of I^h_{ac}, I^m_{ac}, and I_{dc}. The proposed multistage target impedance

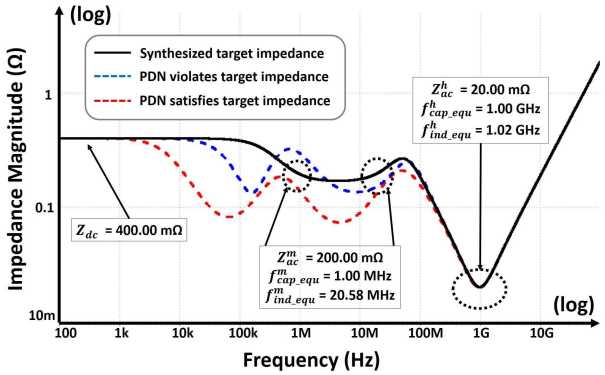

Fig. 24. Synthesized target impedance and PDN impedance.

methodology returns $Z_{\text{dc}} = 400.00$ mΩ, $Z^m_{\text{ac}} = 200.00$ mΩ, and $Z^h_{\text{ac}} = 20.00$ mΩ. The MEFs of the high-frequency range are extracted as $f^h_{\text{cap\_equ}} = 1.00$ GHz and $f^h_{\text{ind\_equ}} = 1.02$ GHz, and the MEFs of the middle-frequency range are extracted as $f^m_{\text{cap\_equ}} = 1.00$ MHz and $f^m_{\text{ind\_equ}} = 20.58$ MHz. Since the middle-frequency range does not overlap with the high-frequency range, we use type IV synthesized circuit of Fig. 21 to track the Z_{dc}, Z^m_{ac}, and Z^h_{ac} in each frequency range. The resultant circuit impedance is shown by the black line in Fig. 24. The tracked frequency-impedance points are also marked in Fig. 24. As for the run time of Z_{target} construction, the parameter characterization process takes 92.58 s. The minor modification during Z_{target} synthesis takes less than three minutes. As the comparison, we also synthesized another PDN impedance which satisfies the target impedance, which is shown as the red dotted line, and a PDN impedance which intentionally violates target impedance in the middle-frequency range shown as the blue dotted line in Fig. 24.

In the transient simulation result for validation, the average voltage drop of the synthesized target impedance circuit is 79.99 mV, and the total dynamic voltage drop is 10.93 mV. Compared with the design constraints of 80.0 and 11.0 mV, the errors are 0.01% and 0.60%. As for the PDN satisfying the target impedance, the dynamic voltage drop is 8.14 mV, which means the dynamic voltage drop constraint is also satisfied in the time domain. For the PDN violating the target impedance, the total dynamic voltage drop is 15.98 mV, which means the dynamic voltage drop constraint is violated in the time domain as is expected.

Second, we use a current profile obtained from a four-core RISC-V processor. The processor is designed with NanGate 45-nm Open Cell Library at 500 MHz. The nominal voltage is 1.1 V, and the workload is multithread floating-point array multiplication, which is derived from RISC-V testing case [18]. In the nonaveraged raw current profile, the current pulse peak is dominated by the simultaneous switching of the cells in the clock paths, and it is 6.47 A. In Fig. 25, the raw current profile is averaged every 50 clock cycles to make the load current variation in the middle-frequency range visible.

The RISC-V finished its initialization at around 150 μs, followed by four plateaus in which the FPUs in the RISC-V are operational. A significant voltage drop event is expected

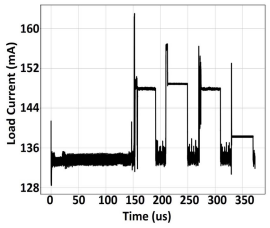

Fig. 25. Four-core RISC-V current profile averaged every 50 clock cycles.

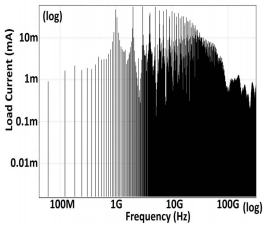

Fig. 26. Current spectrum of single RISC-V core.

near 150-μs simulation time. The load current spectrum of each RISC-V core is shown in Fig. 26, where we can see the current components distribute from below 100 MHz to over 100 GHz and the current includes both the middle- and high-frequency components. Next, we set the voltage drop constraints as $V_{\text{dc\_allow}} = 80.0$ mV, $V^h_{\text{ac\_allow}} = 10.0$ mV, and $V^m_{\text{ac\_allow}} = 10.0$ mV, respectively. The proposed multistage target impedance methodology outputs $Z_{\text{dc}} = 559.44$ mΩ, $Z^m_{\text{ac}} = 267.66$ mΩ, and $Z^h_{\text{ac}} = 1.58$ mΩ. The MEFs of the high-frequency range are extracted as $f^h_{\text{cap\_equ}} = 9.60$ GHz and $f^h_{\text{ind\_equ}} = 28.58$ GHz.

Next, we obtained the current profile of the middle-frequency range from the input port of the synthesized high-frequency target impedance. The zoomed-in view of the middle-frequency current profile, which includes the dc current, is shown in Fig. 27, where we can find the high-frequency peak current is suppressed to 178.81 mA. In addition, we can see a 20-ns transient process as the middle-frequency variation. Then, we use this profile to derive middle-frequency target impedance. The MEFs of the middle-frequency range are extracted as $f^m_{\text{cap\_equ}} = 0.86$ MHz and $f^m_{\text{ind\_equ}} = 9.78$ GHz. The middle-frequency range and the high-frequency range overlap, and then we use type III circuit of Fig. 20 for the circuit synthesis to track the Z_{dc}, Z^m_{ac}, and Z^h_{ac} in individual frequency ranges. The black line in Fig. 28 plots the resultant impedance. Besides, the middle-frequency target impedance is marked as the blue dotted line in Fig. 28 to reveal the components of $f^m_{\text{ind\_equ}}$ and Z^m_{ac}. As for the run time of Z_{target} construction, the parameter characterization process takes 290.02 s. The minor modification during Z_{target} synthesis take less than five minutes.

With the synthesized target impedance circuit, we run the transient simulation using the RISC-V current profile. The minimum load voltage is 1000.90 mV, and the average voltage is 1021.60 mV. The minimum voltage is merely 0.90 mV higher than the expected one of 1000.00 mV, and the average voltage is 1.60 mV higher than the expected one of 1020.00 mV. Fig. 29 shows a zoomed-in view of the

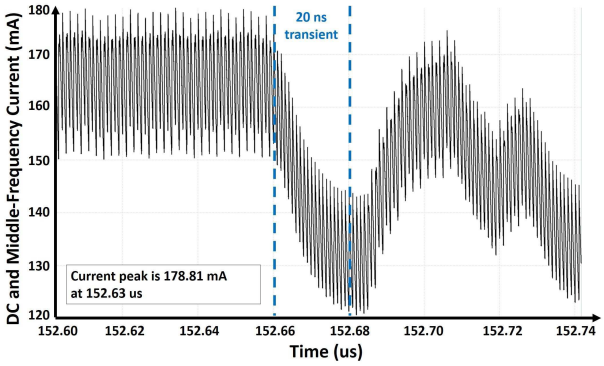

Fig. 27. RISC-V magnified current profile including middle-frequency component.

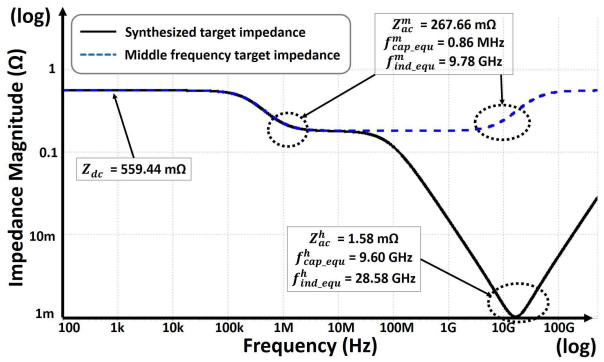

Fig. 28. Multistage target impedance for RISC-V current profile.

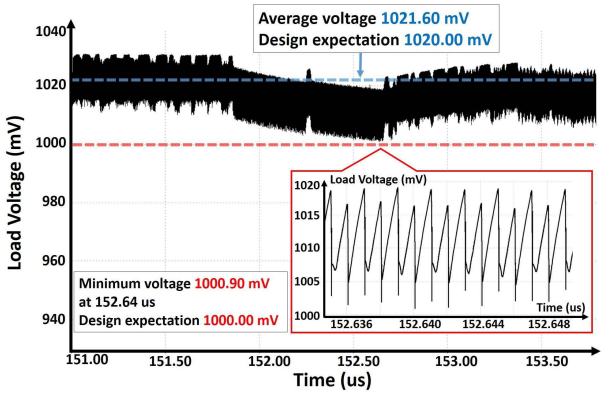

Fig. 29. Worst voltage drop using synthesized target impedance.

transient load voltage at the worst voltage drop. These results verify the proposed method.

C. Experiment for Multiple Current Profiles and Multiple Dynamic Voltage Drop Constraints

In this section, three current profiles are given to derive target impedance for four-core RISC-V load. The setup of RISC-V load is the same as the previous one. The first input current profile, denoted as $I_1(t)$, reuses the experiment setup in Section V-B, which is multithread floating-point array multiplication C program. The other two profiles are derived from MiBench benchmarks [19] to represent real-world workloads

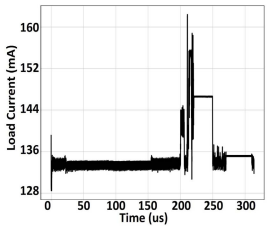

Fig. 30. Four-core RISC-V CRC benchmark current profile, averaged every 50 clock cycles.

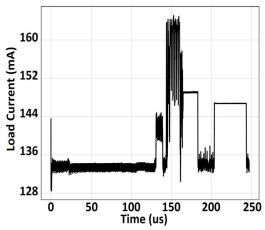

Fig. 31. Four-core RISC-V string-search benchmark current profile averaged every 50 clock cycles.

TABLE III
TARGET IMPEDANCE FROM MULTIPLE CURRENT PROFILES

Profile	Z_{dc_target} (mΩ)	$Z^m_{ac\_allow}$ (mΩ)	$Z^h_{ac\_allow}$ (mΩ)	Char. Time (s)	Min. Volt (mV)
$I_1(t)$	559.44	273.98	1.58	290.02	1011.50
$I_2(t)$	541.67	237.44	1.53	241.52	1010.31
$I_3(t)$	501.81	436.04	1.56	299.96	1007.90
Merged	501.81	237.44	1.53	–	–

(i.e., CRC and string search bare-metal C programs). These current profiles are denoted as $I_2(t)$ and $I_3(t)$, and the averaged current profiles are shown in Figs. 30 and 31, respectively. Next, we set the voltage drop constraints as $V_{\text{dc\_allow}} = 80.0$ mV, $V^h_{\text{ac\_allow}} = 10.0$ mV, and $V^m_{\text{ac\_allow}} = 10.0$ mV. The derived target impedance at different frequency ranges are listed the Table III. By merging the target impedance parameters in each frequency range using the boundary method, the high-frequency MEFs become $f^h_{\text{cap\_equ}} = 9.31$ GHz and $f^h_{\text{ind\_equ}} = 30.12$ GHz. The middle-frequency MEFs are $f^m_{\text{cap\_equ}} = 0.79$ MHz and $f^m_{\text{ind\_equ}} = 9.89$ GHz. These parameters result in type III target impedance of Fig. 20. The parameter characterization process takes less than 300 s for each profile. The modification during circuit synthesis takes less than seven minutes.

With the synthesized target impedance, we run the transient simulation to verify the quality of the proposed method. The minimum voltage level of each current profile is show in the last column of Table III, and the average error to the design expectation is 0.99%. The lowest voltage level among the three profiles is 1007.90 mV, which is 7.90 mV higher than the design expectation. Figs. 32 and 33 show the zoomed-in views of the transient load voltage at the worst voltage drop for $I_2(t)$ and $I_3(t)$, respectively. Compared with the single-current profile scenario, the increased error rate can be caused by the impedance merging method. Even with the slightly increased error, the derived target impedance closely tracks the design expectation. These results verify the proposed method.

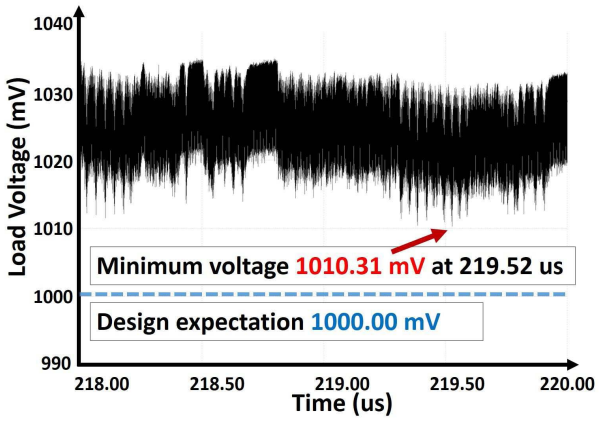

Fig. 32. Worst voltage drop with CRC benchmark profile.

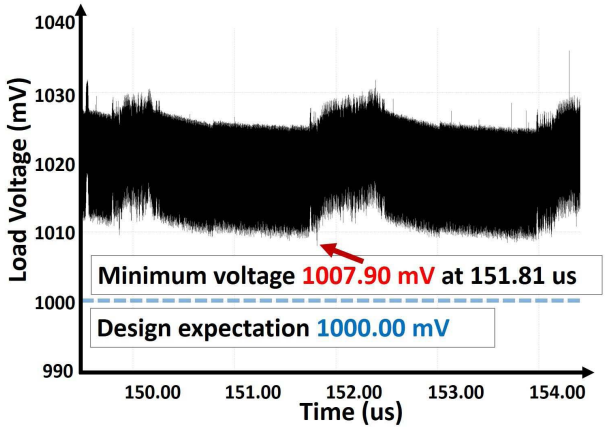

Fig. 33. Worst voltage drop with string-search benchmark profile.

VI. CONCLUSION

This article has proposed a new frequency-dependent target impedance method that satisfies the voltage drop constraints in multiple frequency ranges. Given the voltage drop constraints and load current profiles, frequency-dependent target impedance is derived with the concept of MEF and iterative computation for multiple frequency ranges. We experimentally confirmed that, in the actual processor OpenRISC load case, the synthesized single-stage target impedance satisfies the average voltage drop constraint with 0.02% error, and the overall voltage drop constraint is satisfied with 0.07% error. In the multicore RISC-V processor single-current profile case, the synthesized three-stage target impedance satisfies the voltage drop constraints. The minimum and average voltages are 0.90 and 1.60 mV higher than the design expectations, respectively. Finally, with multiple current profiles and multiple voltage drop constraints, the derived target impedance satisfies voltage drop constraints among different workloads. The average error to the design expectation is 0.99%. These results tightly meeting the given constraints show the effectiveness of the proposed PDN design method.

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