# Impact of the Angle of Incidence on Negative Muon-Induced SEU Cross Sections of 65-nm Bulk and FDSOI SRAMs

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***Abstract*— Muon-induced single event upset (SEU) is predicted to increase with technology scaling. Although previous works investigated the dependencies of muon-induced SEU cross sections on energy, voltage, and technology, the angle of incidence of terrestrial muons is not always perpendicular to the chip surface. Consequently, the impact of the angle of incidence of muons on SEUs should be evaluated. This study conducts negative muon irradiation tests on bulk and fully depleted silicon on insulator static random access memories at two angles of incidence: 0° (vertical) and 45° (tilted). The tilted incidence drifts the muon energy peak to a higher energy as expected. However, the SEU characteristics in the bulk device between the vertical and tilted incidences, including the voltage dependences of the SEU cross sections and multiple cells upset patterns, are similar despite the unexpected impact on the SEU cross section at an operating voltage of 0.4 V.**

***Index Terms*— Angle of incidences, negative muons, single event upset (SEU), static random access memories (SRAMs).**

## I. Introduction

SOFT errors threaten the reliability of terrestrial semiconductor devices. Neutrons are thought to be the main source of soft errors in terrestrial cosmic rays. As the technology scales down, the neutron-induced soft error rate (SER) and single event upset (SEU) cross sections per Mbit have decreased in the last decade [1], [2]. In contrast, we recently demonstrated that the muon-induced SEU cross section per Mbit increases from 65 to 28-nm technology [3]. Therefore, in advanced technologies, the muon-induced soft error should be examined more carefully.

The muon-induced SEU cross sections have attracted much attention. Sierawski *et al.* [4] reported positive muon-induced SEU cross sections measured with 65-, 55-, 45-, and 40-nm bulk complementary metal oxide semiconductor (CMOS) static random access memories (SRAMs). They also investigated the SEU dependence on the supply voltage and muon energy by evaluating 28-nm bulk SRAMs at operating voltages and momentum scanning at RIKEN-Rutherford Appleton Laboratory (RIKEN-RAL) [5]. Gasiot *et al.* [6] studied the positive muon-induced SEU cross sections in 28-nm ultrathin body and buried oxide (UTBB) fully depleted silicon on insulator (FDSOI) SRAMs as well as those on bulk ones. For 3-D tri-gate devices, Seifert *et al.* [2] compared positive muon-induced SEU cross sections measured for 22 and 14 nm to that for 32-nm planar SRAM. Simulation-based SEU evaluations have also been reported. Seifert *et al.* [2] and Serre *et al.* [7] explained recent experimental results of positive muons using the critical charge. Trippe *et al.* [8] predicted a muon-induced SER based on the data from proton tests in a 28-nm SRAM. To investigate the muon-induced SER in a terrestrial environment, Infantino *et al.* [9] evaluated the relationship between the muon-induced SER and the critical charge in a simulation. Similarly, Cavoli *et al.* [10] studied terrestrial cosmic ray-induced SER via simulations and predicted that the muon-induced SER will exceed the neutron-induced one for 22-nm technology.

The above studies focused mainly on the relationship between the SEU cross section and muon energy. On the other hand, the angle of incidence is another factor worth investigating. Like neutrons, because the zenith angle of muons is not always normal to the surface [11], the angle of incidence of muons to a semiconductor device is not always vertical. Focusing on the direct ionization effects of positive and negative muons, a change in the angle of incidence should influence the track on which muons travel inside a chip. Hence, the deposited charge may fluctuate, leading to variations in a muon-induced SEU cross section. On the other hand, the muon

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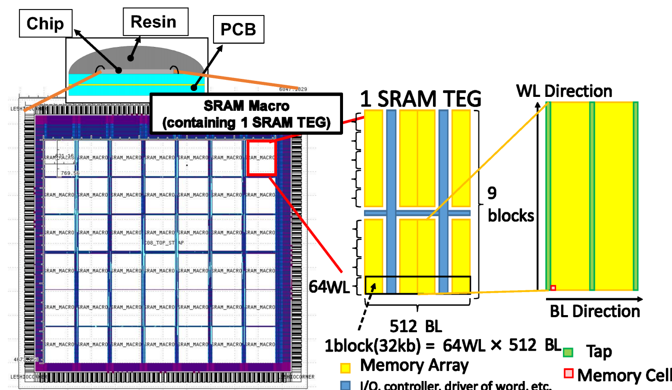


Fig. 1. Structure of bulk and FDSOI SRAM chips. Each chip has 42 SRAM test element groups (TEGs). Each TEG contains a 32-kbit SRAM macro. Bit cell distribution in the macro is shown in the right figure of the array. 2 BL × 64 WL cells share the same well.

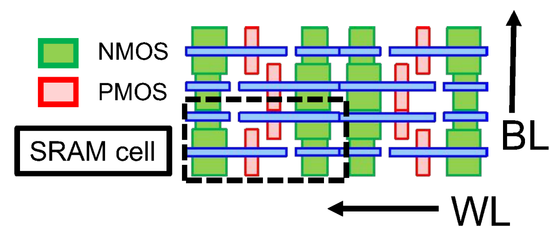


Fig. 2. Layout of 2 × 2 SRAM cells. The SRAM cells are designed with a typical 6T structure.

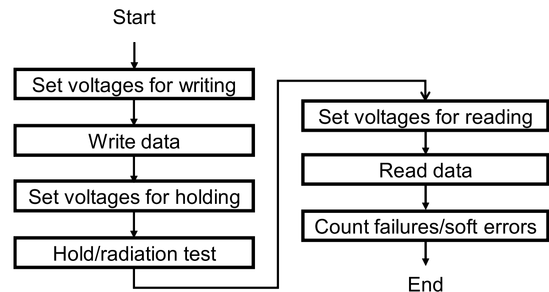


Fig. 3. Test flow. Test can be regarded as static because the hold time is much longer than other times.

capture effect, which is unique to negative muons, is supposed to be angle independent since the low-energy stopping negative muons are captured while secondary ions are emitted in all directions.

In this article, we compare the energy peaks of muons where the muon-induced SEU cross section is maximized as well as the voltage dependences of the SEU cross sections and multiple cells upset (MCU) patterns between 0° (vertical) and 45° (tilted) angles of incidence. Both bulk and FDSOI SRAMs are utilized. Because negative muons have larger SEU cross sections than positive muons and the limited beam time, this work conducts an irradiation campaign using only negative muons. The tilted incidence drifts the muon energy peak to the higher side. However, the voltage dependences of the SEU cross sections and MCU patterns are nearly independent of the angle of incidence, despite an unexpected impact on the SEU cross section at an operating voltage of 0.4 V in the bulk devices.

The rest of this article is organized as follows. Section II describes the SRAM devices, measurement flows, and beam facilities. Section III and IV discuss the experimental results with an emphasis on the energy peak drift and the similarity of the voltage dependences, respectively. Section V concludes this article.

## II. Experimental Setup

The 65-nm bulk and FDSOI SRAM chips were tested using monoenergetic muon beams. These chips were evaluated in [12]–[14]. Compared to the bulk sample, the FDSOI device had a thin insulator layer under the transistor channel. Hence, this FDSOI device is called a silicon on thin buried oxide (SOTB) device [15]. Fig. 1 shows the structure of the tested chips, where each chip contains a 12-Mbit memory cells. The memory cell was designed with a typical 6T SRAM structure. Fig. 2 shows the layout of a 2 × 2 cell. The estimated thresholds of the deposited charges for SEUs were 1.5 and 0.08 fC in bulk and FDSOI devices at 0.5 V, respectively. The charge deposited in the sensitive volume (SV) by muons and their secondary ions were evaluated. These charges differed from the charge collected at the drain terminal. The chips were fabricated using 65-nm technology with eight metal layers and a deep well option. For bulk devices, Gasiot *et al.* [16] reported that deep well options enhance the parasitic bipolar action (PBA) and consequently, it is easier for MCUs with large multiplicities (e.g., 16-bit MCU) in cells containing nMOS transistors to occur in the same P-well compared to those without a deep well. In our chips, 64 bitline (BL) × 2 wordline (WL) cells shared the same N-well.

The beam was given from the printed circuit board (PCB) layer shown in Fig. 1. The reason is explained as follows. The SRAM chips were directly mounted on the PCB and bonded to the PCB wiring patterns instead of using a package. To protect the chip, the chip and bonding wires were capped with resin. Since the resin layer thickness was not constant, the distance from the resin surface to the SV depended on the SRAM cell location, making it difficult to stop every muon at the SV depth. On the other hand, the distance from the PCB surface to the SV was much more uniform. Hence, we irradiated the devices under test (DUT) from the PCB side.

Fig. 3 shows the common measurement flow in the irradiation tests. We conducted static tests with a 600-s hold time for the muon tests. The operating voltages during holding and writing/reading data processes differed. To keep the values stored in the SRAM cells the same after a voltage transition, the voltage transition proceeded slowly, which increased the time by 16 s at most. Regardless of this slow transition, the holding time was much longer. Hence, the tests can be regarded as static. On the other hand, most of the SRAM cells in the bulk device held the data properly at an operating voltage of 0.4 V, whereas the FDSOI device held the data properly at 0.25 V. At such low operating voltages, the total bits (196 Mbit) contained a few hundred unstable bit cells. To exclude such unstable cells, we tested bit failures by writing and reading more than three times before, during (the beam

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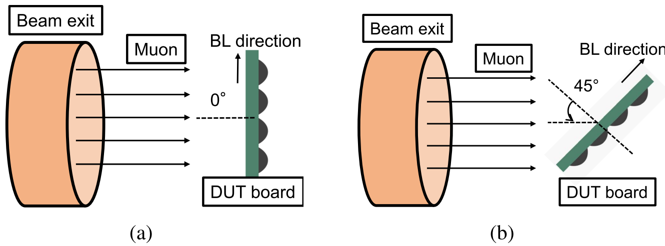


Fig. 4. Beam angle of incidence to the DUT board. 0° and 45° mean the vertical and tilted directions, respectively. At the tilted incidence, the BL direction of the SRAM arrays is also 45° to the beam direction. (a) Vertical incidence (0°). (b) Tilted incidence (45°).

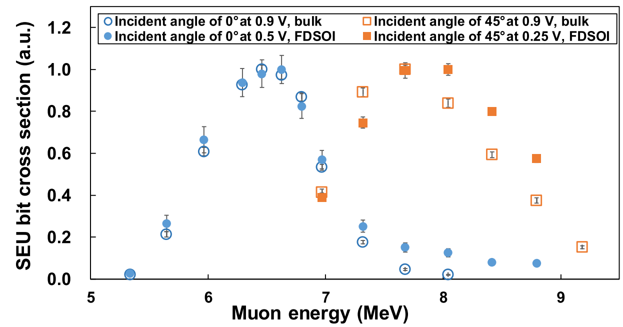


Fig. 5. Dependence of the muon-induced SEU bit cross section on the muon energy in the bulk and FDSOI devices. For each angle of incidence and device, the bit cross section is normalized by the maximum bit cross section. Error bars represent one standard deviation. Peak energy increases from 6.6 to 7.7 MeV when the angle of incidence is changed from 0° (vertical) to 45° (tilted).

stopped), and after the irradiation campaign. Here, the bit failure is defined as the repetitive bit errors in the test runs. For the bit cells with such a failure, the word addresses and the bit locations inside the word were recorded. When calculating the SEU cross sections, the recorded bit cells were excluded.

A negative muon source at Material and Life Science Facility (MLF) [17] of Japan Proton Accelerator Research Complex (J-PARC) was utilized for the irradiation experiments. As we previously reported in [14], the facility produces pions through nuclear reactions between a 3-GeV proton beam and a 20-mm-thick graphite target. The produced pions decay into muons in a long superconducting solenoid magnet. Then, the decay muons are transported downstream to the experimental area. By adjusting the magnetic field, different muon energies are obtained to ensure energy scanning. The energy spectrum of the muon beam follows a normal distribution with a 5% standard deviation [18]. The total flux of the beam measured by two plastic scintillators at almost the same place in the downstream of the DUT boards is similar to [14]. In this study, we counted the coincident charging events of the decay electrons/positrons at both scintillators to exclude the influence of the background and to calculate the flux of muons with a proportional relationship.

Fig. 4 illustrates the incident direction of the beam. The beam was given at two different angles of incidence: 0° (vertical) and 45° (tilted). At the tilted incidence, the beam direction was also 45° with a BL direction of the SRAM arrays. Note that the tilted irradiation along WL was not performed due to the limitations of the DUT holder. At each angle of incidence, energy scanning identified the peak energy, where negative muons stop near the transistors inside the chips and the SEU cross section was maximized. To stop every muon at the same depth inside a chip, the beam was irradiated from the PCB layer. Energy scanning was conducted for both vertical and tilted incident irradiation tests. Because energy scanning was time consuming, the 0° and 45° incident irradiation tests were conducted in separate experiments. We tried our best to place the board at the same position in these two experiments. Due to the power upgrade of the accelerator at J-PARC from 150 to 500 kW, the muon flux increased 2.33× for the tilted incidence test.

To compare the vertical and tilted incidences, the cross section was normalized for each angle of incidence and device. The relative value of the cross section is used in the discussion on the energy and voltage dependences of the SEU cross sections because the muon paths to the SRAM chips differed in the cases of 0° and 45° irradiation, inducing different effects on Coulomb scattering and energy struggling in the device board. The ratio of muons reaching the chips to their total amount depended on the angle. Because the absolute values of the cross sections include these effects, it was difficult to fairly compare the cross sections of the SRAM chip at different angles of incidence. On the other hand, for the cross section comparison between bulk and FDSOI SRAMs, [19] reported that the bulk SRAM has at least 6.5× larger cross section than that of the FDSOI SRAM.

Herein, we define two cross sections. The first one is based on the number of error bits, which is hereafter called the bit cross section. The second is based on the number of events, which is hereafter called the event cross section.

## III. Energy Peak Drift Due to the Tilted Incidence

### A. Experiment Result of Energy Peak Scanning

Fig. 5 shows the SEU bit cross sections induced by negative muons at different energies for vertical and tilted angles of incidence, where the error bars represent one standard deviation. For each angle and device, the cross section is normalized by the maximum cross section in each data set. At each test run for different energies, at least $10^8$ muon$\cdot$cm$^{-2}$ were irradiated to the DUTs. For the bulk devices, the operating voltages of SRAMs were 0.9 V during the energy scanning. On the other hand, in the FDSOI SRAM, the operating voltage was reduced to 0.25 V at the tilted incidence. The cross sections increase 6× as the operating voltage decreases from 0.5 to 0.25 V in the case of the FDSOI SRAM as reported in [14]. Thus, a lower voltage accelerates the scanning process, reducing the required beam time without impacting the muon stopping position or the energy peak. The peak muon energy increases from 6.6 to 7.7 MeV when the angle of incidence is changed in both the bulk and FDSOI devices. Hence, the tilted incidence causes the energy peak drift in the energy dependence of the muon-induced SEU cross sections.

The dominant reason for the energy peak drifting to a larger value may be attributed to the fact that the tilt incidence

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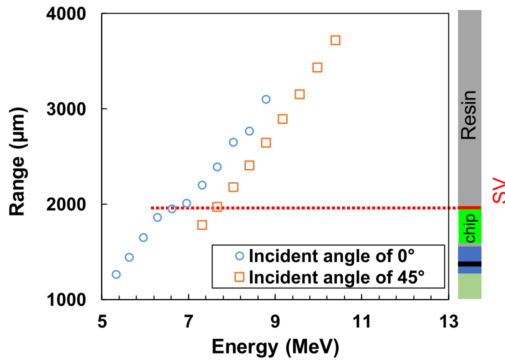


Fig. 6. Relationship between the energy of incident muons and muon stopping position. Energy drift for muons to stop near SV of transistors is clearly observed from 6.6 MeV for the vertical incidence (0°) to 7.7 MeV for the veritical incidence (45°).

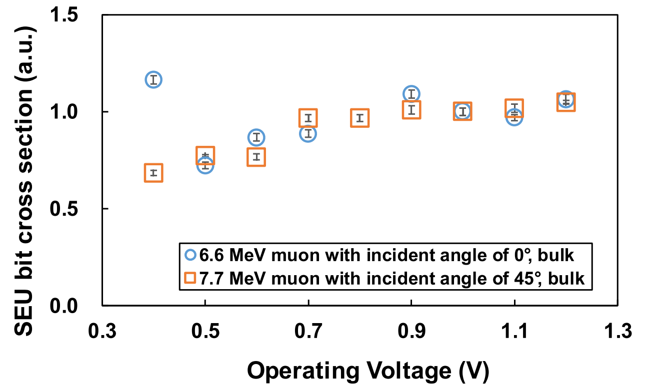


Fig. 7. Dependence of the muon-induced SEU bit cross section on the operating voltage at the vertical (0°) and tilted (45°) incidences in the bulk SRAM. For each angle of incidence, the cross section is normalized by the bit cross section at 1.0 V. Error bars represent one standard deviation.

makes the distance from the PCB to the transistor longer compared with the vertical incidence. As discussed in [12], most negative muons stop near transistors and invoke muon capture reactions at the peak energy. To reach the transistors at the tilted incidence, the muons require a larger energy. Therefore, the energy peak drift may be attributed to the change of stopping energy for muons traveling inside silicon.

### *B. Verification of Stopping Energy Drift With Monte Carlo Simulations*

To verify the hypothesis that the drift peak energy is related to the stopping energy, we evaluated the relationship between the muon energy and stopping position with Monte Carlo simulations using physical heavy ions transport code system (PHITS) [20] simulator. We previously verified our simulation model [12]. To reproduce the irradiation setup, we tried to build the layers inside a chip with the thickness and order the same as the actual chip. The muon sources with different energies were irradiated to the chip from the PCB layer at vertical and tilted angles to investigate their stopping positions.

Fig. 6 plots the relationship between the energy of incident muons and their stopping position. The energy of muons stopping near SV of transistors at 1950 $\mu$m drifts from 6.6 MeV at the vertical incidence to 7.7 MeV at the tilted incidence. For the tilted incidence, the stopping energy estimated with the simulation is consistent with the energy of 7.7 MeV observed in the experiments. Thus, the drift of the peak energy originates from the change in the stopping energy.

## IV. Similarities in SEU Voltage Dependence, MCU Multiplicities, and MCU Patterns

After energy scanning, the muon source of the peak energy was selected for voltage scanning. During voltage scanning, we compared the SEU characteristics including the voltage dependences of the cross sections, MCU patterns, and MCU proportions at the vertical and tilted incidences. Note that due to the small number of MCU events observed in the FDSOI SRAM, the discussion on MCUs is mainly based on the bulk SRAMs. The operating voltages for the bulk SRAM were 0.4 to 1.2 V whereas those for the FDSOI SRAM were only 0.25 and 0.5 V.

### *A. Voltage Dependences of SEU Bit and Event Cross Sections*

Fig. 7 shows the dependence of the muon-induced SEU bit cross section on the operation voltage for the vertical and tilted incidences in the bulk SRAM. For each angle, the cross section is normalized by the cross section at 1.0 V. The error bars represent one standard deviation. The dependence on voltage is almost identical except at an operating voltage of 0.4 V. For the 0° incidence, the SEU bit cross section reached the minimum at 0.5 V, whereas it reached the minimum at 0.4 V for the 45° incidence. Our previous work [12] indicated that the primary mechanism of negative muon-induced SEUs at low voltage is charge collection, but changes to PBA at high voltage. At a higher operating voltage, charge collection is less likely to induce errors due to a higher threshold, namely critical charge, whereas PBA has a higher possibility of inducing MCUs of large multiplicities. Consequently, the bit cross sections for both vertical and tilted incidences increase from the minimum as the operating voltage increase.

Moreover, Fig. 8 shows the separated single bit upset (SBU) and MCU events in the bulk device. Fig. 9 plots the proportion of MCU events to the total events. The voltage dependence of the event cross section is identical except at an operating voltage of 0.4 V.

The similarity is also observed in the FDSOI device at the vertical and tilted incidences. Fig. 10 shows the muon-induced SEU bit cross sections at 0.25 and 0.5 V in the FDSOI SRAM, where the data are normalized by the values at 0.5 V. The cross section decreases by 6.2× and 5.3× at the vertical and tilted incidence, respectively, as the voltage increases from 0.25 to 5 V. Due to the small MCU cross section in the FDSOI SRAM, the MCU event cross section is not elaborated here. Instead, Fig. 11 plots the proportion of MCUs to the total events. Although the error bar is larger due to the small number of MCUs observed in the FDSOI device, the proportions of MCUs are similar for a given voltage regardless of incident angles.

The similar voltage dependences of the bulk and FDSOI SRAMs for the vertical and tilted incidences may be due to the negligible influence of the angle of incidence on muon

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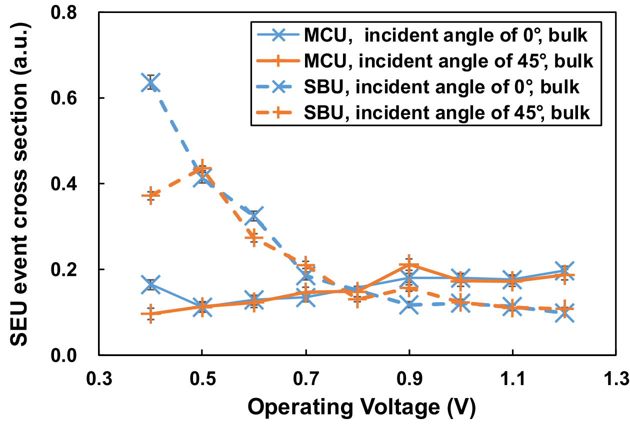


Fig. 8. SBU and MCU event cross section in the bulk SRAMs. For each angle of incidence, the cross section is normalized by the total event cross section at 1.0 V. Error bars represent one standard deviation.

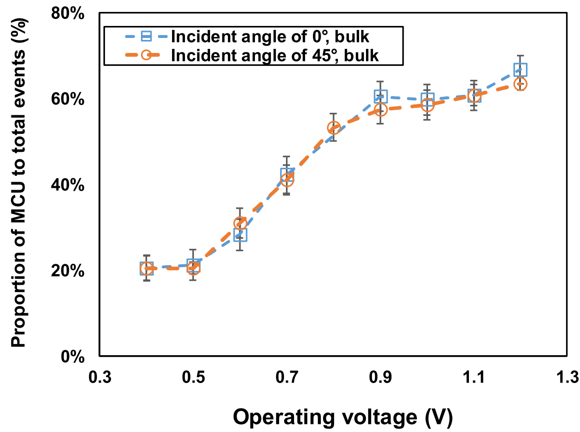


Fig. 9. Proportion of MCUs to the total SEUs including SBUs and MCUs in the bulk SRAM. Voltage dependence of the MCU proportion is the same for both vertical (0°) and tilted (45°) incidence.

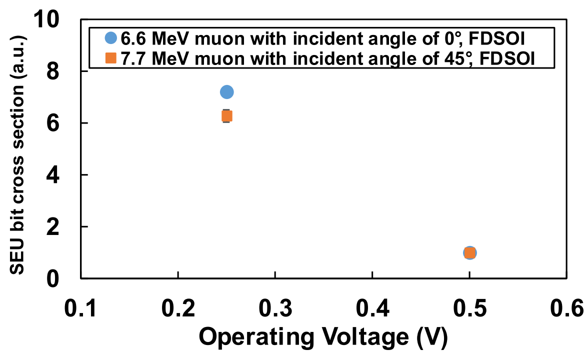


Fig. 10. Muon-induced SEU bit cross section at an operating voltage of 0.25 and 0.5 V at the vertical (0°) and tilted (45°) incidences in FDSOI SRAM. Cross section is normalized by the bit cross section at 1.0 V. Error bars represent one standard deviation.

capture and the secondary ions generated by the muon capture. Since the muon capture requires negative muons to stop, the secondary ions are generated after the negative muon stops. Hence, the direction of secondary ions is isotropic regardless of the incident angle of muon.

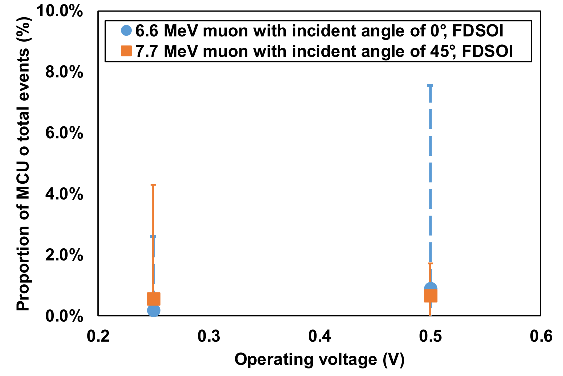


Fig. 11. Proportion of MCUs to the total SEUs including SBUs and MCUs in the FDSOI SRAM. Voltage dependence of MCU proportion is the same for both the vertical (0°) and tilted (45°) incidences. Large error bars are due to small number of MCUs observed in the experiments.

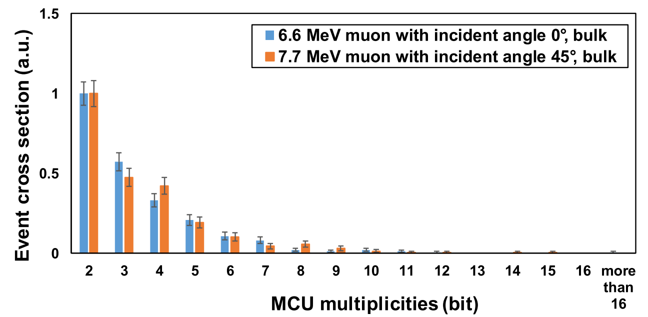


Fig. 12. Event cross sections of MCUs with different multiplicities at 0.4 V for the vertical (0°) and tilted (45°) incidences in the bulk device. Cross sections are normalized by the cross section of 2-bit MCU for each measurement condition. Error bars represent one standard deviation.

In contrast, direct ionization-induced SEUs should be affected by the angle of incidence because the charge deposition track varies and the charge collection efficiency differs spatially. Compared to muon capture, direct ionization deposits less charge as reported in [12]. Hence, its contribution to SEUs increases at lower operating voltage due to a smaller critical charge. This is due to the difference in the SEU cross sections between the vertical and tilted incidences in observed in bulk SRAM operated at 0.4 V (Fig. 7) and FDSOI ones operated at 0.25 V (Fig. 10). Here, direct ionization is the same for both negative and positive muons. Hence, it is possible that a positive muon beam or a more accessible low-energy proton beam can evaluate the angular dependence. However, the results in the study cannot verify this hypothesis as we have not yet performed such experiments. In the future, a positive muon beam and a proton beam to observe whether the tilted incidence causes a more significant decrease in the SEU cross section. Then, the results should be compared with the results of the negative muon reported in this article.

### *B. MCU Multiplicities and Patterns*

The distribution of MCU multiplicities was evaluated to verify the MCU characteristics at the vertical and tilted incidences. Here, the bulk SRAM is used due to the small number of MCU events observed in the FDSOI device. Figs. 12 and 13

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TABLE I

MCU PATTERN CLASSIFICATION IN THE BULK SRAM. PERCENTAGE OF EACH PATTERN IS CALCULATED AS # OF CORRESPONDING MCU EVENTS DIVIDED BY THE TOTAL # OF MCU EVENTS. "–" INDICATES MCU IS NOT OBSERVED IN THE EXPERIMENT

| | | b (%) | w (%) | | | c (%) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | b_x_1_1 | w_1_2_2 | w_1_3_3 | w_1_4_4 | c_x_x_1 | c_x_x_2 | c_x_x_3 | c_x_x_4 | c_x_x_5 |
| 0.4 V | 0° vertical incidence | 22.1 | 16.0 | – | – | 10.6 | 51.1 | 0.2 | – | – |
| | 45° tilted incidence | 22.6 | 14.4 | – | – | 16.1 | 46.6 | – | 0.3 | – |
| 1.0 V | 0° vertical incidence | 14.9 | 8.0 | – | – | 1.1 | 76.0 | – | – | – |
| | 45° tilted incidence | 13.3 | 6.2 | – | – | 2.5 | 77.8 | 0.2 | – | – |

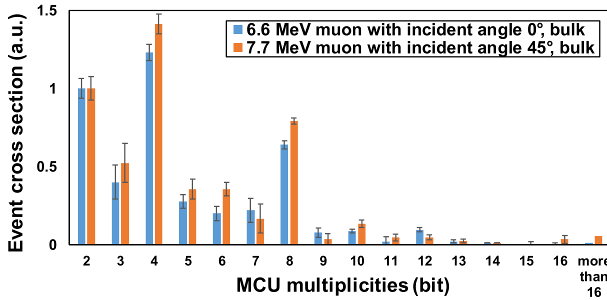


Fig. 13. Event cross sections of MCUs with different multiplicities at 1.0 V for the vertical (0°) and tilted (45°) incidences in the bulk device. The cross sections are normalized by the cross section of 2-bit MCU for each measurement condition. Error bars represent one standard deviation.

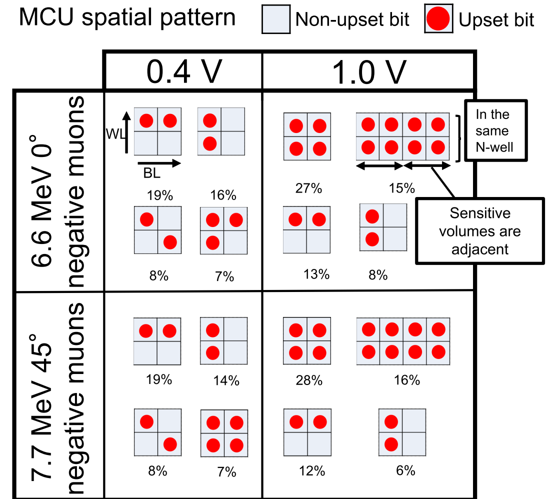


Fig. 14. Top four most frequent patterns of MCUs in the bulk SRAMs. Patterns and frequencies are voltage-dependent but angular independent. The results show the similarity of the MCU patterns in the vertical (0°) and tilted (45°) incidences.

show the event cross sections of the corresponding multiplicity at operating voltages of 0.4 and 1.0 V for the vertical and tilted angles of incidence, where the cross sections are normalized by the cross section of 2-bit MCU for each measurement condition. The distributions of MCU multiplicities are similar, and the difference between the two incidences can be explained by statistical uncertainty.

Furthermore, we counted the patterns of MCUs in the bulk device. Fig. 14 depicts the four most frequent patterns. Note that the MCU patterns in the FDSOI device are not shown due to the small number of observed MCUs. The frequencies and patterns of MCUs are similar for a given operating voltage and are almost angular-independent. On the contrary, the fourth-frequent pattern differs at 0.4 V. The proportion of the 4-bit pattern in $2 \times 2$ rectangle is 6% for the vertical incidence and that of 3-bit pattern in an "L" shape is 4% for the tilted incidence. Thus, the difference for the frequent MCU patterns is small at vertical and tilted incidences.

Finally, we examined the MCU patterns with respect to the BL and WL directions. We categorized the MCUs according to the width and the number of the upsets in BL and WL. Referring to the MCU classification in [1] and [13] and counting the upset numbers along the same WL, the MCU categories are defined as

$$\text{TYPE_}N_1\text{_}N_2\text{_}N_3 \quad (1)$$

where TYPE is the category consisting of b/w/c. Here, categories b, w, and c stand for a single line along BL, a single line along WL and a cluster. A cluster represents an MCU with two or more bits along both the BL and WL directions. $N_1$ is the width in the BL direction, $N_2$ is the width in the WL direction, and $N_3$ is the maximum upset number along the same WL in a single MCU event.

Table I shows the classification results. The proportion distribution is similar for the vertical and the tilted incidences. The similarity in the MCU classification is consistent with the other analysis on MCUs. The 45° angle of incidence is tilted to the BL line, but an obvious increase of MCUs along the BL direction (b_x_1_1) is not observed for the tilted incidence.

As discussed in [12], the muon capture effect can cause MCUs, but not direct ionization due to its small charge deposit. The experimental results regarding MCUs in this article are independent of the angle of incidence. Thus, negative muons contribute to MCUs equally regardless of the angle of incidence. These results are consistent with our expectation that the emission of secondary ions does not have directivity because low-energy stopping negative muons are captured.

## V. CONCLUSION

Herein, we conducted vertical and tilted incidence tests using a negative muon source to evaluate the impact of the angle of incidence on the SEU cross section in bulk and FDSOI SRAMs for a better understanding of the terrestrial muon-induced soft error. In both the bulk and FDSOI devices, the tilted incident causes the muon energy peak where the SEU

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cross section is maximized to drift to a higher one compared to the vertical incidence. On the other hand, the angle of incidence does not affect the voltage dependence of the SEU cross section in neither the bulk nor the FDSOI device except for the trend in the SEU bit and event cross sections between 0.5 and 0.4 V. In the bulk SRAM, a decreasing trend is observed in SEU bit and event cross sections from 0.5 to 0.4 V at a tilted incidence, but an increasing trend arises at a vertical incidence. This difference requires further experiments to identify the origin such as an additional irradiation experiment using positive muons. As for multiplicities and patterns of MCUs, they are independent of the angle of incidence, suggesting that the direction of secondary ions generated by the muon capture process is independent of the angle of incidence of the primary muon.

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