Angular Sensitivity of Neutron-Induced Single-Event Upsets in 12-nm FinFET SRAMs With Comparison to 20-nm Planar SRAMs

Takashi Kato, Masanori Hashimoto, *Senior Member, IEEE*, and Hideya Matsuyama

***Abstract*— The angular sensitivity of neutron-induced single-event upsets (SEUs) is studied in 12-nm FinFET SRAMs. Irradiation experiments are performed using a terrestrial environment-compatible source with varying incidence angles. The analyses of the occurrence rates of SEUs and multiple-bit upsets (MBUs) demonstrate that although the SEU rate decreases at grazing incidence, the MBU rate increases when the incidence direction is parallel to the word lines (WLs) of the SRAM array, as similarly observed in our previous experiments for 20-nm planar SRAMs. It is found that the angular response of multiple-cell upsets (MCUs) is different between the 12-nm FinFET and 20-nm planar SRAMs. The comparative analysis of the voltage dependence of the MCU ratio reveals that this difference is due to the different contribution of parasitic bipolar effects (PBEs), which are more significant in the 20-nm planar SRAMs. It is also indicated that in the 12-nm FinFET SRAMs, the contribution of PBEs is relatively large when the incidence angle is parallel to the WLs. Through the characterization of the MCU events, the validity of this picture is confirmed based on the voltage dependence of the pattern-wise MCU ratio with the consideration of the impact of PBEs on fail bit patterns.**

***Index Terms*— CMOS, FinFET, multiple-bit upset (MBU), multiple-cell upset (MCU), neutron, parasitic bipolar effect (PBE), single-event upset (SEU), SRAM.**

I. Introduction

FinFET technologies have shown a drastic improvement in single-event upset (SEU) tolerance compared to former bulk planar technologies [1]–[8]. This improvement is mainly due to fin structures, which lead to the reduced sensitive volume [5], [9], [10]. Another important aspect of the fin structure is strong anisotropy in the fin shape. It has been reported that this structural anisotropy results in unique angular sensitivity of heavy-ion-induced SEUs in bulk FinFET devices [11], [12]. Zhang *et al.* [11] investigated the angular response of SEU cross sections for heavy ions using 16-nm bulk FinFET flip-flops. They showed that the angular sensitivity was different for particles with different linear energy transfers (LETs), where for low-LET particles the SEU cross section decreased at grazing incidence along the direction perpendicular to the fin. Nsengiyumva *et al.* [12] also investigated the angular response for heavy ions using 14-nm/16-nm bulk FinFET latches. They clearly demonstrated that the SEU cross section depended on the incidence angle only for low-LET particles, where the SEU cross section increased (decreased) at grazing incidence when the incidence direction was parallel (perpendicular) to the fin.

In the terrestrial environment, high-energy neutrons are the major source for SEU events. As for bulk planar devices, there are several reports investigating the angular responses of neutron-induced SEUs, where the forward emission of secondary ions is considered to be the key mechanism [13]–[16]. Regarding bulk FinFET devices, on the other hand, such angular responses have not been investigated. Here, as mentioned above, the angular sensitivity is significant for low-LET particles in FinFET devices [11], [12]. This indicates the possibility of the notable angular sensitivity of terrestrial neutron-induced SEUs for FinFET devices because most of the secondary ions produced by incident neutrons are low-LET particles. Therefore, it is worthwhile to investigate the angular sensitivity of neutron-induced SEUs in bulk FinFET technologies.

For SRAM devices, multiple-cell upsets (MCUs) are a serious concern for SRAM reliability. This is because simple error-correction codes (ECCs) cannot correct multiple-bit upsets (MBUs), which are a type of MCUs where multiple fail bits occur in the same logical word. In bulk planar SRAM devices, it has been demonstrated that the characteristics of neutron-induced MCUs are strongly dependent on the incidence angle of neutrons: the occurrence probability of MCUs increases at grazing incidence [13]–[15]. The authors have recently shown that the MCU characteristics depend on whether the incidence direction is parallel to the word lines (WLs) or the bit lines (BLs) of SRAM devices in a 20-nm bulk planar technology: the MBU rate increases when the incidence direction is parallel to the WLs [16]. In bulk FinFET SRAM devices, several studies have reported the MCU characteristics [7], [17], [18]. However, the impact of the incidence direction on MCUs has not been explored. Considering the structural difference between planar and FinFET transistors, FinFET SRAM devices could possess different types of angular MCU

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Takashi Kato is with the Reliability and Quality Assurance Department, Socionext Inc., Kawasaki 213-0012, Japan, and also with the Department of Information Systems Engineering, Osaka University, Suita 565-0871, Japan (e-mail: kato.takashi@socionext.com).

Masanori Hashimoto is with the Department of Information Systems Engineering, Osaka University, Suita 565-0871, Japan.

Hideya Matsuyama is with the Reliability and Quality Assurance Department, Socionext Inc., Kawasaki 213-0012, Japan.

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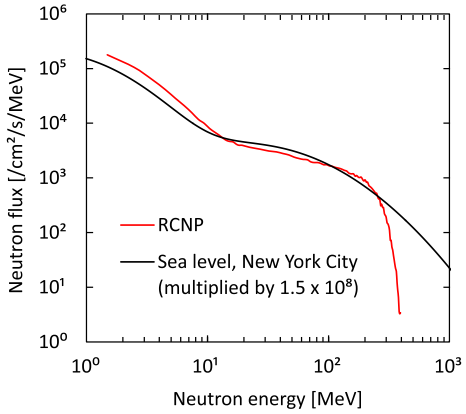

Fig. 1. Neutron energy spectrum of spallation neutron beam at RCNP (red line) [24] and terrestrial neutron at sea level, New York City (black line) [25] (after [16]).

sensitivity in such incidence conditions because typically the BLs (WLs) is parallel (perpendicular) to the fin.

At the same time, since the difference in charge collection processes could result in the difference in MCU characteristics, it is important to consider physical mechanisms underlying MCU events. It is well known that, as devices scale down, parasitic bipolar effects (PBEs) have become more active. In bulk planar SRAM devices, PBEs have significant impact on MCU characteristics [19]–[23]. In bulk FinFET SRAM devices, there have been no studies analyzing the MCU characteristics from the point of view of the PBE contribution. Hence, it should be meaningful to investigate the angular sensitivity of MCU characteristics in terms of both structural effects and PBEs.

This article experimentally investigates neutron-induced SEUs in 12-nm bulk FinFET SRAMs for several angles of incidence. The angular sensitivities of the SEUs, MCUs, and MBUs are evaluated by irradiation tests using an atmospheric-like neutron beam. The occurrence rates of SEU, MCU, and MBU events are statistically analyzed in terms of the dependence on the power supply voltage (VDD) and the incidence angle. To find out the difference in the angular sensitivity between planar and FinFET devices, the obtained results are compared with the results of previous experiments for the 20-nm bulk planar SRAMs [16]. Based on the difference observed in the voltage dependence of the MCU ratio between the 12-nm FinFET and 20-nm planar SRAMs, the underlying mechanism is discussed, focusing on the contribution of PBEs. Furthermore, the MCU characteristics are thoroughly analyzed with respect to the size and fail bit pattern of the MCU events. The contribution of PBEs is also examined in terms of the voltage dependence of the pattern-wise MCU ratio.

II. Experimental Setup

A. Neutron Irradiation

Neutron irradiation testing was performed at the Research Center for Nuclear Physics (RCNP), Osaka University. The spallation neutron beam was used in all the tests. As shown in Fig. 1, the energy spectrum is similar to the terrestrial one in the energy range from 1 to 300 MeV [24]. The integrated flux above 10 MeV was $\sim 2.5 \times 10^9$ cm^2/h. The test vehicles were SRAM chips fabricated in a 12-nm bulk FinFET CMOS process. The package was a standard plastic package. The SRAM chips were irradiated by the neutron beam at three angles of incidence: 0°, 90° (WL), and 90° (BL). These geometrical configurations are schematically illustrated in Fig. 2(a)–(c). The angle of 0° is the direction normal to the silicon die [Fig. 2(a)]. The angles of 90° (WL) and 90° (BL) are the directions parallel to the WLs and BLs of the SRAM cells, respectively [Fig. 2(b) and (c)]. Note that the neutron beam and the irradiation configurations were the same as the previous experiments for the 20-nm bulk planar SRAMs [16].

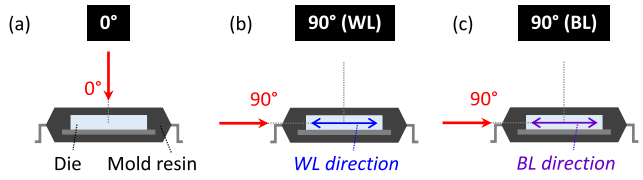

Fig. 2. Neutron incidence angles of three irradiation conditions: (a) 0°, (b) 90° (WL), and (c) 90° (BL). Red arrows represent the direction of neutron beam. (a) 0° is the normal incidence from the top. (b) 90° (WL) and (c) 90° (BL) are for incidences parallel to WLs and BLs, respectively. Note that (c) 90° (BL) is the case where the direction of neutron beam is parallel to the fin direction.

As described in Section I, a key point for the angular sensitivity of SEUs in FinFET devices could be the relative angle between the incidence direction and the fin orientation. In our experimental configuration, the angles of 90° (BL) and 90° (WL) correspond to the cases where the neutron beam is parallel and perpendicular to the fin, respectively.

B. SRAM Operation

The SRAM operation consisted of, in order, write, hold, and read cycles. The test mode was static, i.e., no read operation during hold cycles. Two types of data patterns were used, which were labeled as All0 and CKB0. In the case of the All0 pattern, a logical "0" was written in all the bits. In the case of the CKB0 pattern, logical "0" and "1" were arranged in a checkerboard fashion, where "0" was written in the first bit. The number and physical locations of fail bits were obtained from the error information collected in the read cycle. The single-bit upset (SBU) and MCU events were then extracted separately through the SEU analysis based on the spatial distribution of fail bits. In our analysis, the MBU events correspond to the MCU events in which multiple fail bits occur in the same WL. It should be noted that the number of fail bits accumulated during one hold cycle was kept small enough to avoid the misinterpretation of multiple SBU events as an MCU event.

The calculation of the SEU, MCU, and MBU rates was performed according to the JEDEC standard [25]. The SEU rate was given as $\sigma_{\mathrm{SEU}} \times \phi_{\mathrm{n}}$, where σ_{SEU} and ϕ_{n} are the SEU cross section and the neutron flux of interest, respectively. Here, σ_{SEU} was obtained as $N_{\mathrm{SEU}}/(\Phi_{\mathrm{n}} \times N_{\mathrm{bit}})$, where N_{SEU} is the number of the observed SEU events, Φ_{n} is the incident neutron fluence, and N_{bit} is the number of bits irradiated.

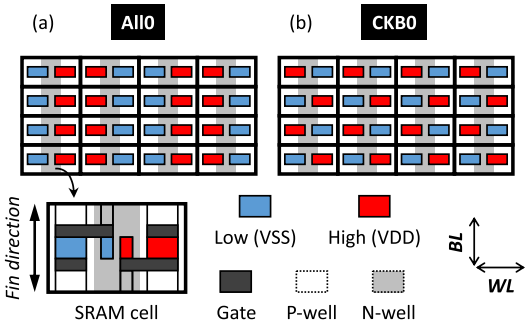

Fig. 3. SRAM node voltages for (a) All0 and (b) CKB0 patterns. Rectangular cells correspond to SRAM cells. The schematic illustration of the cell layout is shown in the lower part. Vertical and horizontal directions are parallel to BLs and WLs, respectively. Blue and red rectangular boxes denote the internal nodes of low (VSS) and high (VDD) voltages, respectively. White and gray regions depict p-wells and n-wells, respectively.

The physical arrangement of internal node voltages is one of the important information for the discussion on MCU characteristics [16]. The voltage arrangements for the All0 and CKB0 patterns are explained in Fig. 3(a) and (b), respectively. In each figure, the 4 rows × 4 columns SRAM array is depicted with rectangular cells, where blue and red rectangular boxes represent low (VSS) and high (VDD) states of internal nodes, respectively. In the case of the All0 pattern, two high nodes of two horizontally adjacent SRAM cells share the same p-well. The VDD was varied from 0.5 to 0.9 V. Note that the above conditions, except for the VDD condition, were the same as the previous experiments for the 20-nm bulk planar SRAMs [16].

III. Results and Discussion

A. Angular Responses of SEU, MCU, and MBU Rates

The voltage dependencies of the SEU, MCU, and MBU rates for the incidence angles of 0°, 90° (WL), and 90° (BL) are shown in Fig. 4(a)–(c), where the SEU rate is the sum of the SBU and MCU rates. The results for both the 12-nm FinFET and 20-nm planar SRAMs are presented in each graph. As demonstrated in Fig. 4(a), the SEU rate for the 12-nm FinFET SRAMs was lower by approximately one order of magnitude than that for the 20-nm planar SRAMs. This is consistent with the previous report and probably due to the structure transition from planar transistors to fin ones [8]. As for the angular dependence, the difference for the SEU rate was not so significant, as seen in Fig. 4(a). For both the SRAMs, the SEU rate decreased at grazing incidence. On the other hand, a noticeable difference was observed for the MCU rate, as seen in Fig. 4(b). These points will be examined later.

As for the MBU rate shown in Fig. 4(c), as is the case in the 20-nm planar SRAMs, the angle of 90° (WL) had the highest rate in the 12-nm FinFET SRAMs. This can be explained by the forward emission of secondary ions because MBU events are the events where multiple fail bits occur along a WL [16]. This is an important observation indicating that, in the terrestrial environment, the device orientation can be an important factor for estimating the efficiency of ECCs in the 12-nm FinFET SRAMs, as well as in the 20-nm planar

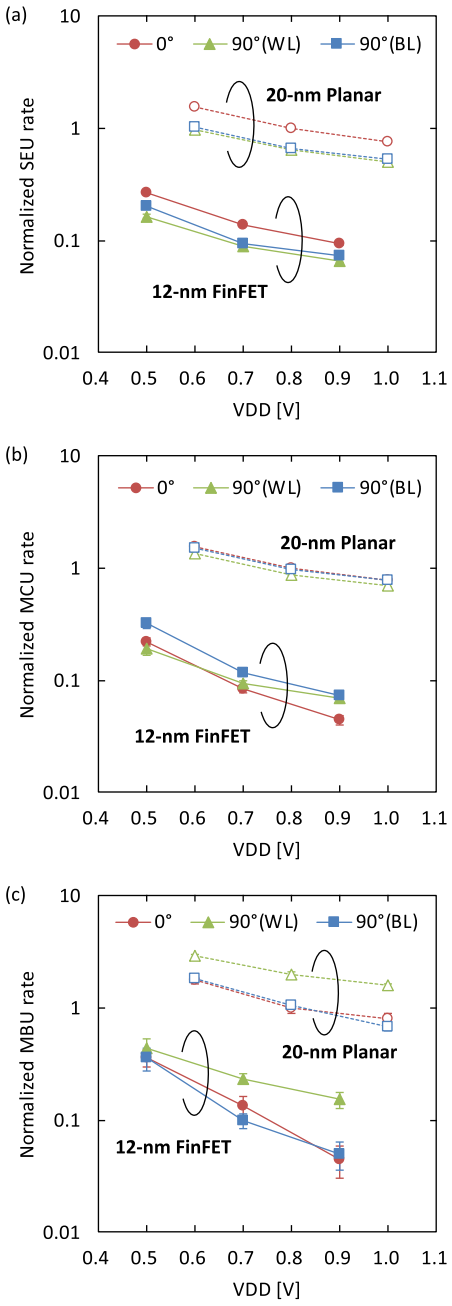

Fig. 4. (a) SEU, (b) MCU, and (c) MBU rates as a function of VDD for the neutron incidence of 0°, 90° (WL), and 90° (BL). Filled and open symbols are for 12-nm FinFET and 20-nm planar SRAMs [16], respectively. Each rate is normalized by the value at 0.8 V of 20-nm planar SRAMs at the angle of 0°. All rates are the values averaged over the All0 and CKB0 patterns. Error bars represent one standard error.

SRAMs. This is because the angular distribution of terrestrial neutrons is anisotropic, where a large number of neutrons strike perpendicular to the ground [26]. Based on the above results, it can be deduced that the vertically mounted SRAM chips with the WLs perpendicular to the ground are the worst condition in terms of the efficiency of ECCs.

The angular sensitivities are highlighted in Fig. 5, where the ratios of the SEU, MCU, and MBU rates at the angles of 90° (WL) and 90° (BL) to those at the normal incidence (0°) are

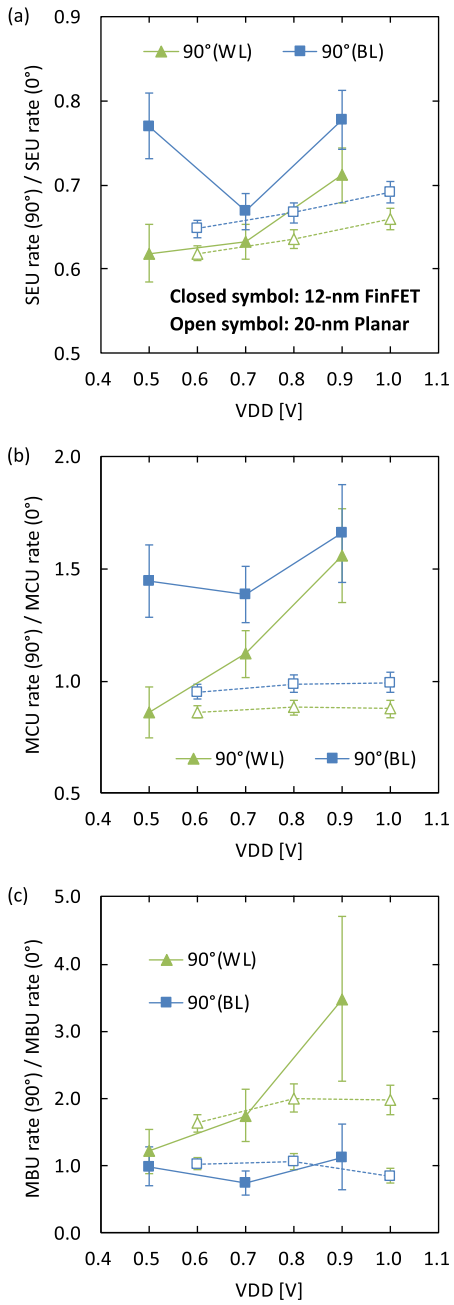

Fig. 5. Ratios of (a) SEU, (b) MCU, and (c) MBU rates for the incidence angles of 90° (WL) and 90° (BL) with respect to the normal incidence case (0°) as a function of VDD. Filled and open symbols are for 12-nm FinFET and 20-nm planar SRAMs, respectively. All rates and ratios are values averaged over the All0 and CKB0 patterns. Error bars represent one standard error. Note that the vertical scales differ.

plotted as a function of VDD. Fig. 5(a) shows that all the ratios for the SEUs are <1. This is obvious from the difference in the visible cross section of the test chip to the neutron beam: the number of neutrons passing through the SRAM cells in a unit of time decreases at grazing incidence.

An interesting observation in the 12-nm FinFET SRAMs is that the gap between the angles of 90° (BL) and 90° (WL) is significant at 0.5 V since the ratio of 90° (BL) is high at 0.5 V. At a lower supply voltage, the critical charge becomes smaller, and hence, the contribution of low-LET secondary particles becomes relatively larger. In this case, the above observation is qualitatively consistent with Nsengiyumva's results of heavy-ion irradiation experiments [12], i.e., for low-LET particles, the SEU cross section increased at grazing incidence when the incidence direction was parallel to the fin. This behavior was explained based on the relative geometry between the fin shape and the particle track [12]. The essence of this geometrical effect is that the particle incidence parallel to the fins results in the long track inside the fin, which increases the charge deposition in the sensitive volume.

More specifically, considering Nsengiyumva's results together with the forward emission of the secondary particles, it is expected that the SEU rate at the lower voltage is higher when the direction of neutron incidence is parallel to the fin than when that is perpendicular to the fin. In our experiments, the rate for the angle of 90° (BL) was higher than that for the angle of 90° (WL) at 0.5 V, where the angle of 90° (BL) corresponds to the incidence direction parallel to the fin. Thus, the observed difference between the angles of 90° (WL) and 90° (BL) is thought to originate from the geometrical effect due to the anisotropy of FinFET structures.

As for the MCUs presented in Fig. 5(b), there are two interesting differences between the 12-nm FinFET and 20-nm planar SRAMs. One difference is that the ratio for the 12-nm FinFET SRAMs is higher than that for the 20-nm planar SRAMs across the range of VDD. This is possibly due to the size scaling of SRAM cells. Since the cell size of the 12-nm FinFET SRAMs is smaller than that of the 20-nm planar SRAMs, the number of cells on each particle track is larger for the 12-nm FinFET SRAMs. In other words, the occurrence probability of MCU events for the 12-nm FinFET SRAMs is more sensitive to the scattering direction of secondary ions, i.e., the incidence direction of neutrons. Another difference is found in the voltage dependence of the ratio. In the 20-nm planar SRAMs, the voltage dependence was small and similar between the angles of 90° (WL) and 90° (BL). On the other hand, in the 12-nm FinFET SRAMs, the voltage dependencies at the two angles differ each other. The ratio at the angle of 90° (WL) clearly increases with increasing voltage. This point will be discussed in Section III-B.

Fig. 5(c) shows the angular sensitivity for the MBUs. For the angle of 90° (BL), the ratio is ∼1 and almost the same between the 12-nm FinFET and 20-nm planar SRAMs. On the other hand, for the angle of 90° (WL), the ratio is meaningfully higher for the 12-nm FinFET SRAMs at 0.9 V, implying that the increase in the MBU rate at grazing incidence can be more significant for the 12-nm FinFET SRAMs at high voltage region.

B. Analyses of MCU Ratios and Consideration of Mechanism

To understand the large difference observed in the angular sensitivity of the MCUs between the 12-nm FinFET and 20-nm planar SRAMs, analyses focusing on the probability of MCU events were performed.

The MCU ratios, which were calculated by dividing the MCU rate with the SEU rate, are presented for the 12-nm

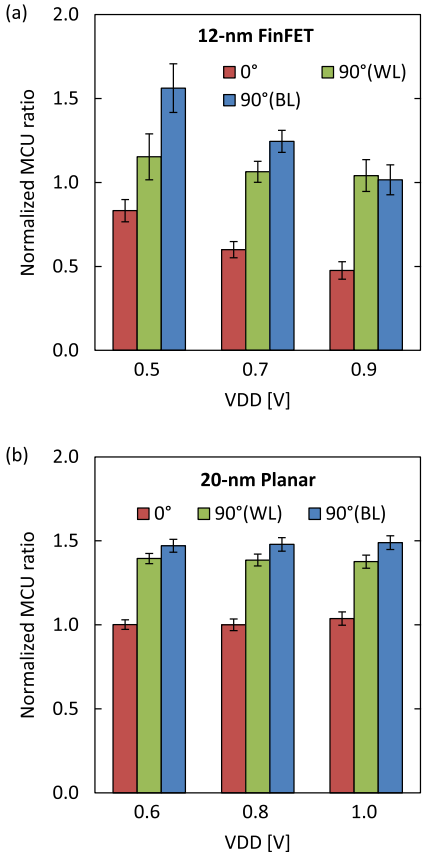

Fig. 6. MCU ratios of (a) 12-nm FinFET and (b) 20-nm planar [16] for the neutron incidence angles of 0°, 90° (WL), and 90° (BL). The ratios are normalized by the value at 0.8 V of 20-nm planar SRAMs in the angle of 0°. All ratios are the values averaged over the All0 and CKB0 patterns. Error bars represent one standard error.

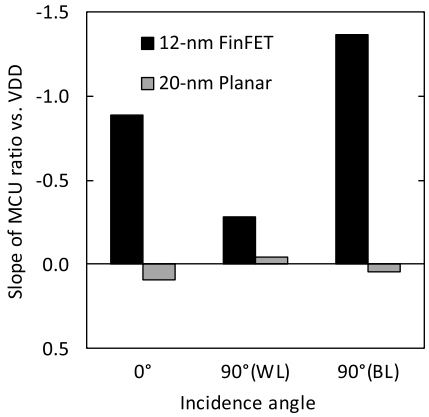

Fig. 7. Slope of the linear fitting of MCU ratio versus VDD (Fig. 6). Black and gray bars correspond to 12-nm FinFET and 20-nm planar SRAMs, respectively. Note that the vertical axis is inverted: the upper side is negative and means a decreasing trend with voltage.

FinFET and 20-nm planar SRAMs in Fig. 6. For both the SRAMs, it is observed that the MCU ratios are higher at the angles of 90° (WL) and 90° (BL) than at the angle of 0°, where the angle of 90° (BL) has the highest ratio. This indicates that the interrelationship between the forward emission of secondary ions and the rectangular geometry of SRAM cells is the primary factor determining the angular response of neutron-induced MCUs in the 12-nm FinFET SRAMs, as well as in the 20-nm planar SRAMs [16].

Taking into account the size scaling of SRAM cells, the MCU ratio is expected to become higher for the 12-nm FinFET SRAMs than for the 20-nm planar SRAMs. However, Fig. 6 shows that the MCU ratio is higher for the 20-nm FinFET SRAMs than for the 12-nm planar SRAMs in almost all the conditions.

Furthermore, a considerable difference between the two SRAMs is found in the voltage dependence of the MCU ratio. In the 20-nm planar SRAMs [Fig. 6(b)], the MCU ratios are almost independent of the voltage. In the 12-nm FinFET SRAMs [Fig. 6(a)], the MCU ratios tend to decrease with increasing voltage. This point is emphasized by comparing the slopes of these voltage dependencies in Fig. 7. The slopes were extracted by linear fitting of the MCU ratio versus the voltage. As seen in Fig. 7, the slopes for the 20-nm planar SRAMs are ∼0 regardless of the incidence angle. In contrast, the slopes are negative values for the 12-nm FinFET SRAMs. Another noteworthy feature is the difference in the magnitude of the slopes among the incidence angles in the 12-nm FinFET SRAMs. It is clearly observed that the voltage dependence of MCU ratio is smaller at the angle of 90° (WL) than at the angle of 90° (BL).

A potential mechanism underlying these features is PBEs because this mechanism affects both the magnitude and voltage dependence of MCU ratios [27], [28]. One of the key points is that the action of PBEs tends to induce MCU events. The large contribution of PBEs can lead to the increase in the MCU ratio. Another key point is that PBEs become more active with increasing the supply voltage. For these reasons, in terms of the slope of the MCU ratio versus the supply voltage, the slope is expected to increase positively as the contribution of PBEs becomes significant. Based on this consideration, the contribution of PBEs can be discussed in Figs. 6 and 7.

In the comparison between the 12-nm FinFET and 20-nm planar SRAMs, the magnitude of the MCU ratio is larger for the 20-nm planar SRAMs and the slope is a more negative value for the 12-nm planar SRAMs. This indicates that the contribution of PBEs is smaller for the 12-nm FinFET SRAMs than for the 20-nm planar SRAMs. This is reasonable from the structural viewpoint. In FinFET structures, the potential inside the fin is well controlled by the surrounding gate. This can lead to the suppression of PBEs because PBEs are induced by the perturbation of the potential.

As for the comparison between the incidence angles of 90° (WL) and 90° (BL) in the 12-nm FinFET SRAMs, it can be deduced that PBEs are less significant at the angle of 90° (BL) compared to the angle of 90° (WL) because the slope shows higher negative value for the angle of 90° (BL), as seen in Fig. 7. With regard to the normal incidence (0°), the slope is the intermediate value between the angles of 90° (WL) and 90° (BL). In the case of the normal incidence, the fractions of secondary ions scattered along the WLs and BLs are equal. In this view, the average response of the angles of 90° (WL)

and 90° (BL) is expected. Therefore, it can be said that the observed slope is consistent with this physical configuration. The important point is that the difference in the slope between the angles of 0° and 90° (WL) leads to the large difference in the MCU ratio at higher voltage, as seen in Fig. 6(a). The strong voltage dependence in the angular response of MCUs for the angle of 90° (WL), as shown in Fig. 5(b), reflects this point. In other words, the difference in the angular responses of MCUs observed in Fig. 5(b) is possibly due to the different contribution of PBEs.

It could be helpful to note that the observed differences in the voltage dependence of the MCU ratio cannot be explained by the critical charge. Since the critical charge increases with increasing voltage for both the SRAMs, the effect of the critical charge can lead to the suppression of the MCU occurrence at high voltage. Also, obviously, the critical charge does not depend on the direction of neutron incidence. Thus, the critical charge is not a dominant factor to explain the differences discussed above.

C. Angular Response of MCU Characteristics

As mentioned in Section I, both the incidence direction of neutrons and PBEs have considerable influence on the MCU characteristics. Therefore, it is worthwhile to compare the angular response of MCU events in terms of their sizes and fail bit patterns between the 12-nm FinFET and 20-nm planar SRAMs.

Fig. 8 shows the multiplicity distributions of the MCU events for the incidence angles of 0°, 90° (WL), and 90° (BL), where 100% corresponds to the total MCU events. Fig. 8(a) and (b) are for the 12-nm FinFET and 20-nm planar SRAMs, respectively. Similar to the 20-nm planar SRAMs, the multiplicity for the 12-nm FinFET SRAMs increases at the angles of 90° (WL) and 90° (BL) compared to the normal incidence (0°). This indicates the influence of forward emission of secondary ions, as discussed in [16]. Focusing on the comparison of the magnitude of the ratio, the ratios of large-multiplicity events are higher for the 20-nm planar SRAMs than for the 12-nm FinFET SRAMs. This is inconsistent with the general view that the size scaling of SRAM cells results in the larger size of MCU events.

One possible interpretation for this observation is the difference in the secondary ions contributing to SEUs. For FinFET devices, the contribution of high-LET particles to SEU events is relatively larger than that for planar devices [6]. Among the secondary ions produced by neutron-induced spallation reactions, the scattering range of high-LET particles is shorter than that of low-LET particles, such as protons and alpha particles. This can lead to the lower ratio of large-multiplicity events in the 12-nm FinFET SRAMs. Another possible interpretation is the impact of PBEs. In Section III-B, it has been suggested that the contribution of PBEs is higher for the 20-nm planar SRAMs than for the 12-nm FinFET SRAMs, which is consistent with the results of the multiplicity distributions because PBEs can increase not only the total MCU ratio but also the occurrence probability of large-multiplicity events [20].

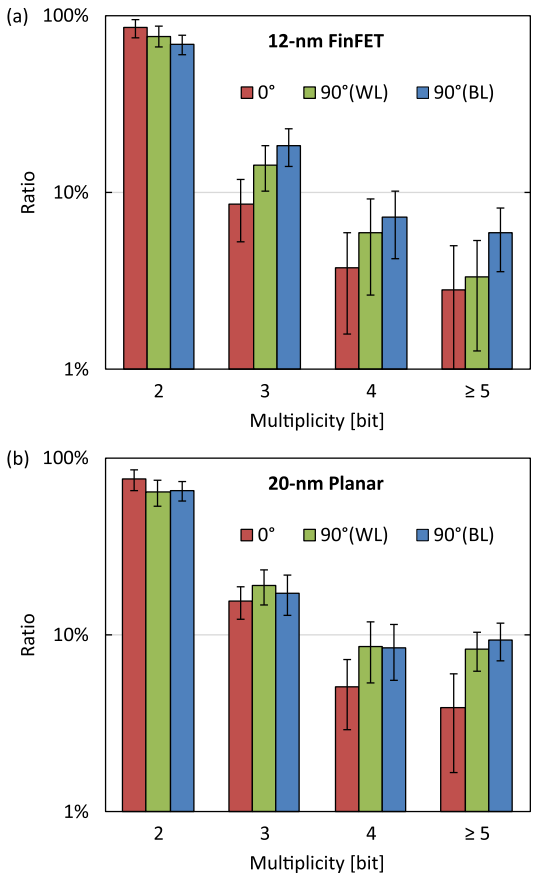

Fig. 8. Multiplicity distributions of neutron-induced MCU events. (a) 12-nm FinFET and (b) 20-nm planar SRAMs. Red, green, and blue bars correspond to the incidence angles of 0°, 90° (WL), and 90° (BL), respectively. All ratios are the values averaged over the All0 and CKB0 patterns and all VDD conditions. Error bars represent one standard error.

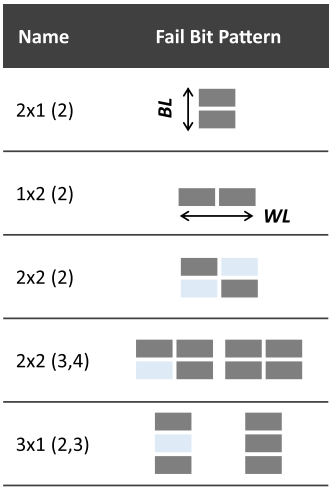

Fig. 9. Groups of fail bit patterns. Rectangular cells are SRAM cells. Gray cells represent fail bits. Vertical and horizontal directions are parallel to BL and WL directions, respectively. The mirror images of each pattern are included in the same group.

The fail bit patterns were analyzed, and MCU events with the patterns shown in Fig. 9 were extracted. There are five MCU groups with different fail bit patterns, which are named as BL-range × WL-range (number of fail bits). Note that the

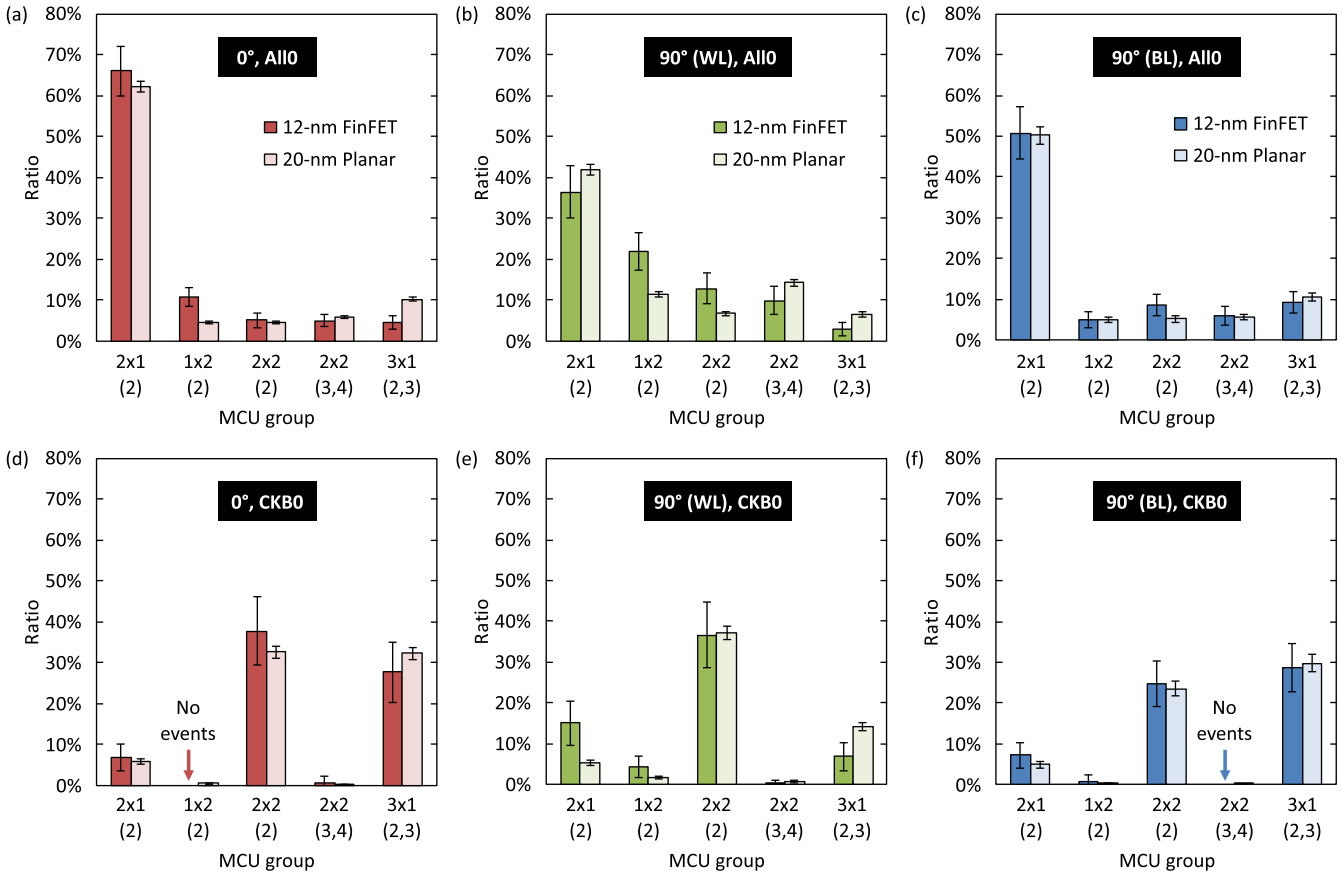

Fig. 10. Ratios for MCU groups shown in Fig. 9. Incidence angles of (a) 0°, (b) 90° (WL), and (c) 90° (BL) in the case of the All0 pattern. Incidence angles of (d) 0°, (e) 90° (WL), and (f) 90° (BL) in the case of the CKB0 pattern. Dark and light colored bars are for 12-nm FinFET and 20-nm planar SRAMs. All ratios are the values averaged over all VDD conditions. 100% corresponds to the total MCU events. Error bars represent one standard error.

mirror images of each pattern are included in the same group. The ratios of these MCU groups are presented in Fig. 10, where the left, middle, and right graphs are for the angles of 0°, 90° (WL), and 90° (BL), respectively. Fig. 10(a)–(c) are for the case of the All0 pattern, and Fig. 10(d)–(f) are for the case of the CKB0 pattern. It is observed that the probability distribution of the MCU groups strongly depends on the data patterns in each angle of incidence.

This is due to the difference in the spatial arrangement of node voltages of SRAM cells. In SRAM circuits, nMOS transistors of high nodes are generally vulnerable to charge collections. In the case of the All0 pattern, the relative location of the nearest neighbor high nodes corresponds to the $2 \times 1(2)$ group [see Fig. 3(a)]. In the case of the CKB0 pattern, this corresponds to the $2 \times 2(2)$ group [see Fig. 3(b)]. This different arrangement is clearly demonstrated in Fig. 10, where the occurrence ratios of the $2 \times 1(2)$ and $2 \times 2(2)$ groups are relatively high for the All0 and CKB0 patterns, respectively.

It should be noted that pMOS transistors of low nodes are also sensitive to charge collections. However, our results did not show the contribution of the pMOS transistors to the MCU characteristics. For example, if the pMOS transistors are dominant in determining the MCU pattern, the ratio of the $2 \times 1(2)$ group is expected to be similar between the All0 and CKB0 patterns because the relative position of two sensitive pMOS transistors in two adjacent SRAM cells along a BL is similar between the two patterns (see Fig. 3). Contrary to this, the significant difference in the ratio of the $2 \times 1(2)$ group is found between the two patterns. Therefore, the dominant contributor to the MCU characteristics is indicated to be the nMOS transistors of high nodes in both the 12-nm FinFET and 20-nm planar SRAMs.

As previously investigated in [16], due to the forward emission of secondary ions, the spatial distribution of fail bits varies depending on the direction of neutron incidence. In particular, the spatial range of fail bit patterns becomes longer in the direction of neutron incidence. The variations among the incidence angles observed in Fig. 10 are consistent with this understanding. For example, the ratios of the $1 \times 2(2)$ and $3 \times 1(2, 3)$ groups are relatively high at the angles of 90° (WL) and 90° (BL), respectively.

The important observation in this pattern analysis is that, as a whole, the probability distribution of these fail bit patterns is similar between the 12-nm FinFET and 20-nm planar SRAMs. This indicates that the physical arrangement of node voltages and the forward emission of secondary ions are the significant factors determining the MCU characteristics and their angular sensitivity in the 12-nm FinFET SRAMs, as well as in the 20-nm planar SRAMs.

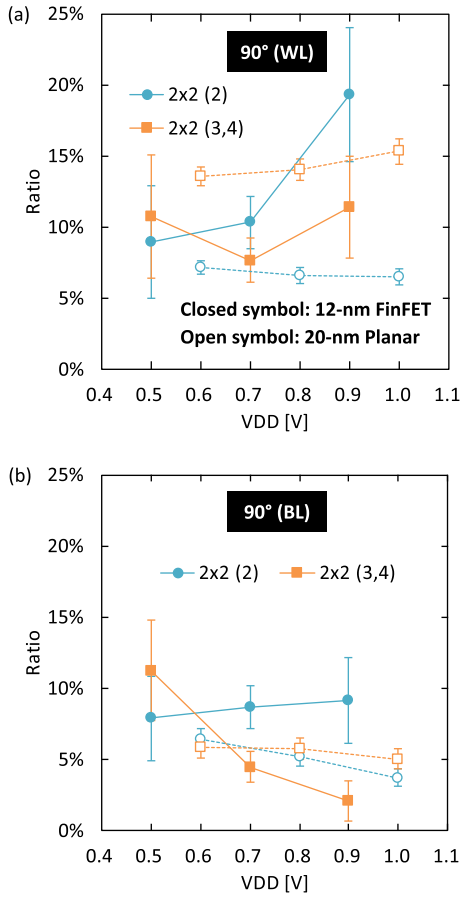

Fig. 11. Ratios of MCU events with 2×2 fail bit patterns as a function of VDD in the case of the All0 pattern. Ratios for the angles of (a) 90° (WL) and (b) 90° (BL). Cyan and orange plots correspond to the groups of $2 \times 2(2)$ and $2 \times 2(3, 4)$, respectively. 100% corresponds to the total MCU events. Filled and open symbols are for 12-nm FinFET and 20-nm planar SRAMs, respectively. Error bars represent one standard error.

D. Voltage Dependencies of Pattern-Wise MCU Ratios

For investigating the contribution of PBEs further, this section looks into the voltage dependence of probability of each fail bit pattern. As mentioned earlier, PBEs affect both the voltage dependence of MCU ratio and the fail bit patterns of MCU events. The contribution of PBEs could be different for different patterns, which may lead to the difference in the voltage dependence among the patterns.

As explained in Fig. 3, the All0 and CKB0 patterns were used in our experiments. The important point is that the difference in the physical arrangement of node voltages leads to the different sensitivity to PBEs. Considering that a potential perturbation in a p-well can activate PBEs in multiple nMOS transistors in the p-well and that high nodes are vulnerable to charge collections, the influence of PBEs on MCUs is more significant for the All0 pattern than for the CKB0 pattern. This is because, in the case of the All0 pattern, high nodes are densely packed in a p-well [see Fig. 3(a)]. Therefore, the MCU events for the case of the All0 pattern were analyzed.

From the fail bit patterns extracted in Section III-C (Fig. 9), this analysis focused on the MCU events with the range of 2×2 bits for the All0 pattern. There are two groups of the patterns of 2×2, as seen in Fig. 9. One is a group of the patterns having two fail bits, which is named as $2 \times 2(2)$. Another group includes the patterns having three or four fail bits, which is named as $2 \times 2(3, 4)$. The key point is that, in contrast to MCU events induced by direct charge collections along particle tracks, PBEs can provoke MCU events with L-shaped and block-like patterns of fail bits because a potential perturbation in a p-well can activate PBEs in multiple nMOS transistors simultaneously [16]. Therefore, in the MCU groups of $2 \times 2(2)$ and $2 \times 2(3, 4)$, it can be supposed that the contribution of PBEs is larger for the $2 \times 2(3, 4)$ group than for the $2 \times 2(2)$ group. With the above considerations, the voltage dependencies of the occurrence ratios of these two groups were analyzed.

Fig. 11 shows the ratios of the $2 \times 2(2)$ and $2 \times 2(3, 4)$ groups as a function of VDD. Fig. 11(a) and (b) are for the incidence angles of 90° (WL) and 90° (BL), respectively. As for the 20-nm planar SRAMs, the voltage dependencies for the two groups are very similar in both angles of incidence. Regarding the 12-nm FinFET SRAMs, on the other hand, the large discrepancy is found between the two groups in the angle of 90° (BL). As can be seen in Fig. 11(b), the ratio of the $2 \times 2(3, 4)$ group obviously decreases with increasing voltage in the 12-nm FinFET SRAMs. In contrast, the ratio of the $2 \times 2(2)$ group is almost independent on the voltage. In the case of the angle of 90° (WL), shown in Fig. 11(a), the difference between the ratios of the two groups is not significant and there is no decreasing trend with respect to the voltage. As discussed in Section III-B, the large contribution of PBEs results in the positive increase in the slope of the voltage dependence of MCU ratio. Therefore, it is expected that the $2 \times 2(3, 4)$ group has a more positive value of the slope compared to the group of $2 \times 2(2)$. However, in the 12-nm FinFET SRAMs, this ratio for the $2 \times 2(3, 4)$ group apparently decreases with the voltage at the angle of 90° (BL), i.e., the negative value of the slope. This result naturally leads to the view that, in the 12-nm FinFET SRAMs, the contribution of PBEs is smaller for the angle of 90° (BL) than for the angle of 90° (WL).

The above analysis is consistent with the discussion in Section III-B and reinforces the suggestion that, in the 12-nm FinFET SRAMs, the difference in the MCU response between the angles of 90° (WL) and 90° (BL) stems from the different contribution of PBEs, which makes the angular sensitivity different from the 20-nm planar SRAMs. Further investigations are needed to identify the physical processes responsible for this situation. Nevertheless, based on our experimental results, it is highly probable that PBEs are one of the key factors for the angular sensitivity in the 12-nm FinFET SRAMs.

IV. Conclusion

We have experimentally investigated the angular sensitivities of the neutron-induced SEUs in the 12-nm FinFET SRAMs. The SEU, MCU, and MBU rates have been evaluated with three angles of neutron incidence. The angular responses of these rates have been compared between the 12-nm FinFET and 20-nm planar SRAMs in terms of the voltage dependence and the MCU pattern. Through the comparison of the MCU characteristics, the difference in the contribution of PBEs has

been discussed between the two SRAMs and also between the incidence angles for the 12-nm FinFET SRAMs.

It has been demonstrated that, although the number of incident neutrons decreases at grazing angle, the MBU rate increases when the incidence direction is parallel to the WLs, as previously observed in the 20-nm planar SRAMs. This result suggests that, in the case where the SRAM devices are mounted with the WLs vertical to the ground, the efficiency of ECCs can be reduced because the most part of terrestrial neutrons are vertically downward. It has been revealed that the angular response of MCUs is different between the 12-nm FinFET and 20-nm planar SRAMs: the voltage dependence of MCU ratio for the 12-nm FinFET SRAMs is considerably dependent on the incidence angle, whereas it is not for the 20-nm planar SRAMs. Considering the influence of PBEs on the MCU characteristics, we have attributed the different angular response of MCUs to the different contribution of PBEs. At the same time, it has been indicated that, in the 12-nm FinFET SRAMs, the contribution of PBEs becomes relatively large when the incidence angle is parallel to the WLs.

Based on our results, it is reasonable to conclude that the angular sensitivity of neutron-induced SEUs is different between the 12-nm FinFET and 20-nm planar SRAMs and that this difference is due to the change in the transistor structure, which leads to the different impact of PBEs. In addition, we suggest that, as demonstrated in this study, the analysis of the voltage dependence of pattern-wise MCU ratios is a fruitful approach to explore the underlying mechanism. This approach may be useful also for proton and heavy-ion experiments.

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