# Impact of Hydrided and Non-Hydrided Materials Near Transistors on Neutron-Induced Single Event Upsets

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*Abstract*—**The impacts of hydrided and non-hydrided materials near transistors on neutron-induced single event upsets (SEUs) were investigated by simulating monoenergetic neutron irradiations on 65-nm technology bulk static random access memories. The onset energy of the SEUs induced by H ions depends on the shielding capability, i.e., the material and thickness, of components placed in front of transistors when those components do not contain hydrogen atoms. The shielding capability also influences the initial slope observed in the energy-dependence of SEU cross sections. Taking into account the non-hydrided component attached to memory cells used in the simulation, all experimental data measured at each neutron facility were reproduced well using SEU cross sections obtained by simulation. We also find that the effect of components near transistors on neutron-induced soft error rates is not negligible even for irradiation by white neutrons.**

*Index Terms*-- **Single event upset, Soft error, Neutron, J-PARC, PHITS.**

## I. Introduction

Neutrons give rise to temporal malfunctions called soft errors for microelectronic devices. Specifically, a single neutron can generate secondary charged particles (e.g., protons, alpha particles, heavy ions, etc.) via nuclear reactions with constituent materials. Secondary charged particles discharge electron–hole pairs in memory elements. Some of the charges collected to nodes holding the memory information are accidentally recognized as signal. As a result, stored bit data are upset. This phenomenon is caused by one neutron, and thus it is called a single event upset (SEU). SEUs caused by secondary cosmic-ray neutrons have been recognized as a serious reliability problem for microelectronic devices at ground level.

Validation of soft error rates (SERs) is necessary to ensure the reliability of devices. Field tests [1] require a huge number of devices and a very long measurement time but provide the most realistic SERs. Acceleration tests at neutron facilities [2]-[5] provide SERs more quickly than field tests. For acceleration tests, some corrections are required to derive realistic SERs in the actual environment or to compare them with other measured data. Therefore, the extent to which various conditions affect the measurements should be determined.

Recently, we conducted neutron irradiation tests on modern complementary metal-oxide semiconductor (CMOS) static random access memory (SRAM) test chips [6]-[10] using various beam types: a white neutron beam at the Research Center of Nuclear Physics (RCNP) at Osaka University [4], quasi-monoenergetic neutron beams at the Cyclotron and Radioisotope Center (CYRIC) at Tohoku University [11], and a spallation neutron source at beamline no. 10 (BL10) of the Material and Life Science Experimental Facility (MLF) at the Japan Proton Accelerator Research Complex (J-PARC) [12], [13]. In those experiments, we investigated the impact of irradiation side on SEUs by measurement and simulation [9], [10]. We found that the SEU rate obtained by package-side irradiation is higher than that obtained by board-side irradiation. Other researchers have reported a similar tendency for other devices [14]. We also found that the placement of hydrides in front of the memory chip considerably increased SEU cross sections because H ions generated via neutron elastic scattering from hydrogen atoms were mostly emitted in a forward direction.

In general, components such as passivation, wafer coating, and buffer coating adjoin memory cells depending on the operating environment, the cost, and so on. These components also have various compositions. When the component does not contain hydrogen atoms, it plays the role of shielding rather than that of a H ion source. Therefore, SEU cross sections for low-energy neutrons might be reduced by non-hydrided components situated physically near transistors.

In this study, we derived SEU cross sections for 65-nm bulk SRAMs by Monte Carlo simulation, for various test board structures. We also analyzed our previous experimental data measured at CYRIC and J-PARC BL10 [8]-[10].

## II. Simulation Method

For the Monte Carlo simulation, Particle and Heavy Ion Transport code System (PHITS) ver. 3.08 [15] was applied to simulate radiation transports and nuclear reactions. Neutron reactions below 20 MeV were calculated using event generator mode (e-mode) ver. 2 [16], [17] with Japanese Evaluated Nuclear Data Library (JENDL) 4.0 [18], while those above 20 MeV were calculated by intra-nuclear cascade of Liege (INCL) model [19] and generalized evaporation model (GEM) [20]. The collected charge was estimated from the energy deposition using the multiple sensitive volume (MSV) model [21]. The collected charge, $Q_{coll}$, is approximated by

$$Q_{coll} = \frac{e}{E_{pair}} \sum \alpha_i E_{dep,i} , \qquad (1)$$

where $\alpha_i$ is the charge collection efficiency of the $i$th sensitive volume (SV), $E_{dep,i}$ is the energy deposited in the $i$th SV, $e$ is the elementary charge, and $E_{pair}$ is the average energy required to generate an electron–hole pair (3.6 eV in silicon). To define the size and the charge collection efficiency for each SV, the charge collection process in a 65-nm bulk n-channel metal-oxide field-effect transistor (NMOSFET) has been investigated systematically by 3-D technology computer-aided design (TCAD) simulator Hyper Environment for Exploration of Semiconductor Simulation (HyENEXSS) [22]-[24]. In this study, the same parameter set was adopted for the MSV model as in the previous study [9].

Fig. 1 shows the configuration of the test board, the memory chip, and the analysis volume used in the simulation. The chip was placed on a 10 mm × 10 mm × 1.6 mm board consisting of epoxy ($C_{15}H_{16}O_2$), pre-preg ($C_{16}H_{16}O_2$), and silica ($SiO_2$) layers. The chip was covered with a package containing bisphenol A epoxy resin ($C_{22.9}H_{26.1}O_{4.3}$), hardener ($C_9H_{10}O_3$), and silica. In the chip, 12 Mbit SRAM cells were placed as a two-dimensional grid. A 0.35-μm-thick insulation layer was placed on top of the SRAM cells, and a 2.43-μm-thick metal layer was placed on top of the insulation layer. We assumed that a 40-μm-thick additional layer made of silicon dioxide would be on top of the metal layer. Simulations with and without the additional layer were performed to investigate the impact of components not containing hydrogen. The analysis volume was divided into two regions, A and B. Region A was defined by the active area of the NMOSFET and an effective funneling length of 0.5 μm, while region B was defined as the remainder of the NMOSFET. The collected charge was estimated when a charged particle struck region A because that region was expected to collect charges due to funneling and be responsible primarily for SEUs.

Monoenergetic neutron irradiations of the test target were simulated, and the number of events, $N(E_n,q)dq$, with the collected charge in [$q$, $q+dq$] at the incident neutron energy, $E_n$, was obtained. The SEU cross section was calculated as a function of the critical charge, $Q_{fit}$, as follows:
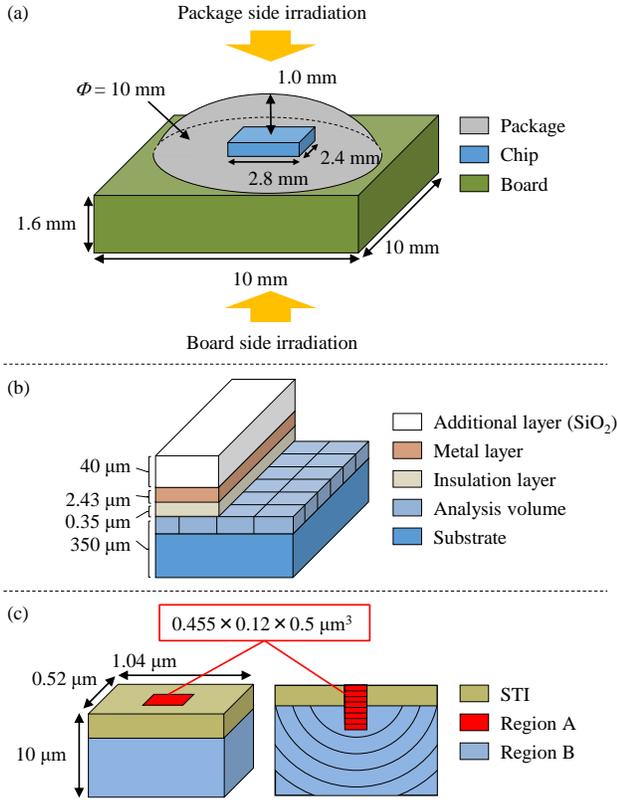
Figure 1. Simulation structures of (a) test board, (b) memory chip, and (c) analysis volume.



Figure 2. Neutron energy spectra for each neutron facility and terrestrial cosmic-ray neutrons calculated by PARMA.
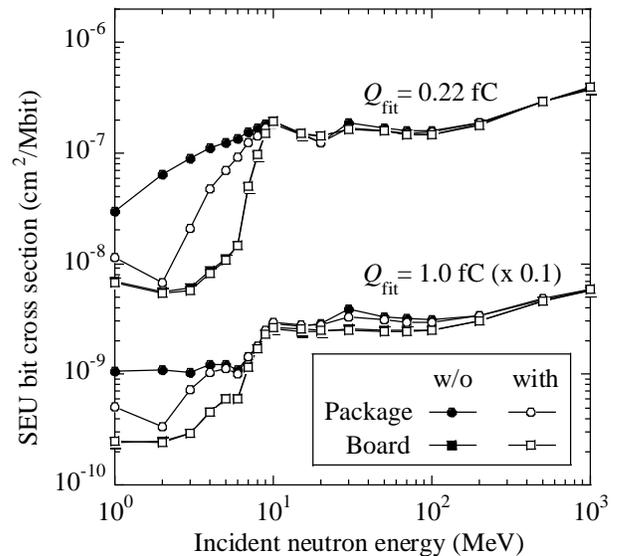


Figure 3. Monoenergetic neutron-induced SEU bit cross sections under each condition at $Q_{fit}$ = 0.22 fC and 1.0 fC calculated by PHITS+MSV model. The error bar for each point is too small to be visible.

$$\sigma_{SEU}(E_n, Q_{fit}) = \frac{A}{N_{in}N_{bit}} \int N(E_n, q)dq, \qquad (2)$$

where $A$ is the surface area of the test board shown in Fig. 1, i.e., $A$ = 1.0 cm$^2$; $N_{in}$ is the number of incident neutrons in the PHITS calculation; and $N_{bit}$ is the number of SRAM cells placed in the memory chip. Note that the critical charge is treated as a fitting parameter to reproduce measured data well, because the actual threshold charge for an upset is unclear. In this paper, we show the results for $Q_{fit}$ = 0.22 fC and 1.0 fC to investigate how the variation of critical charge affects the SEU cross section.

To compare the simulation result with the data measured at each neutron irradiation facility, the number of SEUs, $N_{SEU}$, was calculated as

$$N_{SEU} = t \int \phi(E_n)\sigma_{SEU}(E_n, Q_{fit})dE_n, \qquad (3)$$

where $t$ is the neutron irradiation time and $\phi(E_n)$ is the neutron flux at each neutron facility shown in Fig. 2. Note that a 1 cm B$_4$C filter was installed in the beamline of J-PARC BL10 during the experiment in order to shield the thermal neutrons.

## III. RESULTS AND DISCUSSION

Fig. 3 shows the SEU bit cross sections calculated by PHITS+MSV model for package-side irradiation and board-side irradiation with and without the additional layer. Note

that the error bar for each point is too small to be visible. In the case of $Q_{fit}$ = 0.22 fC, the SEU cross sections for neutron energies above 10 MeV were almost invariant for both package-side and board-side irradiation, whereas below 10 MeV the SEU cross sections varied for package-side irradiation. In the case of $Q_{fit}$ = 1.0 fC, the trend was the same as for $Q_{fit}$ = 0.22 fC except for the energy level at which the difference in SEU cross sections appeared. For board-side irradiation, the SEU cross sections with and without the additional layer were much the same regardless of the critical charge.

Figs. 4 and 5 show the contributions of H ions, He ions, and other ions to the SEU cross section under each condition.
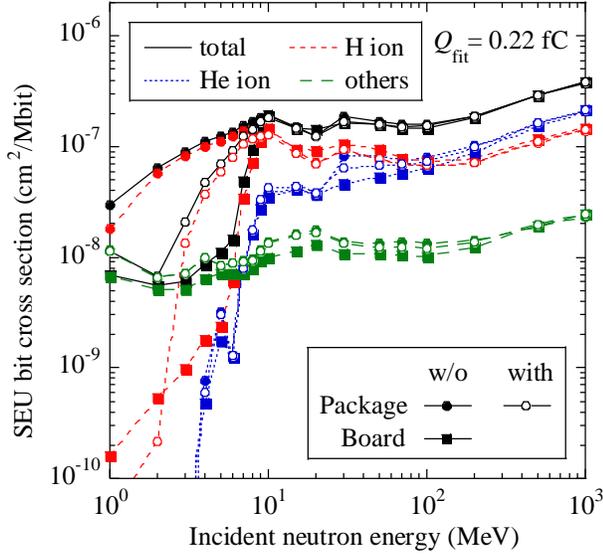
Figure 4. Contribution of H ions, He ions, and other ions for monoenergetic neutron-induced SEU bit cross sections under each condition at $Q_{fit}$ = 0.22 fC.
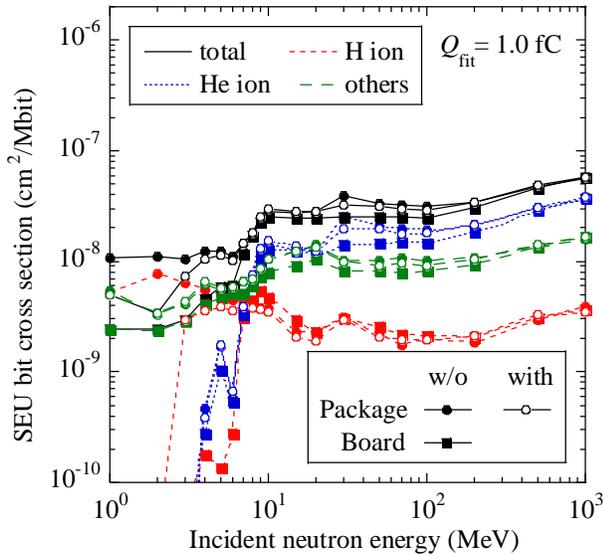


Figure 5. Contribution of H ions, He ions, and other ions for monoenergetic neutron-induced SEU bit cross sections under each condition at $Q_{fit}$ = 1.0 fC.



Figure 6. Ratio of the number of SEUs obtained in the simulation to that obtained in the experiment under each condition without additional layer.
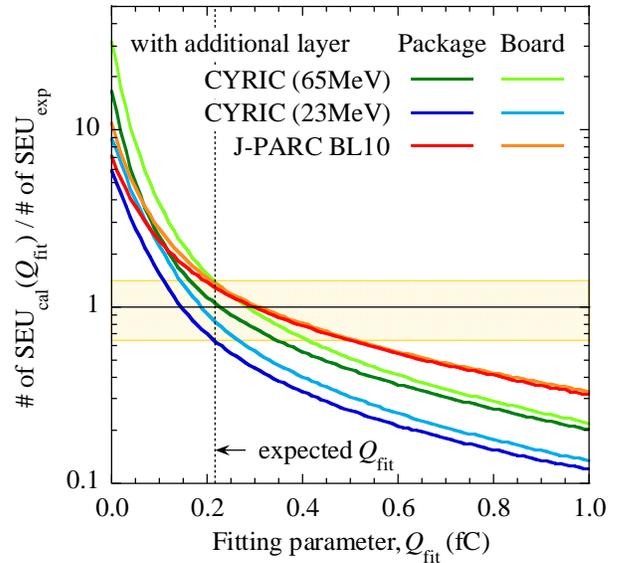


Figure 7. Ratio of the number of SEUs obtained in the simulation to that obtained in the experiment under each condition with additional layer.

Clearly, the difference in SEU cross sections is due to the difference in the contributions of H ions. Naturally, H ions cannot induce SEUs if they do not reach the SV. Therefore, the onset of the SEUs induced by H ions depends on shielding capability, i.e., the material and the thickness, of components placed in front of the transistors. Note that the maximum energy of the H ion generated via neutron elastic scattering from hydrogen atoms is almost the same as the incident neutron energy. The stack of metal and insulation layers placed in front of the analysis volume shielded H ions of energies below 0.45 MeV. When the additional layer was attached, the stack of them shielded H ions of energies below 2.2 MeV. In the case of board-side irradiation, the 300-μm-thick substrate shielded H ions of energies below 6 MeV. These energies correspond to the onset energy of the SEU cross section under each condition. The SEU cross section with a higher onset has a steeper slope around neutron energies of several MeV. This is because the distance range of a several-MeV H ion increases drastically when its kinetic energy increases. In the case of $Q_{fit}$ = 0.22 fC, the effect of the components near the transistors clearly appeared in the neutron-induced SEU cross sections for energies below 10 MeV, since the secondary H ions were the major cause of SEUs. On the other hand, in the case of $Q_{fit}$ = 1.0 fC, the effect of the components near the transistors appeared only below 3 MeV, since the contribution of H ions was smaller.
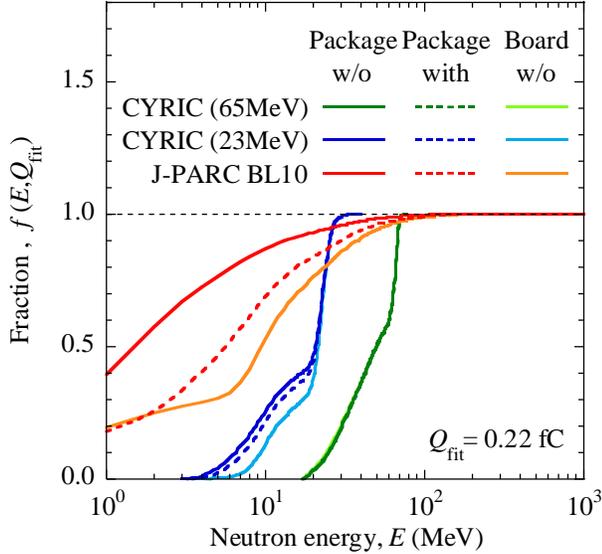
Figure 8. Fractions of the number of SEUs under each condition plotted as a function of neutron energy.

Table I. SERs estiamted from energy spectrum of white neutrons [25] and SEU bit cross sections obtained by package-side irradiation with and without additional layer.

| SER (FIT/Mbit) | w/o additional layer | with additional layer |
|---|---|---|
| $Q_{fit} = 0.22$ (fC) | 1537.3 | 1320.1 |
| $Q_{fit} = 1.0$ (fC) | 270.1 | 245.8 |

Figs. 6 and 7 show the ratio of the number of SEUs obtained in the simulation to that obtained in the measurement of package-side irradiation and board-side irradiation with and without the additional layer. The simulation without the additional layer reproduced the measured data within about 30 % at $Q_{fit} = 0.22$ fC except for the overestimation of the data obtained for package-side irradiation at J-PARC BL10. On the other hand, the simulation with the additional layer reproduced all measured data within about 30 % at $Q_{fit} = 0.22$ fC. This result indicates some non-hydrided components attached to the memory cells in the actual test board.

To address the contribution of low-energy neutrons to the total SEU count, Fig. 8 shows the fraction of SEUs under each condition plotted as a function of neutron energy, as calculated by the following equation:

$$f(E, Q_{fit}) = \frac{\int_0^E \phi(E_n)\sigma_{SEU}(E_n, Q_{fit})dE_n}{\int_0^\infty \phi(E_n)\sigma_{SEU}(E_n, Q_{fit})dE_n} . \quad (4)$$

Because low-energy neutrons abound in the spallation neutron source at J-PARC BL10, more than half of SEUs were caused by neutrons of energies below 10 MeV. Therefore, the existence of an additional layer had a strong influence on the number of SEUs. On the other hand, most of the neutrons in the quasi-monoenergetic neutron beams at CYRIC had the peak energy. Therefore, at CYRIC the number of SEUs obtained in the simulation with the additional layer was much the same as that without the additional layer.

We also calculated the SERs obtained by irradiation of white neutrons to investigate the effect of the additional layer. The energy spectrum of white neutrons is calculated by PHITS-based Analytical Radiation Model in the Atmosphere (PARMA) 4.0 [25], plotted in Fig. 2. Table I shows the SERs obtained by package-side irradiation. SERs on the ground decreased to about 85 % when considering the additional layer. Therefore, information about the components near the transistors is necessary in the accurate estimation of SERs.

## IV. CONCLUSIONS

The impact of components near transistors on neutron-induced SEUs was investigated. It was found that the onset energy of the SEU cross section depended on the shielding capability of components placed in front of the transistors when those components did not contain hydrogen atoms. The slope of the SEU cross section became steeper according to the increased onset energy of the SEU cross section. This behavior is due to the drastic increase in the distance range of several-MeV H ions with increasing kinetic energy. The simulation-vs.-experiment comparison of the number of SEUs suggests that the test board used in the measurements contained some non-hydrided components attached to the memory cell. The simulation with an additional layer could reproduce all measured data within about 30 % at $Q_{fit} = 0.22$ fC. In addition, the effect of the additional layer on SERs is not negligible even for the irradiation of white neutrons.

## REFERENCES

[1] "Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices," JEDEC Standard JESD89A, Oct. 2006 [Online]. Available: http://www.jedec.org

[2] S. A. Wender, S. Balestrini, A. Brown, R. C. Haight, C. M. Laymon, T. M. Lee, P. W. Lisowski, W. McCorkle, R. O. Nelson, and W. Parker, "A fission ionization detector for neutron flux measurements at a spallation source," *Nucl. Instr. Meth. Phys. Res. A*, vol. 336, pp. 226-231, Nov. 1993.

[3] E. W. Blackmore, P. E. Dodd, and M. R. Shaneyfelt, "Improved Capabilities for Proton and Neutron Irradiations at TRIUMF," in *Proc. of 2003 IEEE Radiation Effects Data Workshop (REDW), Monterey, CA, July 21- 25, 2003*, pp. 149-155, Jul. 2003.

[4] Y. Iwamoto, M. Fukuda, Y. Sakamoto, A. Tamii, K. Hatanaka, K. Takahisa, K. Nagayama, H. Asai, K. Sugimoto and I. Nashiyama "Evaluation of the White Neutron Beam Spectrum for Single-Event Effects Testing at the RCNP Cyclotron Facility," *Nucl. Technolo.*, vol. 173, pp. 210-217, Feb. 2011.

[5] A. V. Prokofiev, J. Blomgren, M. Majerle, R. Nolte, S. Rottger, S. P. Platt, C. X. Xiao, and A. N. Smirnov, "Characterization of the ANITA Neutron Source for Accelerated SEE Testing at The Svedberg Laboratory," in *Proc. 2009 IEEE Radiation Effects Data Workshop (REDW), Quebec, Canada, July 20-24, 2009*, pp. 166-173, Jul. 2009.

[6] S. Hirokawa, R. Harada, K. Sakuta, Y. Watanabe and M. Hashimoto, "Multiple Sensitive Volume Based Soft Error Rate Estimation with Machine Learning," in *Proc. 17th Eur. Conf. Radiation and its Effects on Components and Systems (RADECS), Bremen, Germany, Sep. 19-23, 2016*, H17, Sep. 2016.

[7] S. Hirokawa, R. Harada, M. Hashimoto and T. Onoye, "Characterizing Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4-V SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 62, pp.420-427, Apr. 2015.

[8] W. Liao M. Hashimoto, S. Manabe, S. Abe and Y. Watanabe, "Similarity analysis on neutron- and negative muon-induced MCUs in 65-nm bulk SRAM," *IEEE Trans. Nucl. Sci.*, vol. 66, pp.1390-1397, Jul. 2019.

[9] S. Abe, W. Liao, S. Manabe, T. Sato, M. Hashimoto, and Y. Watanabe, "Impact of Irradiation Side on Neutron-induced Single Event Upsets in

65-nm Bulk SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 66, pp. 1374-1380, Jul. 2019.

[10] J. Kuroda, S. Manabe, Y. Watanabe, K. Ito, W. Liao, M. Hashimoto, S. Abe, M. Harada, K. Oikawa, and Y. Miyake, "Measurement of Single-Event Upsets in 65-nm Bulk SRAMs Under Irradiation of Spallation Neutrons at J-PARC MLF," in *Proc. Eur. Conf. Radiat. Effects Compon. Syst. (RADECS), Montpellier, France, Sep. 16-20, 2019*, PC-13L, Sep. 2019.

[11] Y. Sakemi, M. Itoh and T. Wakui, "High Intensity Fast Neutron Beam Facility at CYRIC," International Atomic Energy Agency (IAEA), Vienna, Austria, IAEA-TECDOC-1743, pp. 229-233, Jul. 2014.

[12] F. Maekawa, K. Oikawa, M. Harada, T. Kai, S. Meigo, Y. Kasugai, M. Ooi, K. Sakai, M. Teshigawara, S. Hasegawa, Y. Ikeda and N. Watanabe, "NOBORU: J-PARC BL10 for facility diagnostics and its possible extension to innovative instruments," *Nucl. Instr. Meth. Phys. Res. A*, vol. 600, pp. 335-337, Feb. 2009.

[13] M. Harada, F. Maekawa, K. Oikawa, S. Meigo, H. Takada and M. Futakawa, "Application and Validation of Particle Transport Code PHITS in Design of J-PARC 1 MW Spallation Neutron Source," *Prog. Nucl. Sci. Tecnol.*, vol. 2, pp.872-878, Oct. 2011.

[14] T. Uemura, T. Kato, S. Okano, H. Matsuyama, and M. Hashimoto, "Impact of Package on Neutron Induced Single Event Upset in 20 nm SRAM," in *Proc. Int. Symp. Rel. Phys (IRPS), Monterey, CA, Apr. 19-23, 2015*, SE.9.1., Apr. 2015.

[15] T. Sato, Y. Iwamoto, S. Hashimoto, T. Ogawa, T. Furuta, S. Abe, T. Kai, P. Tsai, N. Matsuda, H. Iwase, N. Shigyo, L. Sihver, and K. Niita, "Features of Particle and Heavy Ion Transport code System (PHITS) version 3.02," *J. Nucl. Sci. Technol.*, vol. 55, pp. 684-690, Jan. 2018.

[16] T. Ogawa, T. Sato, S. Hashimoto and K. Niita, "Development of a reaction ejectile sampling algorithm to recover kinematic correlations from inclusive cross-section data in Monte-Carlo particle transport simulations," *Nucl. Instr. Meth. Phys. Res. A*, vol. 763, pp. 575-590, Nov. 2014.

[17] T. Ogawa, T. Sato, S. Hashimoto and K. Niita, "New algorithm for Monte Carlo particle-transport simulation to recover event-by-event kinematic correlations of reactions emitting charged particles," in *Proc. of Joint Int. Conf. on Math. and Comput., Supercomput. in Nucl. Appl. and the Monte Carlo Method (M&C+SNA+MC), Nashville, TN, Apr. 19-23, 2015*, pp.1-11, Apr. 2015.

[18] K. Shibata, O. Iwamoto, T. Nakagawa, N. Iwamoto, A. Ichihara, S. Kunieda, S. Chiba, K. Furutaka, N. Otuka, T. Ohsawa, T. Murata, H. Matsunobu, A. Zukeran, S. Kamada and J. Katakura, "JENDL-4.0: A New Library for Nuclear Science and Engineering," *J. Nucl. Sci. Technol.*, vol. 48, pp. 1-30, 2011.

[19] A. Boudard, J. Cugnon, J.-C. David, S. Leray and D. Mancusi, "New potentialities of the Liege intranuclear cascade model for reactions induced by nucleons and light charged particles," *Phys. Rev. C*, vol. 87, 014606, 2013.

[20] S. Furihata, "Statistical analysis of light fragment production from medium energy proton-induced reactions," *Nucl. Instr. Meth. Phys. Res. B*, vol. 171, pp. 251-258, Nov. 2000.

[21] S. Abe, and T. Sato, "Soft error rate analysis based on multiple sensitive volume model using PHITS," *J. Nucl. Sci. Technol.*, vol. 53, pp. 451-458, Mar. 2016.

[22] N. Kotani, "TCAD in Selete," in *Proc. of Int. Conf. Simulation of Semiconductor Processes and Devices (SISPAD), Leuven, Belgium, Sep. 2-4, 1998*, pp. 3-7, Sep. 1998.

[23] T. Wada, M. Fujinaga, Y. Okura, H. Ishikawa, S. Ito, T. Uchida, T. Enda, S. Otsuka, H. Komatsubara and T. Shinzawa, *Ext. Abstr. 53th Spring Meet. Japan Society of Applied Physics (JSAP), Mar. 22-26, 2006*, 22p-ZA-2, Mar. 2006 [in Japanese].

[24] M. Nakamura, *OYO BUTURI (Monthly Publication of The Japan Society of Applied Physics)*, vol. 77, pp.818-822, 2008 [in Japanese].

[25] T. Sato, "Analytical model for estimating terrestrial cosmic ray fluxes nearly anytime and anywhere in the world: Extension of PARMA/EXPACS," *PLoS ONE*, vol. 10, e0144679, Dec. 2015.