A Gate Delay Model Focusing on Current Fluctuation over Wide-Range of Process and Environmental Variability

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ABSTRACT
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Categories and Subject Descriptors
B.7.2 [Integrated Circuits]: Design Aids—Simulation

General Terms
Design, Experimentation, Performance

Keywords
gate delay model, variability, static timing analysis, statistical timing analysis

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able not only for variation-aware SSTA but also for DVS and variable $V_{th}$ design. In addition, the proposed model can be used to compute the sensitivity in the operating condition shifted from the nominal condition. (2) Additional time-consuming transient analysis for characterization is not required at all. The proposed current variation modeling needs only DC analysis, which is independent of input slope and output load, and hence the additional characterization cost is quite small. (3) We can compute gate delay in any conventional manners by using the replaced output load, and hence every timing analyzer can perform variation-aware timing analysis with the pre-process of output load translation. Delay is calculated by table look-up model, for example, as follows:

Prior preparation: (1) look-up table using input transition time and output load at nominal condition, (2) proposed current estimation model.

Input: (1) input transition time, (2) output load, (3) variational parameter values.

Step 1: Translate variability into current fluctuation by the proposed current estimation model, Step 2: Replace output load based on current fluctuation, Step 3: Calculate delay by look-up table with the replaced load.

The rest of the paper is organized as follows. Section 2 describes the key idea, that is translation of current variation into output load. Section 3 gives an implementation of the proposed idea for RC output load and slow input transitions. Section 4 shows experimental results to confirm the accuracy. We also demonstrate a comparison with the conventional sensitivity-based method. Finally, we conclude the paper in Section 5.

2. KEY IDEA OF PROPOSED MODEL

A feature of the proposed gate delay calculation is variational current modeling instead of direct delay modeling. Delay of a CMOS logic gate is the time required to charge/discharge its output load. Variability sources, such as gate length, change charging/discharging current, which results in gate delay variation. Therefore, variation-aware current estimation can guide gate delay computation for variability. We observe that charging/discharging current has an almost linear relation with respect to variation sources, and it is easier to model.

2.1 Relationship among delay, current and variability

We first review the relationship among gate delay, charging/discharging current and variability sources. Saturation current of MOSFET $I_{sat}$ is expressed as follows in alpha-power law MOSFET model [9].

$$I_{sat} = k\mu_{eff}W \frac{L}{L_{ox}} (V_{gs} - V_{th})^{\alpha},$$  \hspace{1cm} (2)

where $\mu$ denotes an effective mobility, $\mu_{eff}$ a dielectric constant of a gate oxide, $L_{ox}$ a gate oxide thickness, $W$ a channel width, and $L$ a channel length. $\alpha$ is a coefficient to denote carrier velocity saturation effect, and it becomes close to 1 in advanced technologies. $V_{th}$ is a threshold voltage, and $k$ is a coefficient. Equation (2) shows that the saturation current is roughly proportional to supply voltage, threshold voltage, channel width and mobility, and inversely proportional to gate length and gate thickness. An example of current variation in a 90nm CMOS technology is shown in Figure 2, where $dV_{th}$ is the variation of $V_{th}$ from the nominal value. $I_{step}$ ($I_d$ at $V_{ds} = V_{dd} = V_{th}$) has a linear relation with $V_{dd}$, $V_{th}$ and temperature $T$ and it is roughly inversely proportional to $L$. We therefore expect that current fluctuation can be modeled by a simple expression of

$$L^{-1}, V_{dd}, dV_{th}$ and $T$. Gate delay is basically inversely proportional to current [8]. Intuitively speaking from the above discussion, the gate delay is inversely proportional to $(V_{dd} - V_{th})$. This means that the sensitivity-based delay model for variability, which is widely adopted in SSTA, is not suitable for large variability of $V_{dd}$ and $V_{th}$, whereas it really works well for small amount of variation. In order to develop a gate delay model applicable to wide-range fluctuation of $V_{dd}$ and $V_{th}$, which is eagerly demanded in DVS and variable $V_{th}$ design, focusing and modeling current fluctuation is a reasonable approach.

2.2 Translation of current fluctuation into output load

We here show the key idea of the proposed model. We use a fall transition, as an example, of a 90nm single-stage inverter with 100fF output load when a step rise input transition is given (Figure 3). The fall gate delay depends on the drain current of NMOS $I_d$. The amount of charge to discharge, $Q$, is expressed as

$$Q = C V_{dd},$$  \hspace{1cm} (3)

where $V_{dd}$ is supply voltage and $C$ the total capacitance to discharge. $C$ includes $C_{load}$ and parasitic capacitance inside a cell. Generally speaking, when the drain current increases twice by process variation, the delay becomes half. When the output load becomes half, the delay also decreases to the half. The above discussion means that the variation of current can be translated into output load while keeping the gate delays equal. Considering that $Q$ varies with $V_{dd}$ fluctuation, we thus should translate $I_d$ variability into $C_{new}$ as follows,

$$I_d + \Delta I_d : I_d = Q : C_{new},$$  \hspace{1cm} (4)

$$= C(V_{dd} + \Delta V_{dd}) : C_{new} V_{dd},$$  \hspace{1cm} (5)

$$\Rightarrow \text{Delay}(I_d + \Delta I_d, Q) = \text{Delay}(I_d, Q_{new}),$$  \hspace{1cm} (6)

$$C_{new} = \frac{I_d}{I_d + \Delta I_d} \frac{V_{dd} + \Delta V_{dd}}{V_{dd}} C.$$  \hspace{1cm} (7)
where $\Delta$ denotes variability and superscript $new$ corresponds to values in the nominal condition. The rise delay is calculated similarly.

In order to realize the above translation, we need two techniques: (1) current estimation and (2) estimation of parasitic output capacitance. The second technique is also required in transistor-level timing analyzer, such as [10], and it is not novel. We therefore do not discuss capacitance estimation further in this paper. With regard to (1), the saturation current $I_{\text{sat}}$ is reasonable for Equation (7) when the input signal is a step signal, because the NMOS works like a constant current source in the saturation region. In practical designs, however, input signals have a certain amount of transition time. Current modeling for slow input transition will be discussed later in Section 3.

A paper proposes a gate delay model that translates difference of power/ground voltage level between driver and receiver into output load toward power/ground-noise-aware timing analysis [6]. Though the idea that delay variation is expressed by output load replacement is the same, the variability of this paper includes both manufacturing and environmental fluctuation, and the target is different.

### 2.3 An analysis example

We demonstrate an example to validate the idea of the proposed method in a 90nm CMOS technology. This example supposes that power supply voltage $V_{dd}$ fluctuates. The upper figure in Figure 4 shows delay variation estimated by circuit simulation with the actual varied $V_{dd}$ and with the proposed idea. The lower figure shows the delay estimation error of the proposed model. In this analysis, the estimation error is below 2% even though the supply voltage is varied from 0.7 to 1.3V by 0.6V, where the nominal supply voltage is 1.0V. The proposed idea works well for wide-range variation. Figure 5 shows a waveform example, where the difference of supply voltage is removed by normalization to 1.0V for waveform comparison. Gate delay is measured after the voltage normalization as well. We can see that the output transition waveform is well estimated. We also verify the effectiveness under variations of $L$, $V_{th}$ and $T$ in a similar way.

#### 3. COPING WITH RC OUTPUT LOAD AND SLOW INPUT TRANSITION

To implement the proposed idea in a timing analyzer, there are two obstacles in current modeling: (1) RC output load and (2) slow input transition. This section shows the solutions for each obstacle.

**3.1 Translation for RC output load**

Coping with RC output load is indispensable in nano-meter technology era, because wire resistance is large especially in inter-block interconnections. We here show that the proposed idea can be applied consistently to generic output load.

Figure 6 shows the concept for a generic output load, where $Y$ is the driving point admittance of the actual circuit, and $Y^{new}$ is that after translating variability into output load. Similar to capacitive output load, $Y^{new}$ is calculated by

$$Y^{new} = \frac{I_{d}}{I_{d} + \Delta I_{d}} \frac{V_{dd} + \Delta V_{dd}}{V_{dd}} Y.$$

We can see that Equation (7) is one of the special cases of Equation (8). In the case of CRC $\pi$ model in Figure 7, $C_{1}^{new}$, $C_{2}^{new}$ and $R^{new}$ can be simply expressed as follows:

$$C_{1}^{new} = \frac{I_{d}}{I_{d} + \Delta I_{d}} \frac{V_{dd} + \Delta V_{dd}}{V_{dd}} C_{1},$$

$$C_{2}^{new} = \frac{I_{d}}{I_{d} + \Delta I_{d}} \frac{V_{dd} + \Delta V_{dd}}{V_{dd}} C_{2},$$

$$R^{new} = \frac{I_{d} + \Delta I_{d}}{I_{d}} \frac{V_{dd} + \Delta V_{dd}}{V_{dd}} R.$$

**3.2 Current estimation for slow input transition**

We here discuss current estimation used to translate variability into output load in Equations (7) and (8). When a fast input transition is given, i.e. the output transition is much slower than the input transition, $I_{\text{step}}$ is used as $I_{d}$, as explained in Section 2.2. This section supposes a situation that the input transition is slower than the output transition in Figure 3. The operating condition of the NMOS depends on the input waveform and the output load, and hence it is difficult to identify the discharging current that should be used for the proposed translation. To solve this problem, we have observed discharging current in various conditions of input waveform and output load, and found that the discharging current becomes almost maximum when the output goes across 50% of the supply voltage. Also obviously, the discharging current starts to flow when the input voltage reaches to the threshold voltage of the NMOS.

Figure 8 shows a typical current waveform when a slow input transition is injected. The current shape can be approximated as a trapezoid as shown in Figure 8 and the integrated area of the current is equal to the area of a rectangle whose height is $I_{\text{avg}} = \frac{1}{2}(I_{V_{th}} + I_{V_{th}+0.5V_{dd}})$, where $I_{V_{th}}$ represents the drain current when the input voltage equals the threshold voltage, and $I_{V_{th}+0.5V_{dd}}$ is the drain current when the output voltage equals half of the supply voltage. Please recall that gate delay is the time required to charge/discharge the output load. The output voltage depends on the amount of charge that has been charged/discharged through the MOS. In other words, the integral average of the charging/discharging current determines the delay characteristics. This is why $I_{\text{avg}}$ is reasonable for slow input transition. We therefore decide to use $I_{\text{avg}}$ as $I_{d}$. Here, you may
think that $V_{in}=V_{th}$ is not necessary because of its small value, but we experimentally confirm that $I_{V_{in}=V_{th}}$ contributes to accurate delay estimation, especially in the case that $V_{dd}$ is close to $V_{th}$.

A requirement for current estimation is flexibility and robustness that can accept new variation parameters and multiple input cells. We, in this paper, use a response surface method as a candidate. However, other methods also can be used as long as their accuracy is sufficient. In the response surface method, we can choose the order of polynomials according to the required accuracy. We derive polynomial expressions for $I_{V_{in}=V_{th}}(L^{-1}, V_{dd}, dV_{th}, T, V_{th})$ and $I_{V_{in}=0.5V_{dd}}(L^{-1}, V_{dd}, dV_{th}, T, V_{th})$. $V_{th}$ is dependent on $L$, $V_{dd}$ and $T$ as well as $dV_{th}$, and hence $V_{th}$ in $I_{V_{in}=V_{th}}$ is separately estimated beforehand by the response surface method.

When deriving $I_{V_{in}=V_{th}}$, the output voltage is reasonably assumed to be $V_{dd}$, because at that timing the output is about to start a transition. A remaining problem is how to compute $V_{in}$ when the output is $0.5V_{dd}$. Note that the output waveform shape and/or the crossing timing of $0.5V_{dd}$ can be computed by the delay model in the nominal condition with the replaced output load. The input waveform is also given, and hence we can estimate $V_{in}$ when the output is $0.5V_{dd}$ without transient simulation. A chicken-and-egg problem of current and $V_{in}$ estimation exists, that is current estimation needs $V_{in}$, and $V_{in}$ estimation requires the output load computed based on current estimation. We experimentally confirm that $V_{in}$ can be estimated by iteratively updating the output load with the proposed translation, which will be shown in Section 4.2.1.

### 3.3 Problem of starting time of switching

The proposed method is expected to be applicable for large supply voltage and threshold voltage variation. This situation leads to a problem that at the time at which the output starts to change varies (Figure 9). "Proposed Output" is normalized to the actual $V_{dd}$. In this example, we stretch the waveform with respect to voltage from "Actual Input" to "Input at nominal", since the supply voltage drops.

### Table 1: Condition of the variability for Monte Carlo analysis.

<table>
<thead>
<tr>
<th>Variable parameter</th>
<th>Mean</th>
<th>$\sigma$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L$</td>
<td>100nm</td>
<td>20nm</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>1.0V</td>
<td>0.5V</td>
</tr>
<tr>
<td>$dV_{th}$</td>
<td>0V</td>
<td>0.3V</td>
</tr>
<tr>
<td>$T$</td>
<td>37.5 $^\circ$C</td>
<td>82.5 $^\circ$C</td>
</tr>
</tbody>
</table>

In this case, the timing when the input reaches to the threshold voltage gets earlier by $\Delta t$ due to voltage drop, which causes delay increase that is irrelevant to current variation. A similar problem also occurs when $V_{th}$ varies. Thus, the crossing timing offset ($\pm \Delta t$) of threshold voltage is separately computed and compensated in delay estimation (Figure 10). The input transition waveform is given in STA, and hence $\Delta t$ can be calculated without any special information or simulation.

### 4. EXPERIMENTAL RESULTS

This section demonstrates the accuracy of the proposed gate delay model and its efficiency in applicable variation range. We assume that $L$, $V_{dd}$, $dV_{th}$ and $T$ vary as Table 1, where $dV_{th}$ denotes a $V_{th}$ offset excluding the influence of the other parameters. $V_{dd}$ and $V_{th}$ are widely varied, because the proposed model also aims to cover DVS and variable $V_{th}$ design. Thus, there are combinations in which MOSFETs works only in sub-threshold region. The sub-threshold current changes in an exponential manner with respect to $V_{dd}$ and $V_{th}$, and hence the regression to polynomials is not appropriate. However, generally speaking, in those combinations, gate delay is unacceptably large. We therefore eliminate those combination of $V_{dd}$ and $V_{th}$ in experiments.

In the 90nm technology we use for experiments, the value of 2fF corresponds to an input capacitance of a standard inverter. The results of fall delay in an inverter are shown, and $L$, $V_{dd}$, $dV_{th}$ and $T$ vary simultaneously and independently as long as there are no special notations in the following experiments. In the following figures of waveform example, solid lines denote actual waveforms, and dotted lines correspond to the proposed model.

### 4.1 Comparison with conventional methods

In this section, we demonstrate advantages of the proposed model compared with conventional methods.

#### 4.1.1 Applicable range

We demonstrate the applicable variation range of the proposed method comparing with the sensitivity-based model. Figure 11 shows a comparison in delay estimation error when $dV_{th}$ is varied. The proposed method provides accurate estimation even though $dV_{th}$ varies by $\pm 0.35V$. When delay estimation within 10% error is demanded, $V_{dd}$ variation of $\pm 0.5V$ and $dV_{th}$ variation of $\pm 0.35V$ are
In Step 1-4, additional transient simulation is not necessary. $I_{\text{avg}}$ computed in the above procedure is compared with that calculated by using the exact value of $V_{\text{in}}$ obtained from transient analysis. In the results of Monte Carlo analysis, RMS error of $I_{\text{avg}}$ estimation is 7.6% for output load of 2fF, 4.0% for 10fF, and 0.2% for 100fF. Increasing the number of the iteration from Step 2 to Step 4 hardly improves the accuracy of $I_{\text{avg}}$ estimation. We conclude that $V_{\text{in}}$ can be computed in the above process with a reasonable accuracy.

4.2.2 Accuracy of delay estimation

We next evaluate the accuracy of delay estimation. We perform Monte Carlo analysis whose evaluation count is 3000. Figure 14 shows the accuracy of delay estimation when the input transition time is 100ps. The transition time of 100ps corresponds to the transition with fan-out 8. We can see that gate delay is well estimated even for slow input transition. RMS error is 2.9ps (14.0%) for output load of 2fF, 3.3ps (7.0%) for 10fF, and 3.7ps (1.5%) for 100fF. Figures 15 and 16 show the error histograms and CDFs (cumulative distribution functions) of the proposed method. When the input transition time is 300ps, RMS error is 11.2ps for 2fF and 8.9ps (13.2%) for 10F and 11.3ps (3.8%) for 100F. RMS error is 11.7ps (3.4%) for a combination of 500ps and 100F. In the situation that the input transition is slow and the output load is small, it is difficult to estimate delay in general, however, the proposed method estimates the delay with an acceptable accuracy.

Figure 17 shows an example of transition waveform in the case of $V_{\text{dd}}$ fluctuation. The waveform shape as well as the propagation delay is well estimated. In timing analysis, accurate estimation of output transition time is also required. RMS error is 1.7ps (5.3%) for output load of 2fF, and 6.1ps (1.4%) for 100F when the input transition time is 100ps. The proposed model gives accurate output transition time as well as delay time.

4.2.3 Gate delay distribution

We here demonstrate that the proposed gate delay model can reproduce a statistical distribution of gate delay. We perform Monte Carlo analysis and compare the actual distribution given by circuit simulation with that of the proposed method. Figure 18 shows the
delay histograms and CDFs. The distribution shapes by the proposed method agree with those by circuit simulation. The proposed method can be used for deriving gate delay distribution.

4.2.4 NAND, NOR

The proposed method is applicable for NAND and NOR as well as inverter. We perform a Monte Carlo analysis whose evaluation count is 500. $L$ and $dV_{th}$ are varied independently for every transistor. Figure 19 shows the delay estimation accuracy of a 2-input NAND gate. RMS error is 3.9ps (5.5%). In the case of 2-input NOR gate (Figure 20), RMS error is 4.9ps (9.1%). The proposed model can be applied for any single-stage CMOS gates.

4.3 Accuracy evaluation for RC output load

We next evaluate the accuracy when RC output load is given. We perform a Monte Carlo analysis whose evaluation count is 3,000. A 2.0mm-long wire is used as an RC output load. We translate the wire into a CRC $\pi$ model by [11]. Figure 21 shows the accuracy of the proposed method and a waveform example is Figure 22. RMS error is 11.6ps (1.2%). We can see that the proposed method works well for RC output load as well as capacitive load.

4.4 Application to multiple-stage path and flip-flop

4.4.1 Multiple-stage path

We also evaluate the accuracy when multiple-stage path is given (Figure 23). We assume that $L$ and $dV_{th}$ vary independently at each transistor. The capacitance of 100F is attached to each gate output. Figure 24 shows a waveform example. We can see that the proposed method works well for multiple-stage path.

4.4.2 Flip-flop

CLK-to-Q delay of a negative-edge trigger D flip-flop in Figure 25 is examined. The signal path to consider in delay estimation is extracted and shown in Figure 26. A transmission gate is modeled such that the sum of NMOS and PMOS current is expressed in

Figure 18: Delay distribution (input transition time 100ps, output load 100fF).

Figure 19: Delay estimation accuracy (NAND: A: LH (input transition time 100ps), B: High, output load 10fF).

Figure 20: Delay estimation accuracy (NOR: A: LH (input transition time 100ps), B: Low, output load 10fF).

Figure 21: Delay estimation accuracy for RC output load (2.0mm-long wire).

Figure 22: Waveform evaluation for RC output load ($L$ 80nm, $V_{dd}$ 0.7V, $dV_{th}$ 0.1V, $T$ 70°C, 2.0mm-long wire).

Figure 23: Example of multiple-stage path.

Figure 24: Waveform evaluation for multiple-stage path (solid lines denote actual waveforms, and dotted lines correspond to proposed model).

Figure 25: Negative-edge trigger DFF.
a second-order polynomial assuming that step inputs of CLKN and CLKP are given at the same time for simplicity.

We vary $L$ and $dV_{dd}$ independently at each transistor, and the same values of $V_{dd}$ and $T$ are given to all transistors. The transition time of given CLK signal is 100ps in this experiment. Figure 27 shows a waveform example. Labels CLK, CLKN, CLKP, A, B and Q correspond to the nodes in Figure 26. The waveforms by the proposed method are very close to the actual waveforms.

We next show the statistics of the estimation accuracy. We perform Monte Carlo analysis whose evaluation count is 1000. Figure 28 shows the accuracy of delay estimation when the output load is 10fF. RMS error is 6.7ps (6.9%). We can see that CLK-to-Q delay is well estimated.

### Delay estimation accuracy (DFF: clock transition time 100ps, output load 10fF).

We propose a method to compute variational gate delay by translating variability into output load. Every variation source is considered as a factor that fluctuates charging/discharging current. The proposed model provides accurate delay estimation in a wider range of manufacturing and environmental variability compared with sensitivity-based model, thanks to capturing variability in current modeling. Any additional characterization by time-consuming transient analysis is not necessary at all. Experimental results reveal that the RMS error of the proposed model is small even for slow input transition. The large applicable range of variability may eliminate delay characterization in numerous corners and provide a solution for timing verification in DVS and $V_{th}$ control design.

### 4.5 Application to sensitivity calculation

When the average of a variational parameter shifts, the sensitivity becomes different with the sensitivity at the nominal condition. The proposed model can give the sensitivity in Equation (1) easily even when the average changes. Let us show an example. In this experiment, we vary $V_{dd}$ such that the average and $3\sigma$ are 0.8V and 0.1V, respectively. The sensitivity to $V_{dd}$ at 1.0V is not accurate when nominal $V_{dd}$ is actually 0.8V. On the other hand, when we compute the sensitivity at 0.8V by using the proposed model, the estimation accuracy is much improved. Figure 29 shows the delay estimation accuracy. The proposed model can be used to compute the sensitivity at any point, which improves accuracy of SSTA that exploits the benefit of the sensitivity-based delay model (e.g. [2]).

### 5. CONCLUSION

We propose a method to compute variational gate delay by translating variability into output load. Every variation source is considered as a factor that fluctuates charging/discharging current. The proposed model provides accurate delay estimation in a wider range of manufacturing and environmental variability compared with sensitivity-based model, thanks to capturing variability in current modeling. Any additional characterization by time-consuming transient analysis is not necessary at all. Experimental results reveal that the RMS error of the proposed model is small even for slow input transition. The large applicable range of variability may eliminate delay characterization in numerous corners and provide a solution for timing verification in DVS and $V_{th}$ control design.

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### 7. REFERENCES


