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Characterizing SRAM and FF soft error rates with measurement and simulation

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ABSTRACT

Soft error originating from cosmic ray is a serious concern for reliability demanding applications, such as autonomous driving, supercomputer, and public transportation system. Also, as the number of electronic devices increases, consumer electronics may require higher reliability than ever. On the other hand, device miniaturization and lower voltage operation degrade the immunity of SRAM and flip-flops in VLSI, and then soft error countermeasures will be demanded in more and more products. This paper characterizes and discusses soft error rates of SRAM and flip-flops in the terrestrial environment. Measured soft error rates of bulk and FDSOI SRAMs are presented. Also, the multiplicity and mechanism of multiple cell upsets (MCUs), which can spoil error correction code (ECC), are discussed. Flip-flops are also sensitive to radiation, but its protection is not well established since ECC cannot be applied. This paper reviews redundant FFs that are developed aiming at higher radiation immunity and demonstrates the resilience improvement with irradiation test results. Also, the importance of layout design is pointed out with a comparative study. Simulation, on the other hand, is a key technology to understand the soft error mechanism and guide radiation aware design for higher reliability. This paper outlines a physics-based multi-scale Monte Carlo simulation framework tailored for soft error simulation. The simulation flow and the model construction are explained, and some important implications are derived from the simulation results that assume 65-nm to 25-nm SRAMs. Finally, this article touches on future trends regarding device structure and overlooked secondary cosmic rays. The advantage and unique features of FinFET recently reported in literature are introduced. Also, muon-induced soft error is discussed focusing on the difference between positive and negative muons.

1. Introduction

With the exponential rate of enhancement both in transistor performance and integration scale, VLSI (very large scale integration) systems have been driving advancement of information systems. The problem of soft errors occurring inside the VLSIs in terrestrial radiation environment has been recognized as a major threat for electronics at ground level [1]. Radiation-induced soft error is represented as a transient malfunction in VLSIs due to single event upset (SEU), which is caused by a transient signal induced by energetic ionizing radiation and destroy the information stored in memory elements.

People and society have been more and more dependent on the services provided by the information systems. For example, autonomous driving is intensively studied, and experiments with prototyped cars are carried out all over the world. The autonomous driving is an intelligible and highly probable near-future situation that we are entrusting our lives to VLSI-centric information systems. Another technology movement is Internet of Things (IoT), and a report predicts that more than 30 billion devices are connected to Internet in 2018 [2]. We are expecting IoT would enable more comfortable, more efficient, safer and securer society. Thus, these technology trends make it a social requirement to guarantee the reliability of the information systems and that of

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the VLSI systems accordingly.

Another strong demand for VLSI is low power operation for not only portable devices but also high-performance systems, such as supercomputers and cloud servers. Supply voltage scaling is a key to reduce the power dissipation in VLSI circuits. Especially, an aggressive voltage scaling down to near-threshold voltage can achieve a significant reduction in power dissipation [3]. Therefore, near-threshold circuits that operate at a supply voltage comparable to the threshold voltage are drawing a lot of attention. However, near-threshold circuits are sensitive to manufacturing variability and environmental fluctuation. This sensitivity has been a major concern, and many researchers have investigated ways to cope with it (e.g., Refs. [4–6]). However, little attention has been paid to the vulnerability of near-threshold computing to radiation particles.

For achieving lower-voltage operation, further device miniaturization, and manufacturing variability mitigation, new transistor structures are developed and put into production. Silicon on insulator (SOI) is one of the devices to mitigate the elevating power consumption of large-scale integration (LSI) since SOI is suitable for lower-voltage operation compared to conventional bulk devices [7]. Especially, fully depleted SOI (FDSOI), whose channel region is thinner and more depleted than conventional partially depleted SOI (PDSOI), has been developed to achieve lower voltage operation [8]. Moreover, silicon on thin buried oxide (SOTB) device, which is an FDSOI device, has better threshold voltage controllability with body biasing by thinning the insulator layer (buried oxide; BOX) under the channel region [9,10]. More recently, fin field-effect transistor (FinFET), which has better channel controllability thanks to multiple-side gate wrapping the fin, is becoming the mainstream transistor structure beyond 20-nm technology.

Depending on the fabrication technology and operating voltage, the immunity to radiation varies. When pursuing a low-voltage operation, the soft error rate (SER) increases as the supply voltage decreases in general because critical charge, which is the charge threshold to cause a soft error, decreases [11]. If the SER of near-threshold circuits is much higher than that in the super-threshold (nominal supply voltage) region, it would not be appropriate to use near-threshold computing for reliability-demanding applications. Furthermore, the new transistors have different characteristics against radiation, and the mechanism of soft error can change. Therefore, soft error immunity must be characterized for designing reliable integrated systems.

This paper discusses the SER characterization of static random access memory (SRAM) and flip-flop (FF), which are the most sensitive components in VLSIs [12], with irradiation experiments and simulation. The presented results cover conventional bulk transistor, which continues to be used for cost-effective IoT applications, FDSOI, and FinFET transistors. Furthermore, muon-induced soft error is also discussed as a future reliability concern.

Improving soft error immunity is studied at various levels, such as system, architecture, software, circuit, and device levels. At system level, redundancy based fault tolerance, such as triple modular redundancy (TMR), is often adopted in mission critical applications. At architecture level, hardware instruction retry in a microprocessor [13], fine-grained TMR in FPGA [14], etc. are studied. At software level, fine-grained code duplication and check code insertion is a popular approach to detect soft errors [15]. This paper focuses on and introduce circuit and device level countermeasures to soft error.

This paper is organized as follows. Section 2 explains soft error occurring in terrestrial environment. Section 3 presents measured SRAM SER and discusses multiple cell upset (MCU) with an emphasis on low voltage operation. Section 3 introduces radiation-hard FFs with irradiation test results. Soft error simulation requires multi-physics simulation covering nuclear physics, device physics, and circuit behaviors. Such a multi-physics simulation framework is exemplified in Section 5. Finally, Section 6 discusses the future trends including FinFET SER and muon-induced soft error, and Section 7 gives concluding remarks.

2. Soft error in terrestrial environment

Radiation effects can lead to permanent and temporal errors. There are three radiation effects in electron devices; total ionizing dose (TID) effect, displacement damage dose effect (DDD), and single event effect (SEE), where DDD and TID are not visible in terrestrial radiation environment whereas they are significant in space applications. TID represents a long-term degradation due to the cumulative energy deposited in a material, and DDD is the cumulative degradation especially resulting from the displacement of nuclei in a material. SEE is caused by a single event of a particle incident, resulting in temporal or permanent errors. SEE includes following phenomena; SEU, single event transient (SET), single event latchup (SEL), single event burnout (SEB) and single event gate rupture (SEGR). Here, SEB, induces a localized high-current state resulting in catastrophic failure, and SEGR, which causes a breakdown and subsequent conducting path through the gate oxide, occur in power devices and then they are not discussed in this paper. SEU and SET are often called soft error since they are temporal error and are not hard error. SEL is a latchup caused by single energetic particle. Local SEL could occur in SRAM manufactured in advanced technologies, and as possible solutions, current-limiting device (CLD) based detection [16] and well structure modification [17] are proposed. However, SEL cannot be eliminated by architecture-level countermeasures, which is a distinct difference from SEU and SET. Therefore, SEL is not discussed in this paper.

When an ionized radiation particle goes into the silicon substrate of a transistor, electron-hole pairs are generated. After that, the transport of generated electron-hole pairs, such as diffusion and drift, collects electric charge to the drain region of the transistor [1]. The collected charge finally induces a temporal glitch at the drain node of the transistor. Temporal errors caused by this glitch are called soft errors. More specifically, a glitch occurring in a combinational circuit is called SET, and a glitch that occurs in a memory element and upsets the memory information is called SEU. The critical region inside the silicon substrate where an ionized particle hit causes a soft error is called a sensitive node or sensitive volume.

In terrestrial environment, soft errors are induced by alpha particles emitted from package material and neutrons originating from cosmic ray. Alpha particles are ionized radiation particles and hence they can directly generate electron-hole pairs, as illustrated in Fig. 1. Neutrons, on the other hand, indirectly induce soft error through reaction with atomic nucleus of transistor materials, which is also shown in Fig. 1. The nuclear reaction generates charged secondary particles like protons, alpha particles and heavy ions. The charged particle generates electron-hole pairs on the particle track and deposits charge. The generated charge is collected to the drain by drift and diffusion, and causes

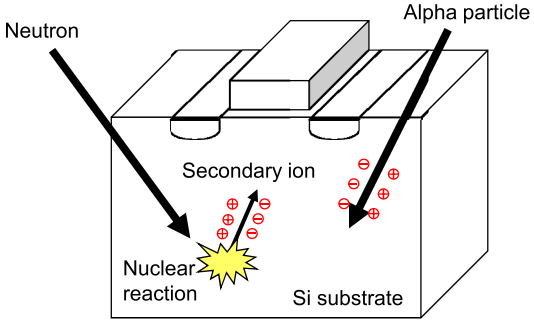

Fig. 1. Soft error mechanism due to neutron and alpha. ©[2013] IEEE. Reprinted, with permission, from Ref. [20].

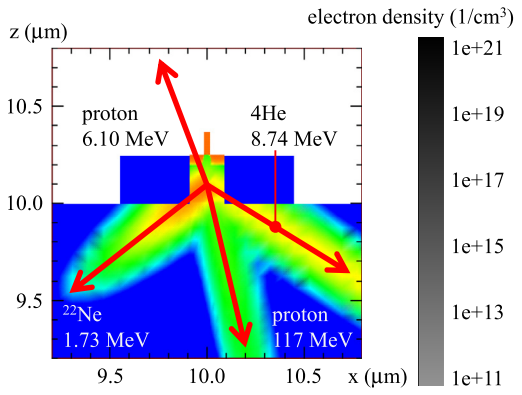

Fig. 2. An example of nuclear reaction, n + ^{28}Si → n + 2p + ^{4}He + ^{22}Ne, and charge deposition due to secondary ions.

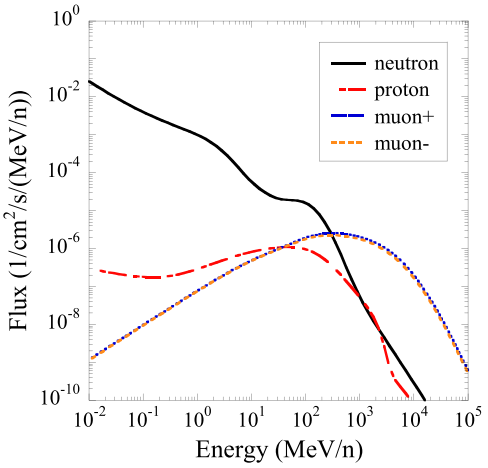

Fig. 3. Energy spectra of major secondary cosmic ray particles at NYC obtained with EXPACS [22,23].

soft error. An example of such nuclear reactions and charge deposition due to the generated secondary particles is shown in Fig. 2. Alpha particle induced soft error can be mitigated by using a low alpha emission package. On the other hand, although building can somewhat reduce neutron flux [18], neutrons are difficult to be eliminated in general, and then neutron is the major source of soft error in terrestrial environment [19].

Besides, recent literature (e.g. Ref. [21]) points out that muons are a potential source of soft error in the terrestrial environment. Fig. 3 shows the energy spectra of major secondary cosmic ray particles. A substantial component of secondary cosmic rays at ground level is known to be muons [21], and its fraction is about three-quarters of the total cosmic ray flux. Muon-induced soft error will be therefore discussed in Section 6.2.

3. SRAM

This section discusses SRAM soft error immunity to neutron focusing on low voltage operation and presents measurement results of neutron-induced soft errors over a wide range of supply voltages down to 0.3 V mainly reported in Refs. [24–26]. Existing studies have shown that the neutron-induced SER in SRAM increases as the supply voltage is lowered [27,28], which is because reducing the supply voltage decreases the energy required to cause upsets. These studies, however, were done using a voltage between the nominal supply voltage and 0.8 V, and near-threshold and subthreshold ranges were not investigated.

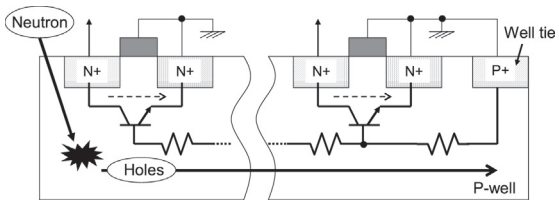

Fig. 4. Cross section of bulk NMOSs in memory cells. Parasitic bipolar transistors cause multiple upsets due to increase in potential of P-well. ©[2011] IEEE. Reprinted, with permission, from Ref. [25].

3.1. MCU mechanism and its countermeasure

MCUs induced by a single neutron are becoming a serious concern [28–30]. MCUs can be mostly mitigated by interleaving and error correction code (ECC). On the other hand, as the number of upsets for an event becomes larger, MCU patterns which cannot be eliminated by interleaving and ECC are more likely to arise. Such critical MCUs are called MBU (multiple bit upsets), and they prevent massively-parallel high-performance computing systems and highly reliability-demanding applications from being implemented and operated. Besides, there are four possible mechanisms of MCU; (1) successive hits of an ion, (2) multiple hits by multiple ions, (3) charge drift/diffusion (charge sharing), and (4) parasitic bipolar action (PBA).

In bulk SRAM, (3) charge sharing and (4) parasitic bipolar action are major mechanisms at the nominal supply voltage. Charge sharing causes MCU due to charge diffusion to multiple cells. Parasitic bipolar action triggered by well potential fluctuation flips multiple cells in a well. Fig. 4 illustrates the parasitic bipolar action in bulk SRAM. Holes generated by a neutron-induced nuclear reaction elevate the voltage of the P-well, which is equivalent to the base-emitter voltages of the parasitic bipolar transistors, due to well resistance. Consequently, the collector-emitter current of the parasitic bipolar transistors increase, which causes MCUs. Regarding supply voltage, these two mechanisms have opposite tendencies. As the supply voltage becomes lower, the critical charge becomes smaller, which makes charge sharing-induced MCUs occur easily. On the other hand, the parasitic bipolar action becomes less active due to lower collector-emitter voltage, and consequently, MCUs due to the parasitic bipolar action are less likely to arise. The mixture of these two tendencies determine the dependency of MCU on voltage, which is illustrated in Fig. 5.

In SOTB SRAM, on the other hand, MCUs due to (3) charge sharing and (4) parasitic bipolar action do not occur since SOTB transistors do not share a well. Therefore, the remaining (1) successive hits of an ion and (2) multiple hits by multiple ions cause MCUs in SOTB SRAM. Consequently, the MCU rate is lower and large-bit MCUs are less probable to occur in SOTB SRAM.

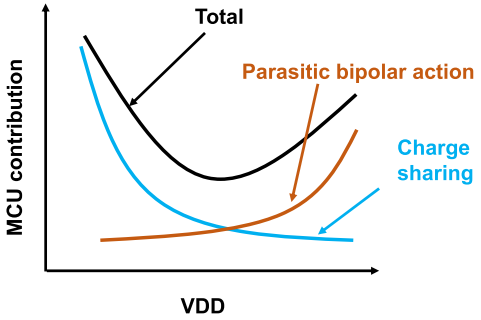

Fig. 5. Qualitative explanation of contributions of PBA and charge sharing to MCU in bulk SRAM.

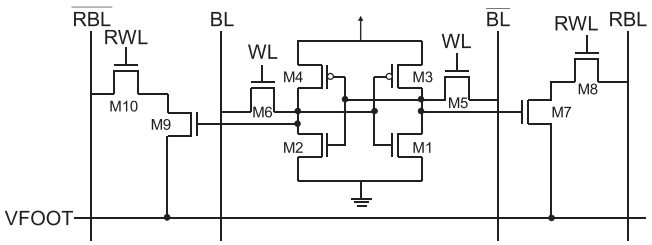

Fig. 6. Structure of 10 T memory cell. ©[2011] IEEE. Reprinted, with permission, from Ref. [25].

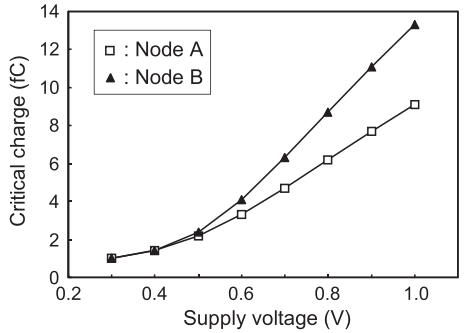

Fig. 7. Simulated critical charge of 10 T memory cell as a function of supply voltage in 65-nm CMOS process. Nodes A and B represent two individual sensitive nodes in a memory cell. ©[2011] IEEE. Reprinted, with permission, from Ref. [25].

These qualitative discussions on MCU, voltage dependency and the difference between bulk and SOTB will be validated with measurement results in the following.

3.2. 65-nm 10 T subthreshold bulk SRAM

3.2.1. Experimental setup

A test chip including a 256 kb 10 T SRAM was fabricated in a 65-nm CMOS bulk process with triple well structure. Fig. 6 shows the cell structure of the 10 T SRAM. This SRAM can operate even at 0.3 V because the cross-coupled inverters are large enough to mitigate threshold voltage variability. The size of a memory unit is 4.4 μm × 0.8 μm. To investigate the contribution of the parasitic bipolar action to the occurrence of MCUs, we implemented two types of memory cell arrays having different distances between the well ties; 25.6 μm (wide) and 6.4 μm (narrow).

Vulnerability of a memory cell to radiation particles is often evaluated using critical charge, which is defined as the minimum charge required to flip the data stored in a memory cell. Fig. 7 shows the critical charge obtained by circuit simulation with a double exponential current model. The critical charge decreases as the supply voltage is reduced, which means that reduction in the supply voltage degrades immunity to radiation particles.

Irradiation experiments were carried out as follows. Accelerated high-energy-neutron SER measurements were performed at the Research Center for Nuclear Physics (RCNP) at Osaka University, Japan [28]. The energy spectrum of the RCNP neutron source is similar to the terrestrial neutron energy spectrum [28,30].

3.2.2. Measurement results

Fig. 8 shows the neutron-induced SER as a function of the supply voltage. The SER increases as the supply voltage is reduced. The SER at 0.3 V is 7.8 times higher than at 1.0 V.

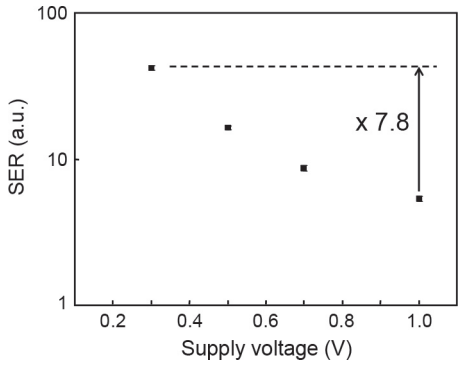

Fig. 8. Neutron-induced SER as a function of supply voltage of memory cell array. Each error bar indicates ±3σ, where σ is defined as the square root of the number of the observed upsets. ©[2011] IEEE. Reprinted, with permission, from Ref. [25].

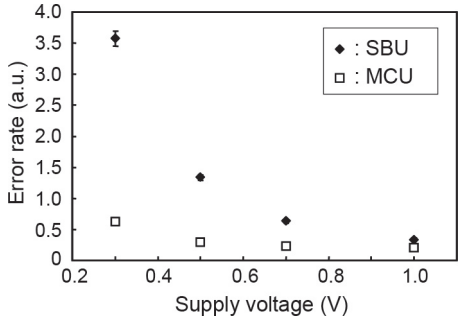

Fig. 9. Neutron-induced SBU and MCU rates as a function of supply voltage of memory cell array. SBU and MCU rates are plotted with error bars, where each error bar indicates ±3σ. ©[2011] IEEE. Reprinted, with permission, from Ref. [25].

Fig. 9 illustrates the dependence of the SBU (single bit upset) and MCU rates on the supply voltage. Here, the MCU rate was derived by dividing the number of failing bits (for example, a “2b MCU” was considered to be two errors) during the measurement period. The SBU rate dramatically increases as the supply voltage is reduced.

As described with Fig. 7, the decrease in the supply voltage reduces the critical charge. Ibe et al. [31] reported that SBU is dominated more significantly as technology scaling proceeds due to lighter particles such as protons and alpha particles, which are secondary particles produced by the nuclear reaction between neutrons and Si. Rigidly speaking, the reduction in the supply voltage and the device miniaturization are different in terms of the sensitive volume and the charge collection efficiency. Meanwhile, the supply voltage reduction corresponds to the device miniaturization in terms of the critical charge. Decomposition of SEUs into their triggering secondary particles will be discussed in Section 3.2.3.

On the other hand, the dependence of the MCU rate on the supply voltage is smaller than that of the SBU rate. A reason is that the contribution of lighter particles to MCUs is smaller than that to SBUs since lighter particles cannot deposit charge large enough to trigger the parasitic bipolar action [31]. Interestingly, however, the MCU rate shown in Fig. 9 slightly increases when the supply voltage is below 0.5 V. Remind that the charge sharing and parasitic bipolar action have opposite directions in terms of supply voltage, as mentioned in Section 3.1. While the parasitic bipolar action is the dominant mechanism of MCUs in the super-threshold region in this particular design, the effect of charge-sharing becomes larger in the near-threshold and subthreshold regions, which results in the increase in the MCU rate between 0.3 and 0.5 V, as depicted in Fig. 9.

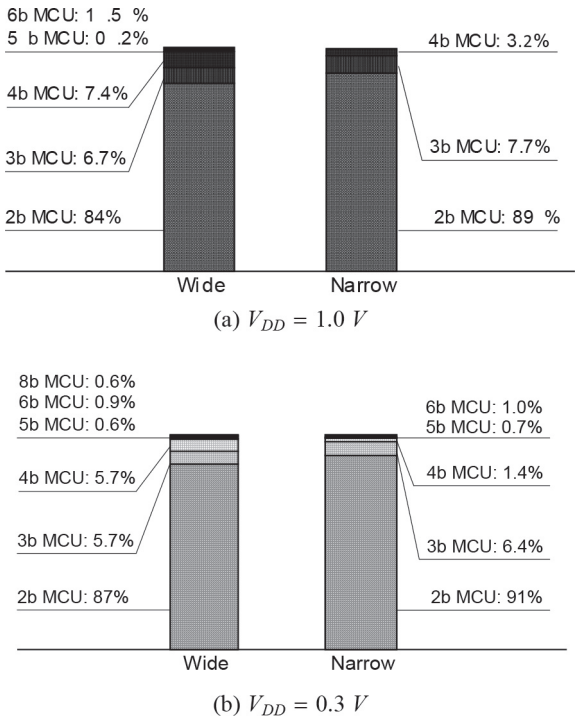

Fig. 10. Comparison of neutron-induced MCU distributions. ©[2011] IEEE. Reprinted, with permission, from Ref. [25].

Finally, the MCU distributions in the memory cells with wide and narrow well-tie distances are shown in Fig. 10. Large-bit MCUs are likely to occur in memory cells with a wide well-tie distance compared to ones with a narrow well-tie distance since the distant well-ties are less effective to keep the well potential and consequently prevent the parasitic bipolar action. A decrease in the supply voltage also increases the probability of large-bit MCUs due to the decrease in the critical charge. 8-bit MCU was observed at 0.3 V. In bulk SRAM, most of MCUs occur in the same well, and then the SRAM is designed such that bit cells in the same well are not included in the same word to make ECC effective.

3.2.3. Simulation

To investigate the secondary particles contributing to SEUs, a Monte Carlo simulation was performed using PHITS (Particle and Heavy Ion Transport code System) [32]. PHITS is employed to simulate neutron-induced soft errors together with a 3-D TCAD (Technology Computer Aided Design) simulator in Ref. [33], which will be explained in Section 5. In this section, on the other hand, the collected charge is calculated by a sensitive volume model [34].

Fig. 11 shows the simulated SEU probability including both SBU and MCU per neutron flux as a function of critical charge at the incident angles of 60° and 0°. Individual contributions from secondary H (proton), He (alpha), and heavier ions to the SEU are separated for the result of 0° in Fig. 11. There is little difference between the SEU probabilities at the angles of 60° and 0°. On the other hand, the critical charge of our 10 T SRAM in 0.4-V operation estimated by circuit simulation is 1.4 fC (Fig. 7). Therefore, He and heavier ions are the dominant secondary ions causing SEUs in 0.4-V operation because these ions occupy 89% of the SEU probability at 1.4 fC of critical charge.

On the other hand, a more recent report [35] demonstrates two orders of magnitude increase in soft error rate at 0.19 V compared from 1.0 V. This drastic increase is well explained by the contribution of secondary proton, and this tendency is supported by PHITS simulation in

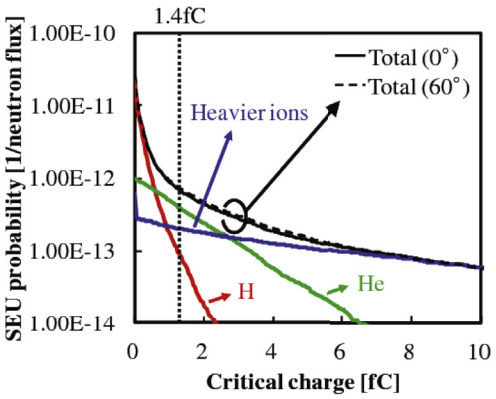

Fig. 11. Simulated SEU probability of each ion as a function of critical charge. ©[2012] IEEE. Reprinted, with permission, from Ref. [24].

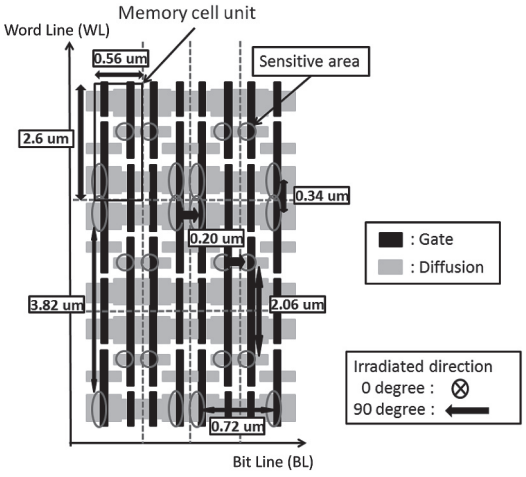

Fig. 12. SRAM cell layout.

Ref. [35]. The latest bulk SRAM may encounter drastic SEU increase unexpectedly when the supply voltage is aggressively lowered.

3.3. 65-nm 6 T SOTB and bulk SRAMs

3.3.1. Experimental setup

Two SRAM test chips of SOTB and bulk devices were fabricated in a 65-nm CMOS technology with eight metal layers from the same Graphic Data System (GDS) data. A major difference between SOTB and bulk devices is the existence of the BOX layer under the channel region. The thickness of the BOX layer in SOTB devices is 10 nm while other SOI devices often have BOX layers thicker than 100 nm [36–38]. Fig. 12 shows the layout of the 6 T SRAM cell designed according to the logic design rule. In both SOTB and bulk SRAMs, the SRAM area is covered by a deep N-well.

Neutron irradiation test was carried out at RCNP of Osaka University. Four SOTB SRAM boards and two bulk SRAM boards, on each of them 16 chips are mounted, were irradiated, where the boards were aligned to be perpendicular to or in parallel to the beam track. These irradiation angles correspond to the notations of 0° and 90° in Fig. 12, respectively.

3.3.2. Measurement results

Fig. 13 shows the measurement results of the accelerated neutron test with voltage scaling. Note that the definition of MCU here states that two or more simultaneous upsets are in vertically, horizontally,

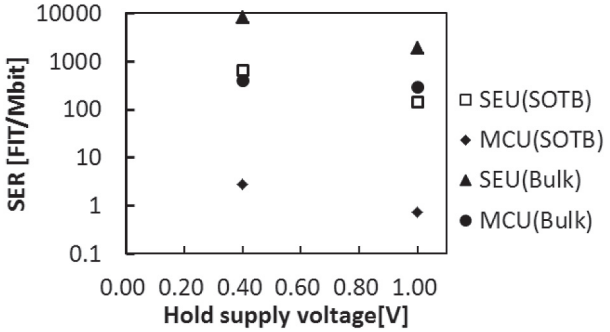

Fig. 13. Measured neutron-induced SEU and MCU vs. supply voltage (0°). Each error bar indicates the standard deviation of the obtained upsets. ©[2015] IEEE. Reprinted, with permission, from Ref. [26].

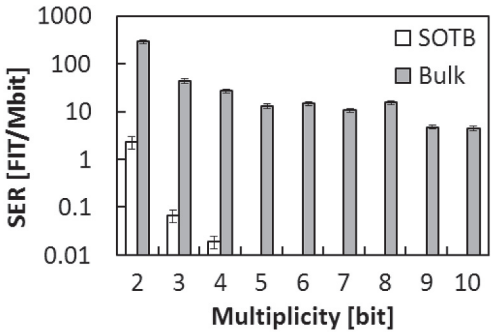

Fig. 14. Measured neutron-induced MCU rate as a function of number of bit flips in the SOTB and bulk SRAMs at 0.4 V and 0°. ©[2015] IEEE. Reprinted, with permission, from Ref. [26].

and/or diagonally adjacent bits. The number of measured SEUs on the SOTB SRAM at 0.4-V supply voltage was 4.4 times larger than that at 1.0-V supply voltage, while the number of SEUs on the SOTB SRAM at 0.4 V was 0.08 times smaller than that on the bulk SRAM at 0.4-V supply voltage. The number of SEUs on the SOTB SRAM at 0.4-V operation was roughly equivalent to that on the bulk device at 1.0 V. On the other hand, the numbers of measured MCUs on the SOTB SRAM at 0.4 V and 1.0 V were 0.01× and 0.003× smaller than those on the bulk SRAM, respectively. Therefore, roughly speaking, SOTB SRAM can achieve more than two orders of magnitude lower SER when ECC is applied.

Fig. 14 shows the MCU rates for each number of simultaneous bit flips in the SOTB and bulk SRAMs at the incident angle of 0°. As the number of bit flips increases, the number of measured MCUs quickly decreases in the SOTB SRAM, while it slowly decreases in the bulk SRAM. Even the MCU rate of simultaneous 10-bit flips in the bulk SRAM is higher than the MCU rate of 2-bit flips in the SOTB SRAM. In terms of MCU, SOTB is superior to bulk since MOS transistors are isolated by the BOX layer in SOTB and the charge sharing and parasitic bipolar action do not occur, as discussed in Section 3.1. Note that even in bulk SRAMs, 0.4-V operation is supposed to make the parasitic bipolar action less active as illustrated in Fig. 5. Fig. 15 shows the result at the incident angle of 90°. In this case, 9-bit MCU occurred even in the SOTB SRAM, while its rate was more than three orders of magnitude lower than that of the bulk SRAM. This result is explained by the fact that secondary ions contributing to MCU tend to be emitted forward and pass through multiple memory cells along the neutron beam. When the incident angle is 90°, the secondary ions emitted forward by nuclear reaction travel parallel to the chip surface, and they are more likely to pass through multiple sensitive volumes for upsets. Hence, larger MCUs were observed at the incident angle of 90°.

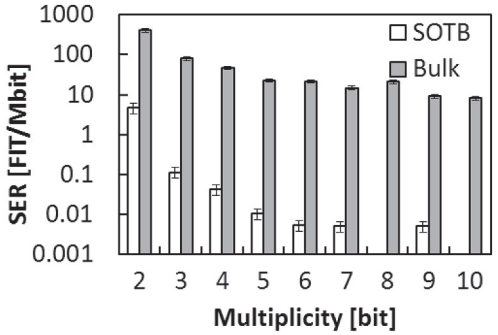

Fig. 15. Measured neutron-induced MCU rate as a function of number of bit flips in the SOTB and bulk SRAMs at 0.4 V and 90°. ©[2015] IEEE. Reprinted, with permission, from Ref. [26].

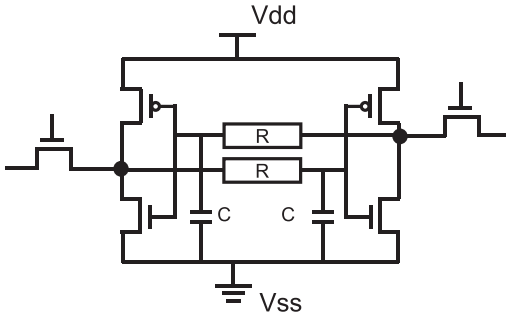

Fig. 16. SRAM cell hardening.

This MCU mechanism due to successive multiple hits of sensitive volumes makes upset classification difficult in simulation since the secondary ions traveling parallel to the chip surface pass through not only off transistors but also on transistors. Ref. [39] points out that the upset classification based on the charge deposited to on transistors in addition to off transistors improve the accuracy. Machine learning based classifier construction proposed in Ref. [39] could be effective for accurate MCU estimation.

3.4. SRAM cell hardening

In addition to ECC, SRAM cell hardening for SEU mitigation has been studied to improve the immunity of individual SRAM cells to radiation. Basically, a few passive elements are added to common 6-T SRAM cell.

Reference [40] proposed to insert two resistances R inside the cross-coupled inverters as shown in Fig. 16. The inserted resistances reduce the amount of collected charge and delay the pulse propagation to the paired inverter input, which improves the immunity to radiation. For the similar purpose, Ref. [41] proposed to replace PMOS transistors to very high resistance elements.

Reference [42] proposed to add two capacitors C1 in addition to R as shown in Fig. 16. Capacitors C further delay the pulse propagation. The authors claim this resistive and capacitive feedback hardening method is more effective in SOI than bulk transistors. More recently, the SRAM presented in Ref. [43] adopted a 3D structure to increase C dramatically without increasing the cell area [44].

4. Radiation-hard flip-flops

Flip-flops are cells that temporarily store data on a chip, and they are key components to organize sequential circuits, such as pipeline circuits and control logic. Therefore, an unwanted flip of stored

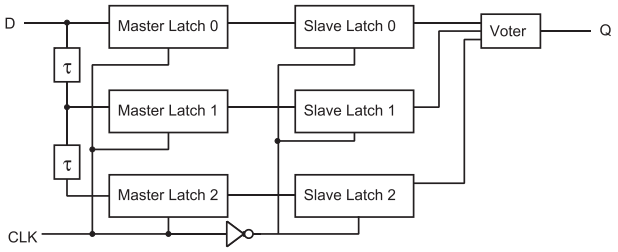

Fig. 17. Triple-modular-redundancy flip-flop.

data may result in failure in data path and state machine. Increasing their radiation hardness protects semiconductor chips from malfunctioning. This section discusses radiation-hard D flip-flops (DFF) and compares conventional and recent state-of-the-art radiation-hard FFs.

Redundancy is a frequently-used technique against soft errors, and it is often introduced in FF error mitigation. In this case, storage cells are duplicated to detect a flip, or triplicated to correct the flip. Dual lockstep is a well-known system/processor-level technique to guarantee functional safety for automotive systems, which is defined in an international standard of ISO 26262. In a typical dual lockstep system, two processors are working together to perform the same operations with a certain amount of time difference. If the results from the duplicated processors are inconsistent, the same operations are repeated. Dual lockstep is a simple mitigation technique against soft errors, but its area and performance overheads are not negligible. Therefore, a low overhead solution to avoid failures in sequential circuits is demanded in many applications.

4.1. Bit-level redundancy

For enhancing reliability with small overhead, redundant storage cells are utilized. SRAMs have redundant bits to correct or detect errors by single-error correction and dual-error detection (SECDED) mechanism [45]. However, SECDED cannot be applied to FFs since errors cannot be corrected and detected within a single clock cycle and FFs are not placed as an array. For FFs, therefore, bit-level redundancy is mandatory to correct the stored data. Triple modular redundancy FF (TMR-FF) in Fig. 17 is a simple and powerful mitigation technique for soft errors, but it involves large power, delay and area overheads. τ is a delay element to prevent an SET pulse from being captured to multiple redundant latches. The possibility to capture an SET pulse to a latch is proportional to clock frequency. Ref. [46] describes that the SER by an SET pulse from combinational circuits on a chip fabricated by a 28-nm CMOS technology becomes larger than the SER by a particle hit on FFs over 300 MHz at 0.9-V supply voltage.

4.2. Transistor-level redundancy

For reducing power, delay and area overheads, various latches and FFs other than TMR have been proposed. For a bulk process, duplicating or triplicating stored data so called the multi-modular structure is effective to mitigate upsets of storage cells. On the other hand, in an SOI process, duplicating or triplicating storage cells is not mandatory when series-stacked transistors, which are not influenced simultaneously in SOI, are exploited. This section introduces FFs for bulk and SOI processes as well as a low-power radiation-hard FF.

4.2.1. Multi-modular flip flop

Dual-interlocked storage-cell (DICE) is the most famous one, which is utilized on central processing units (CPUs) for high-performance computers [47–49]. Fig. 18 shows a schematic diagram of the DICE latch. It consists of duplicated latches, and it includes four half Muller C-elements (HCE). Two input pins of the HCE are connected to the output pins of different HCEs. Even if an ion penetrates into one of HCEs and the output pin generates an SET pulse, the output pins of the other HCEs do not fluctuate and then extinguish the SET pulse.

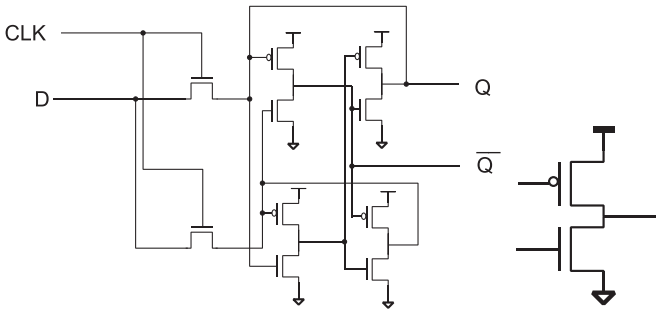

Fig. 18. DICE latch (left) and half Muller C-element (right).

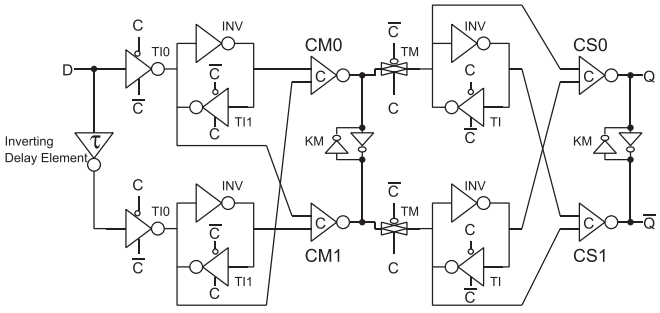

Fig. 19. BCDMR FF.

We proposed bistable cross-coupled dual modular (BCDMR) FF (Fig. 19) based on the built-in soft error resilient (BISER) FF (Fig. 20) [50–52]. BISER consists of duplicated latches, C-elements, and weak keepers. Stored value is kept even when an ion penetrates into the weak keeper or one of the duplicated latches. Therefore, BISER FF eliminates an unexpected flip caused by an SEU. A drawback of the BISER FF is that C-element CM generates an SET pulse, and then it may be captured by the duplicated slave latches. As described in Section 4.1, the possibility of capturing an SET pulse becomes higher in proportion to the clock frequency. The BCDMR FF, on the other hand, is robust against soft errors at a higher clock frequency since the C-elements are duplicated, and the weak keepers are replaced by the keeper consisting of inverters with the same transistor size. Even when one of the duplicated C-elements generates an SET pulse, the other C-element and the keeper store the original value and eliminate the SET pulse. On the contrary, the weak keeper cannot keep the original value because it is composed of two inverters with differently-sized transistors. The inverter in the weak keeper connected to the output node of the C-element must have lower drivability than the C-element to enable the C-element to overwrite the stored value.

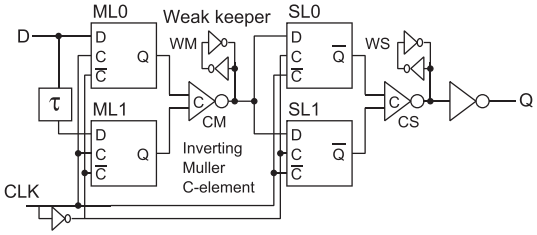

Fig. 20. BISER FF.

Table 1
SERs in FIT/Mbit by neutron irradiation results of the redundant FFs w/o considering MCUs as shown in Fig. 22 (a).

	Clock Freq.		
	1 MHz	100 MHz	200 MHz
BISER FFs	130	150	150
BCDMR FFs	8	71	48
D-FFs	1,031 (no clock is applied)		

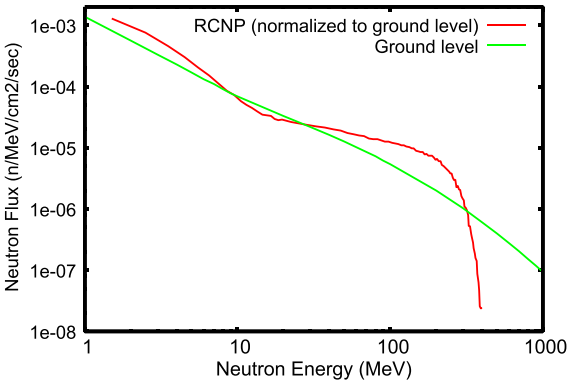

Fig. 21. Neutron spectrum at ground level and that of white neutron beam at RCNP normalized to ground level.

We fabricated and irradiated a test chip with both of BISER and BCDMR FFs to 3 MBq α foil by changing clock frequency from 1 MHz to 160 MHz. The SER of BISER at 160 MHz becomes 5.5 times larger than at 1 MHz, while BCDMR keeps the same SER level at 1 and 160 MHz [50].

Due to the asymmetrical structure of the weak keeper, the BISER FF is also weak against process variations. We demonstrated that the BCDMR FF on the twin well fabricated by a 65-nm bulk process has 55% smaller variations than the BISER FF [53].

Aggressive process scaling has been worsening MCU rates. Ref. [54] investigates MCU rate according to process scaling. It suggests that the ratio of MCU/SEU is approaching 100% when the distance between the duplicated circuit elements is around 0.3 μm. The spectrum of neutron at the sea level is broadly distributed over 1000 MeV as shown in Fig. 3. The BCDMR FF is strong against relatively low-energy α irradiation. However, high-energy neutrons generate much more electron-hole pairs to influence adjacent circuit elements. Table 1 shows SERs by the spallation white neutron beam with the spectrum in Fig. 21 at RCNP, Osaka University. Both BISER and BCDMR FFs have higher SERs at higher clock frequency by neutron irradiation unlike the alpha irradiation, which suggests the redundant circuit elements are simultaneously affected by a single secondary ion.

To prevent two redundant circuit elements from being influenced by a single ion, we designed and fabricated a chip in a 65-nm bulk process including interleaved standard cells of the BISER and BCDMR FFs [55]. Fig. 22 compares the conventional non-interleaved placement (a) of the BCDMR FF and the interleaved placement (b) in which the sensitive circuit pairs are located as far apart as possible. Each sensitive circuit element has its pair that should not be affected simultaneously, and then the paired elements become critical to a particle hit close to them. Placing those paired elements with a larger distance reduces the possibility of upsetting those elements at the same time.

Table 2 shows SERs in FIT/Mbit. The SERs of the interleaved BCDMR FF becomes all zero. On the other hand, in the interleaved BISER FF, bit flips by soft errors are still found, and the SERs are increased by the clock frequency due to an SET pulse coming from the C-element [55] as already mentioned.

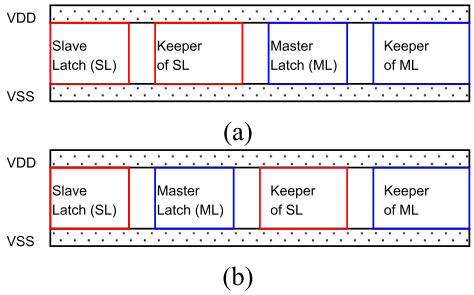

Fig. 22. Non-interleaved conventional (a) and interleaved (b) placement of the BCDMR FF. Red and blue pairs are sensitive circuits. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Table 2
SERs in FIT/Mbit of interleaved redundant FFs by neutron irradiation with the layout structures of Fig. 22 (b).

	Clock Freq.[MHz]			
	1	10	100	300
BISER	18	26	44	212
BCDMR	< 9 (No error)			–

4.2.2. *Low-power radiation-hard flip flop*

Low power operation is mandatory on battery-operated devices and also on high-performance computers dissipating huge amount of power with hundreds of thousands of processing units. The adaptive-coupling FF (ACFF) [56] in Fig. 23 is one of low-power FFs without any multiplication to prevent soft errors. ACFF embeds two AC (adaptive-coupling) elements to refresh a stored value by a single phase of a clock signal (CLK). Without using the other phase of a clock signal ($\overline{\text{CLK}}$), no clock buffer is required.

Combining the structure of ACFF and other multi-modular FFs, DICE ACFF and BCDMR ACFF were developed to intend both of low power and radiation hardness [57,58]. Figs. 24 and 25 show those FFs. Power consumption of the ACFF structure become smaller as decreasing data activity (α) since power consumption of clock buffers can be reduced by sharing them among several FFs. Fig. 26 shows power consumption of the conventional non-redundant (DFF and ACFF), redundant (DICE and BCDMR FFs) and low-power redundant FFs (DICE and BCDMR ACFFs) normalized by the power of DFF. At $\alpha = 10\%$, power consumption of BCDMR and DICE ACFFs become close to DFF.

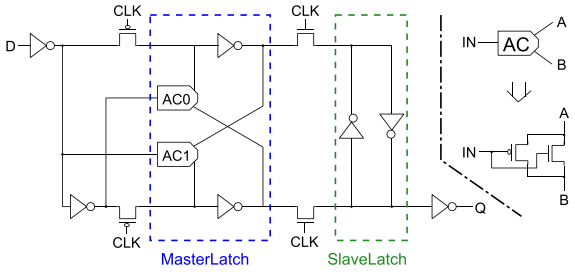

Fig. 23. Adaptive coupling flip flop.

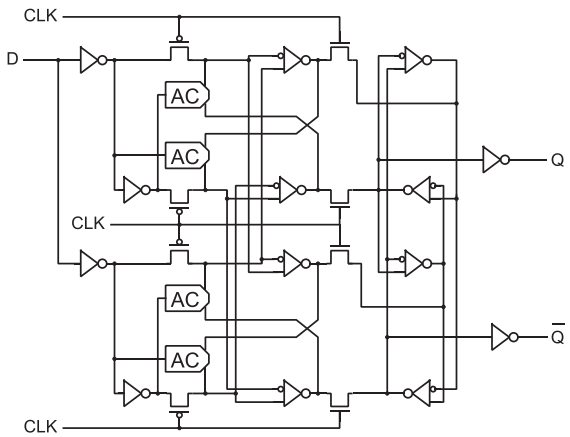

Fig. 24. DICE ACFF.

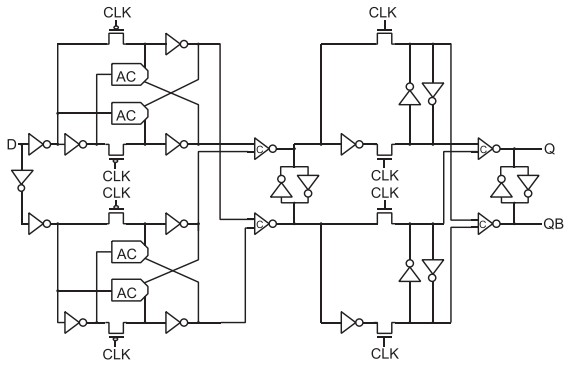

Fig. 25. BCDMR ACFF.

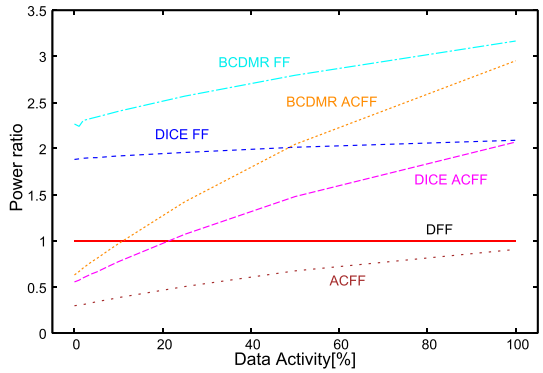

Fig. 26. Power dissipation of non-redundant (ACFF), redundant (DICE and BCDMR FFs) and low-power redundant FFs (DICE and BCDMR ACFFs) normalized by power of DFF.

4.2.3. *Flip flops with series-connected stacked transistors for FDSOI*

To suppress short channel effects in highly-scaled process nodes, process-level and fabrication-level developments have progressed. FDSOI is one of the promising candidates for planar structures, and the other one is FinFET, which will be introduced in Section 6.1 in detail. FDSOI suppresses short channel effects by constructing transistors on a BOX layer. Transistor channel is formed in a thin silicon layer on the BOX layer. FDSOI is strong against soft errors since the generated carriers in the bulk substrate region are not collected to the drain region. Fig. 27 compares neutron-induced SERs of conventional DFFs fabricated by 65-nm bulk and FDSOI processes, respectively [57]. The

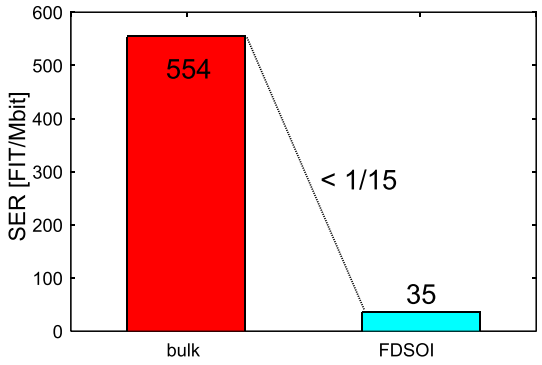

Fig. 27. Comparison of SERs in FIT/Mbit of DFFs between bulk and FDSOI at VDD = 1.2 V by neutron irradiation applying 35 MHz clock.

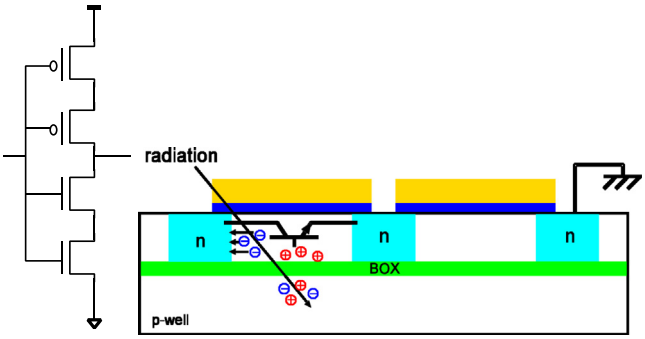

Fig. 28. Stacked inverter (left) and its cross section of stacked NMOSFETs (right).

SER of FDSOI is 1/15 times smaller than that of bulk. Note that DFFs in bulk and FDSOI processes share the same layout structure.

One of the radiation-hard circuit structures for FDSOI is the stacked inverter, in which two transistors are series-connected as shown in Fig. 28 [59]. In FDSOI, every transistor channel is isolated by the BOX layer. Fig. 29 depicts a structure of the stacked FF that consists of stacked inverters and clocked inverters. A radioactive particle affects only a MOSFET through which the particle is going and then turns on the MOSFET. If two transistors are stacked, one of those is still in OFF state, which prevents an SET pulse from propagating to the output node as shown in Fig. 28.

The stacked FF has a drawback in delay time because the stacked inverter drives the transmission gate between the master and the slave latches. To decrease the delay overhead, we proposed the stacked leveling critical charge FF (SLCCFF) (Fig. 30) [60]. Although the basic structure of SLCCFF is similar to the stacked FF with high soft error immunity, the connections between the master and slave latches are

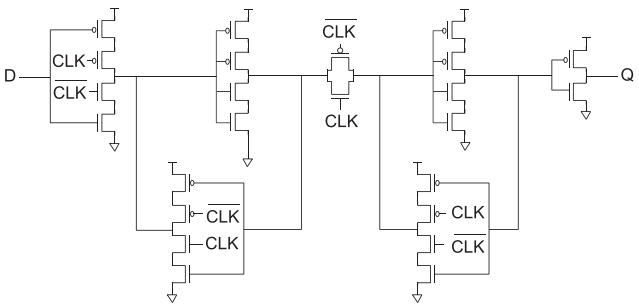

Fig. 29. Stacked FF.

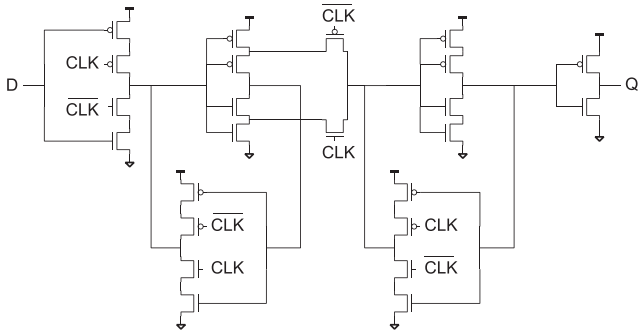

Fig. 30. SLCCFF.

Table 3
Energy, delay and area comparison.

	Energy	Delay	Area
DFF	1.00	1.00	1.00
Stacked FF	2.13	2.00	1.12
SLCCFF	1.89	1.67	1.24

Table 4
Average neutron- and alpha-induced SERs of DFF, stacked FF and SLCCFF at 1.2 V in a 65-nm FDSOI process.

	neutron	α particle
DFF	1.00	1.00
Stacked FF	0.34	0.026
SLCCFF	0.45	0.008

different. In the stacked FF, both of the PMOS and NMOS transistors are connected to the regular output terminal of the stacked inverter in the slave latch, while in SLCCFF the PMOS and NMOS transistors are connected to different nodes between the pair of the PMOS or NMOS stacked transistors in the master latch. The slave latch is charged or discharged through three transistors in the stacked FF but through two transistors in SLCCFF. It makes the SLCCFF delay smaller than the stacked FF. Tables 3 and 4 compare energy, delay, area overhead and SERs of a conventional DFF and the stacked FF and SLCCFF. Although the area of SLCCFF is 11% larger than the stacked FF, the delay time of SLCCFF is reduced to 78% of the stacked FF. Both of the stacked FF and SLCCFF have almost the same SERs and 1/3 times lower than DFF to neutron radiation.

4.2.4. *Low-power flip flops with stacked transistor structure for FDSOI*

As explained in Section 4.2.2, ACFF without local clock buffers achieves low power. Low-power radiation-hard flip flops can be implemented for FDSOI by combining the stacked transistor with ACFF. Figs. 31 and 32 show two structures named the AC All Stacked FF (AC_AS FF) and the AC Slave Stacked FF (AC_SS FF) [61].

The AC structure itself is low-power and strong against soft errors since the AC element attenuates an SET pulse. Table 5 compares area, power and the number of transistors. AC_SS FF and AC_AS FF has 12% and 24% area overheads, respectively, compared with ACFF and DFF, while they have only less than 10% power overheads.

Fig. 33 shows how an SET pulse from the node n0 is attenuated at the node n1 after the SET pulse passes through the AC element AC0. Even by the SET pulse down to 0.4 V from 0.8 V, the voltage level of n1 goes down to around 0.7 V, which is only 0.1 V perturbation. AC_AS FF has two stacked structures on the master and slave latches, while AC_SS FF has no stacked structure on the master latch. By owing the pulse

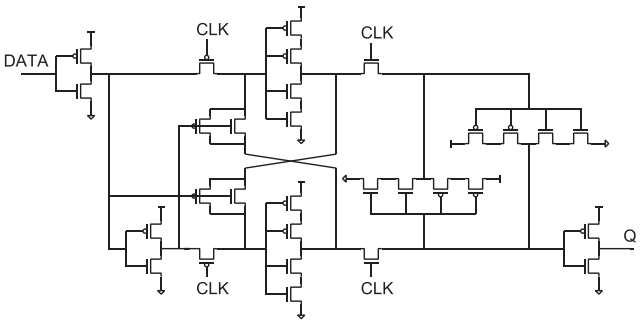

Fig. 31. AC all stacked FF.

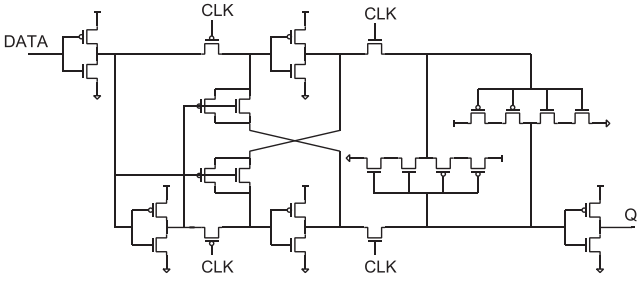

Fig. 32. AC slave stacked FF.

attenuation capability of the AC element, AC_SS FF has the same level of radiation hardness as the AC_AS FF. Fig. 34 shows the alpha-induced SERs of DFF, ACFF, AC_SS FF and AC_AS FF. Since the master latch in ACFF keeps a stored value at CLK = 1, ACFF achieves lower SER than DFF. At CLK = 0, however, SER of ACFF is higher than that of DFF or almost equivalent. AC_SS FF and AC_AS do not cause any error at all (DATA, CLK) conditions.

Table 5
Number of transistors and simulation results of area and dynamic power of each FF.

FF	Area	Power	# of Tr.
DFF	1	1	24
Stacked FF	1.12	1.02	28
ACFF	1.00	0.55	22
AC_SS FF	1.12 (1.12)	0.58 (1.05)	26
AC_AS FF	1.24 (1.24)	0.58 (1.07)	30

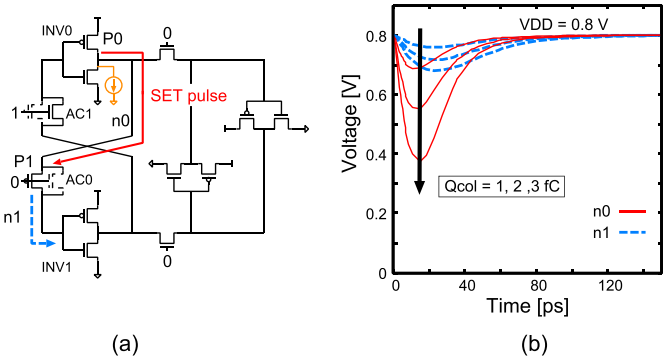

Fig. 33. SET pulse is attenuated after passing through PMOS transistor in AC element. Q_{col} stands for the collected charge.

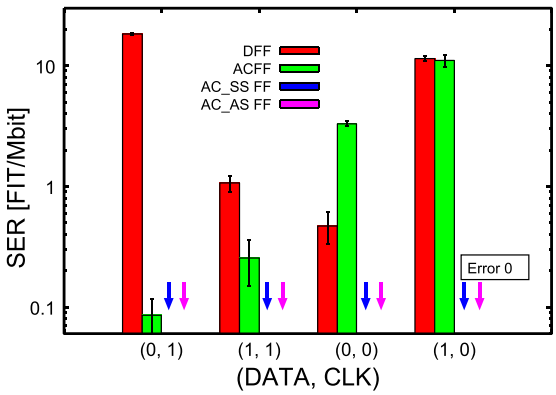

Fig. 34. α-induced SER of DFF, ACFF, AC_SS FF and AC_AS FF at 0.8 V.

5. Simulation

A Monte Carlo simulation is a validating method to SER. Simulations are useful to identify the key ingredients in soft error phenomena because it can output information that cannot be obtained by measurement. Simulations are also helpful to take measures in the design of radiation-tolerant devices because they can predict SERs in the design stage of devices and circuits. There are several Monte Carlo-based simulation tools such as SEMM-2 [62], MRED [63], MC-ORACLE [64], MUSCA SEP3 [65] CORIMS [66], NISES II [67], and so on. We have also developed multi-scale Monte Carlo simulator called PHYSERD (PHits-HYenexx integrated code System for Effects of Radiation on Devices) [33,68]. PHYSERD has been applied to simulate neutron-induced soft errors on bulk NMOSFETs based on event-by-event TCAD simulation that simulates the transient response of devices. Here, we have only focused on NMOSFETs because higher linear energy transfer (LET) is required to cause soft errors by PMOSFET-struck [69], but it should be noted that the PMOSFET-struck soft error can be also analyzed similarly. The physics-based simulation method is powerful and reliable, but it is inappropriate in particular situations because event-by-event TCAD simulation takes long computational time. Therefore, we have also constructed multiple sensitive volume (MSV) model for the NMOSFET [70]. We have simulated neutron-induced soft errors by PHITS + MSV and compared the result by PHITS + MSV with those obtained by PHYSERD to clarify the reproducibility of PHITS + MSV. In this section, we introduce outlines of PHYSERD and MSV model, and show some results of soft error simulation.

5.1. PHYSERD

5.1.1. Simulation method

PHYSERD has been developed by linking a particle transport code PHITS [71] and a 3-D TCAD simulator HyENEXSS (Hyper Environment for Exploration of Semiconductor Simulation) [72–74]. PHITS can deal with the transport of all the particles over wide energy ranges by using several nuclear reaction models and data libraries. Especially for calculating neutron reactions at energies below 20 MeV, PHITS has an original option of “event generator mode (e-mode)” [85–87]. The e-mode can describe secondary ion production based on evaluated nuclear data libraries by taking into account the conservation law of energy and momentum. HyENEXSS can simulate the charge collection process in the 3-D modern device using the drift-diffusion method.

The flow chart of SER analysis by PHYSERD is shown in Fig. 35. First, particle transport and collision in the device are simulated by PHITS. Information about the secondary ions (i.e., the ion species, the kinetic energy, the generation position, and the direction of motion) is stored in “dump file” event by event. Among them, the events

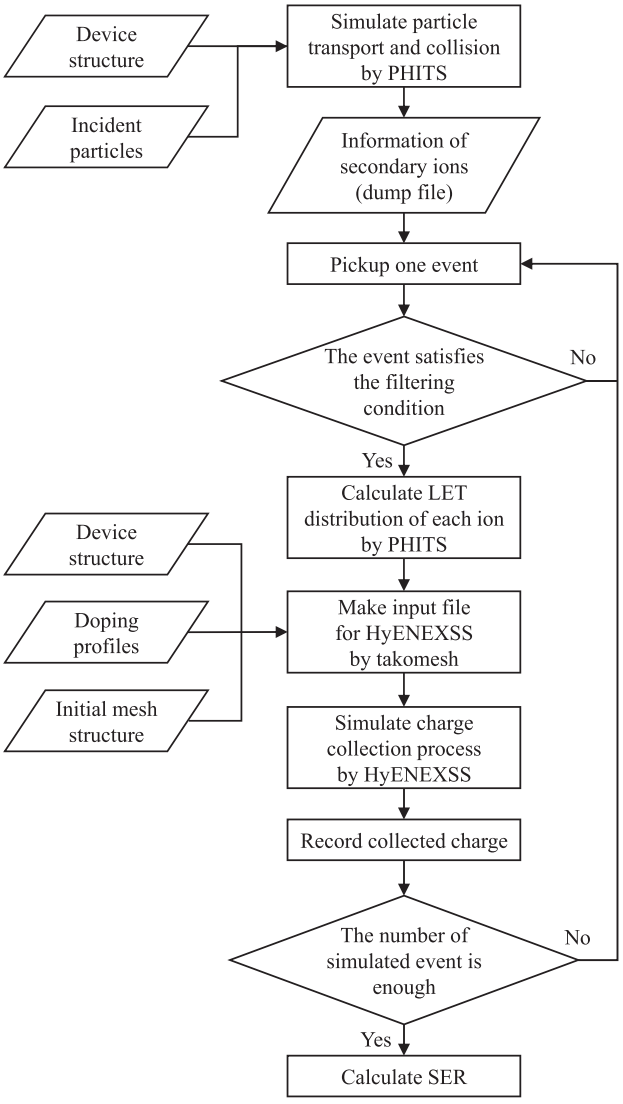

Fig. 35. Flow chart of SER analysis by PHYSERD.

expected to be primarily responsible for the soft errors are selected, and the initial charge distribution along each ion track is calculated by PHITS. An interface tool called “takomesh” [75] makes an input file for HyENEXSS which includes the LET distributions of each secondary ion, the device structure, the doping profiles, and the initial mesh structure. As shown in Fig. 36, takomesh subdivides the mesh along each ion track to optimize the mesh structure for the soft error simulation, where octree mesh method is adopted as a mesh generation algorithm. The charge collection process is simulated by HyENEXSS, and the transient current response and the collected charge are stored for each event.

The number of events, $N(q)dq$, with the collected charge in $[q, q + dq]$ is obtained by performing event-by-event device simulation repeatedly. The SER is calculated as a function of the critical charge Q_{crit} as follows:

$$SER = \frac{F \times A}{N_{in} \times N_{bit}} \int_{Q_{crit}}^{\infty} N(q)dq,$$

where F is the total neutron flux, A is the surface area of the test device, N_{in} is the number of incident neutrons in PHITS calculation, and N_{bit} is the number of bit cells placed in the device.

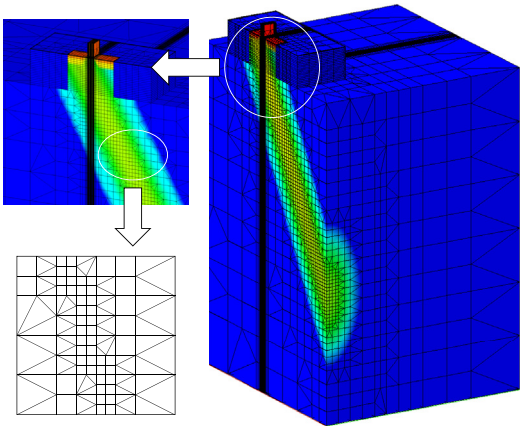

Fig. 36. Mesh structure generated by takomesh. Meshes around ion track are subdivided.

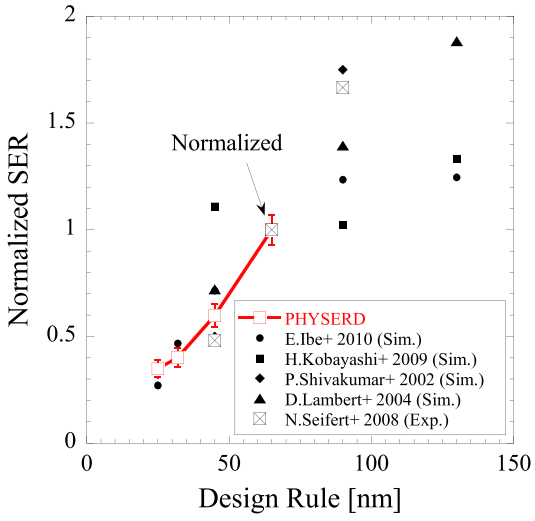

Fig. 37. Scaling trend of calculated SERs. The simulated and measured data are taken from Refs. [31,76–79]. All the SERs are normalized at 65-nm design rule.

5.1.2. Simulation results and discussion

PHYSERD has been applied to simulate terrestrial neutron-induced SERs for 65-nm, 45-nm, 32-nm, and 25-nm bulk technology NMOSFETs [68]. Fig. 37 shows the scaling trend of SER obtained by PHYSERD and other studies [31,76–79]. These data are normalized at 65-nm design rule. The SER by PHYSERD shows a decreasing trend similar to other SERs with a decrease in the design rule, except [76]. The increasing trend observed at 45 nm in Ref. [76] may be due to the small Q_{crit} compared with the other cases.

We have also investigated what secondary ions are major causes of soft errors. Fig. 38 shows contributions of H, He and the other ions to the SER for the 25-nm technology NMOSFET calculated by PHYSERD. At $Q_{crit} = 0.6$ fC, the contribution of He ions amounts to about 70%. When Q_{crit} decreases, H ions replace He ions as the main cause of soft errors. This result indicates that it is important to select a proper nuclear reaction model to estimate production of H and He ions accurately.

5.2. Multiple sensitive volume model

A sensitive volume (SV) model [80] has been commonly employed to estimate the amount of charge collected to the storage node without TCAD simulation. There are two types of SV models. One is the single-SV (SSV) model, which assumes that all the charge deposited in the SV are collected in the storage node. The other is the MSV model [81], which considers the spatial dependence of the charge collection efficiency (CCE). CCE is defined as the ratio of deposited charge to collected charge. The shape, size, and CCE of each SV are determined from LET dependence of SEU cross sections obtained by heavy-ion testing [82] and/or from results of detailed TCAD simulations.

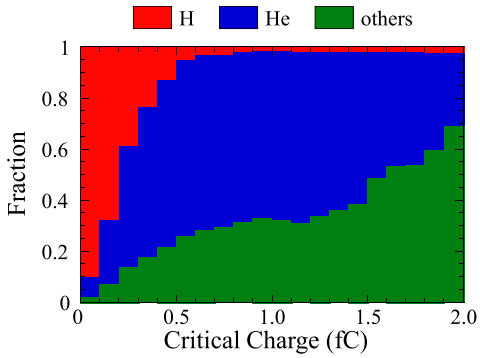

Fig. 38. Contribution of each secondary ion to SER for 25-nm technology NMOSFET.

We have performed a systematic investigation for charge collection process in the 25-nm technology NMOSFET using HyENEXSS to construct the MSV model. The charge collection process is roughly classified into drift process and diffusion process. Therefore, the NMOSFET was first divided into two regions: one where the drift process dominates charge collection and the other where the diffusion process plays the leading part in the charge collection. The drift process and the diffusion process were investigated separately to construct the MSV model.

5.2.1. Systematic investigation for drift process

When an ion strikes the depletion region of NMOSFET, the potential is temporarily distorted, and it enhances charge collection by drift (so-called funneling effect). As an example, Fig. 39 shows the time evolution of electron density, hole density and potential. The funneling affects charge collection till about 40 ps because the distortion of potential disappears at that time. It should be noted that the time when the

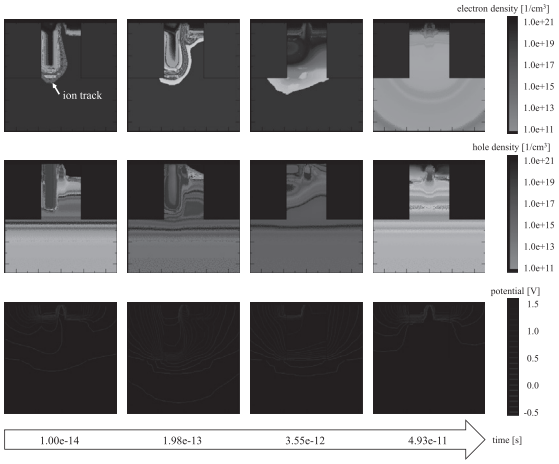

Fig. 39. Time evolution of electron density, hole density and potential for drain-node struck by an ion with a track length of 0.2 μm. The potential is distorted along with the ion track and reverts to normal at 49.3 ps. Electrons are pulled out from the source node to the substrate side at 0.198 ps.

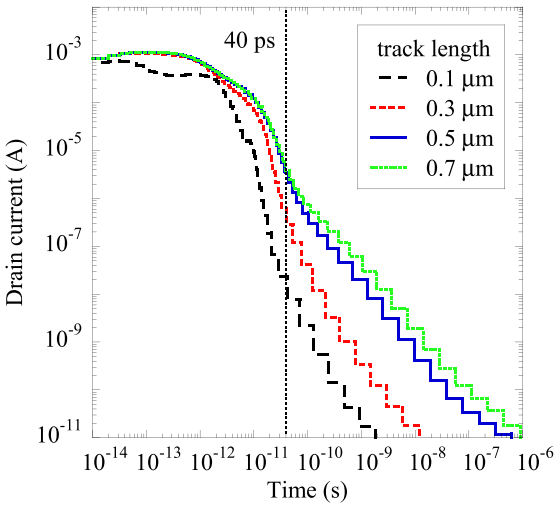

Fig. 40. Drain currents in NMOSFET for each track length.

distortion of potential disappears is almost the same independent of ion-track length. To verify the effective length for charge collection due to funneling, transient analyses were performed for drain-node struck with different ion-track lengths. As shown in Fig. 40, drain currents with an ion-track length exceeding 0.5 μm are almost identical till about 40 ps. Thus, the effective funneling length is set to 0.5 μm.

The CCE mainly due to drift at i-th position, α_i, is defined as the following equation:

$$\alpha_i = \frac{Q_{\mathrm{coll}}(l_i) - Q_{\mathrm{coll}}(l_{i-1})}{Q_{\mathrm{dep}}(l_i) - Q_{\mathrm{dep}}(l_{i-1})},$$

where $Q_{\mathrm{dep}}(l_i)$ and $Q_{\mathrm{coll}}(l_i)$ are the deposited charge and the collected charge into the drain node with an ion-track length of l_i, respectively. Fig. 41 shows the calculated CCEs for drain-node struck, and source-node struck plotted as a function of ion-track length. For drain-node struck, the CCEs with the ion-track length of around 0.1 μm exceed 1.0 because additional electrons are pulled out from the source node and some of them are collected to the drain node, as shown in Fig. 39. This mechanism is called PBA [83], which is already discussed in Section 3 with Fig. 4. The CCE decreases together with extending the length of ion track around 0.18 μm, which is probably because additional deposited

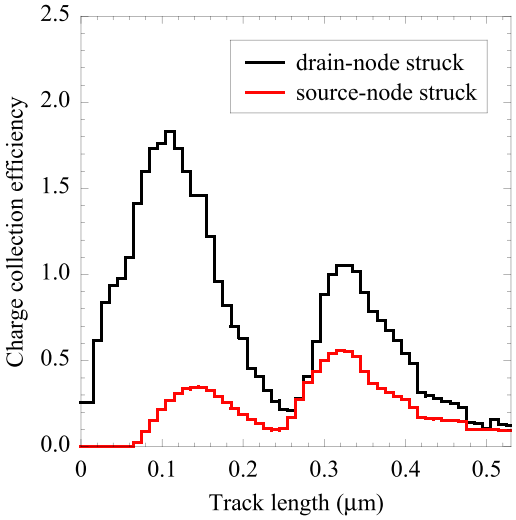

Fig. 41. CCEs for drain-node struck and source-node struck plotted as a function of track length.

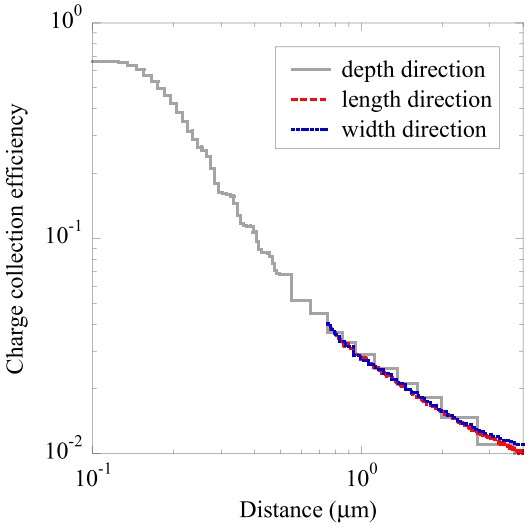

Fig. 42. CCE for several positions of spherical charge plotted as a function of distance between charge and center of transistor surface.

charge impedes the PBA. For source-node struck, CCEs are lower than those for drain-node struck over the whole length because the deposited charge is mostly collected to the source node. Especially below 0.06 μm, CCEs are nearly zero.

5.2.2. *Systematic investigation for diffusion process*

To investigate the CCE mainly due to diffusion, transient analyses with the spherical charge were performed. Here, the CCE is given by the ratio of the collected charge to the deposited charge. The deposited spherical charge was moved in the transistor depth, length and width direction. Fig. 42 shows the CCE plotted as a function of the distance between the spherical charge and the center of the transistor surface. The CCEs below 0.15 μm are almost constant because the deposited charge is near the depletion regions and the charge is collected mainly by drift. After that, the CCE decreases with the distance from the transistor surface. At the distance of 0.75 μm and beyond, the CCEs obtained by moving the charge laterally, i.e., in length and width directions, are almost the same as those obtained by changing the depth. This result indicates that the spatial dependence of the CCE due to diffusion remains almost constant regardless of the direction.

5.2.3. *Construction of MSV*

As described above, the NMOSFET was first divided into region A, where the CCE is mainly due to drift, and region B, where the CCE is mainly due to diffusion. Region A is defined by the active area of the NMOSFET and the effective funneling length, and the rest of the NMOSFET is defined as region B. To keep the difference in CCEs of the two adjacent SVs below 10%, the region A and the region B were subdivided into 148 SVs and 45 SVs, respectively. The CCE in the region A is switched event-by-event depending on whether ions strike in the depletion region of drain or source, which is because the CCE significantly varies as shown in Fig. 41. When an ion strikes both the depletion regions, the average of the CCEs obtained by the drain-node struck and the source-node struck was applied.

The collected charge, Q_{coll}, is approximated by the following equation:

$$Q_{\mathrm{coll}} = \frac{e}{E_{\mathrm{pair}}} \sum_{i=1}^{n} \alpha_i \times E_{\mathrm{dep},i},$$

where α_i is the CCE of the i-th SV, $E_{\mathrm{dep},i}$ is the energy deposited in the i-th SV, e is the elementary charge, and E_{pair} is the mean energy required

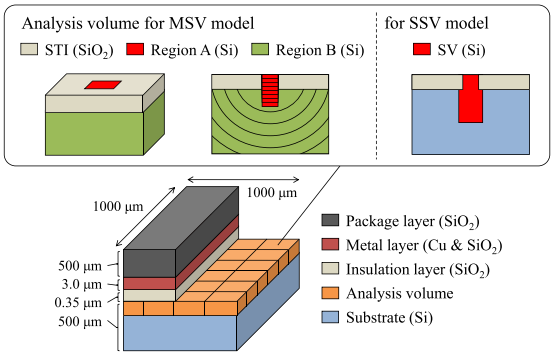

Fig. 43. Configuration of computational system used in PHITS. For the MSV model, the analysis volume is divided into regions A and B, which are then subdivided into smaller SVs. For the SSV model, an SV is placed on the analysis volume.

to generate an electron-hole pair (3.6 eV in silicon). After approximating the collected charge, the SER is calculated with the same process as described above.

5.2.4. Simulation results and discussion

Terrestrial neutron-induced SER for 25-nm technology has been simulated by PHITS + MSV, and the results were compared with those obtained by PHYSERD [68] and PHITS + SSV [84]. Fig. 43 shows the configuration of the computational system used in PHITS. Note that the size and shape of SV used in PHITS + SSV are adjusted to be consistent with the SER obtained by PHYSERD as much as possible. The SERs obtained by each simulation method were shown in Fig. 44. PHITS + MSV reproduces the SER obtained by PHYSERD better than PHITS + SSV over the whole range of critical charge.

To validate the event reproducibility for the two SV models, the relative collected charge (i.e., the ratio of collected charge obtained by using the SV model to that obtained by using PHYSERD) was calculated for each event. Fig. 45 shows the event distribution of the relative collected charge for each SV model. About 90% of events obtained by PHITS + MSV are consistent within 30% of the collected charge estimated by PHYSERD, whereas less than 40% of events obtained by PHITS + SSV are consistent. The result indicates that the SSV model cannot reproduce each event even though the SER matches with that

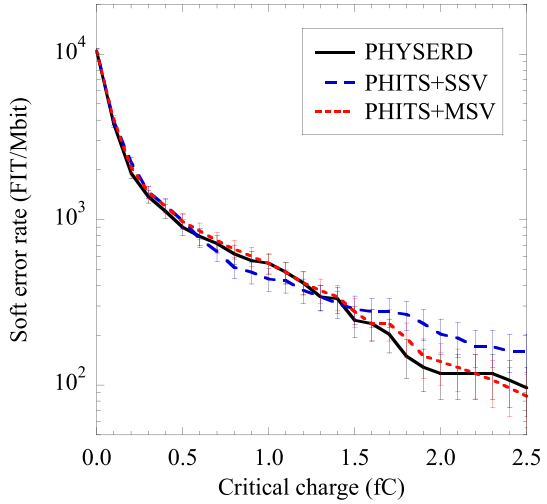

Fig. 44. SERs calculated by PHYSERD, PHITS + SSV and PHITS + MSV.

obtained by PHYSERD. The event reproducibility based on the SV models is improved by considering the spatial dependence of CCE and the position where ions strike.

In this study, the computational time required for SER analysis by PHITS + MSV, including the investigation of CCE, is approximately one-fourth of that by PHYSERD. Moreover, once appropriate CCEs and SVs are prepared for the NMOSFET, PHITS + MSV can estimate the SERs in half the computational time required for the first PHITS + MSV calculation. In conclusion, PHITS + MSV is the most suitable among the methods compared in this study for SER estimation in particular situations such as validating the tolerance of a device in different radiation environments.

6. Future trend

Finally, this section reviews future trends in terms of device structure and potential particles inducing soft errors, and discusses the soft error immunity of FinFETs and muon-induced soft errors.

6.1. FinFET

6.1.1. Single event effects on FinFET

Multi-gate transistors such as FinFET are developed to suppress short channel effects and continue scaling down technology nodes. FinFET typically has double-gate which is wrapped around the channel region, and its structure can lead to better control over the gate and achieve higher performance, less process variations, and lower leakage current. FinFET also has better soft error immunity than planer bulk transistors since thin fin structure reduces the volume of depletion regions and radiation-induced charge collection efficiency is drastically suppressed as shown in Fig. 46. Several researchers report that bulk FinFET processes have 3.5–100× lower soft error rates compared to bulk planer processes [88–90]. On the other hand, unique characteristics are reported since the transistor shapes drastically change from the conventional planar process.

H. Zhang et al. showed that FinFET transistors behave differently from the planar transistors for soft errors since the radiation track length in FinFET decreases when the incident angle increases [91], which corresponds to the horizontal radiation in Fig. 46. B. Narasimham et al. reported alpha-induced SEU cross sections in a 16-nm FinFET D-FF increase exponentially at a low supply voltage and the SEU cross section at low supply voltage is larger than that for a 20-nm planar process at the nominal supply voltage. T. Uemura et al. reported alpha-induced SET and SEU rates in a 10-nm FinFET process. The rate reduction on SET thanks to FinFET is 10× smaller than that on SEU and consequently the importance of SET increases relatively [90]. Here, logic cells consist of a large number of fins, which elevates charge generation probability. Also, shallow isolators between fins also increase charge collection efficiency. P. Nsengiyumva et al. reported heavy-ion-induced SEU cross sections in a 16-nm FinFET [92]. SEU cross section for a FinFET DFF is similar to that for a 22-nm bulk planar DFF at LET values larger than 10 MeV-cm^2/mg.

Soft error rates on FinFET depend on fin structures, and hence soft error rates vary depending on technology nodes, fabrication facilities and circuit design methodologies. Further experimental and simulation results are required to estimate soft error rate in advanced FinFET technologies.

6.1.2. Heavy-ion-induced SEU rates on a 16-nm FinFET BCDMR FF

A test chip in a 16-nm FinFET process was fabricated to measure heavy-ion-induced SEU cross sections for BCDMR FFs [51], which is introduced in Section 4. Accelerated tests were performed at the Berkeley Lab., and the irradiated heavy ions are listed in Table 6. Fig. 47 shows the measured SEU cross sections of the 16-nm FinFET BCDMR FFs, 65-nm bulk planar FFs [57] and 16 nm FinFET FFs [93]. There is

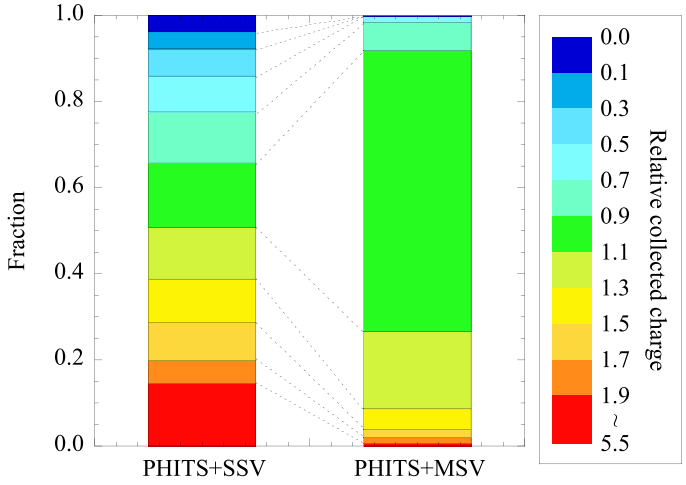

Fig. 45. Event distribution of relative collected charge obtained by each SV model.

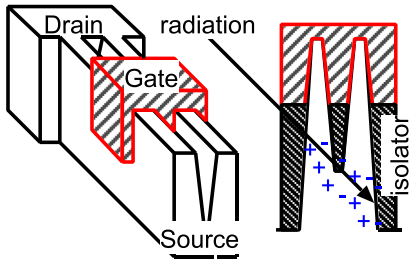

Fig. 46. Cross sectional view of a two-fin bulk FinFET.

Table 6
LET values of heavy ions irradiated at the Berkeley Lab. for 16-nm FinFET. LET is in MeV-cm^2/mg.

Ion	O	Si	Ar	Cu	Kr	Ag
LET	2.19	6.09	9.74	21.2	30.9	46.8

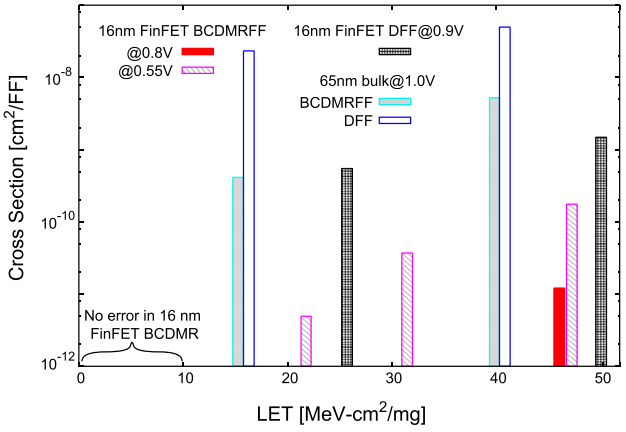

Fig. 47. Heavy-ion-induced SEU cross section with normal incident. 16-nm FinFET DFF results are referred from Ref. [93].

no error in 16-nm FinFET BCDMR FFs when the LET values are less than 9.74 MeV-cm^2/mg. When the supply voltage is 0.8 V, the 16-nm FinFET BCDMR FFs has no error when the LET value is 30.9 MeV-cm^2/mg or less. The cross section in the 16-nm BCDMR FF at 0.8 V by Ag ions (LET = 46.82 MeV-cm^2/mg) is 1/400 smaller than that in the 65-nm BCDMR FF by Kr ions (LET = 40.3 MeV-cm^2/mg). In the 16-nm FinFET process, the critical node distances are reduced compared with 65-nm planar bulk process. However, the 16 nm BCDMR FF achieves better soft error mitigation than the 65-nm BCDMR FF. This result shows that charge sharing can be suppressed by using FinFET structures.

6.2. Muon-induced soft errors

Muons are the most abundant cosmic-ray particles at ground level (*i.e.*, about three-quarters of the total charged-particles) as shown in Fig. 3. The muon is an elementary particle similar to the electron, but the mass of a muon is 105.7 MeV/c^2, which is 207 times larger than the mass of an electron. There are two types of muons, namely, the negative muon (μ^-) and the positive muon (μ^+). Both positive and negative muons are unstable particles with the mean lifetime of 2.2 μs.

Until recently, the effect of muons on microelectronics has been discussed among a few research groups. In the pioneering work of Ziegler and Lanford [94], the occurrence of muon-induced soft errors was predicted for memory devices with extremely low critical charge. Dicello et al. reported on experimental studies of muon and pion induced SEUs and discussed their contribution to the SER at ground level [95–98]. They observed only a few errors during muon irradiation because of insufficient beam intensity and large critical charge of the devices used in the irradiation tests. For a while after these works, the effect of cosmic-ray muons on soft errors had not been considered to be serious because only a small amount of energy is deposited in memory devices due to their small stopping power and the deposited charge cannot exceed the critical charge.

Recently, the cosmic-ray muon induced soft error has received much attention because a reduction in resilience to soft errors has become evident with a decrease in critical charge due to the device miniaturization and low voltage operation of circuits. Sierawski et al. performed a series of positive muon accelerating tests for deep-submicron technologies [21,99,100] and predicted the SERs for different technology nodes (65, 45, 32, 22 and 16 nm) by simulation [99]. The prediction indicated that the muon SER might become significant for 16-nm technology. Following their works, similar SEU experiments with low-energy positive muons were conducted for 28-nm ultra thin body and BOX (UTBB) FDSOI and bulk SRAMs by Gasiot et al. [101] and for 32-nm planar and 22-nm and 14-nm 3D tri-gate technologies by Seifert et al. [102]. The estimated muon SERs for the 14-nm and 22-nm devices, however, were negligible compared to neutron SERs. More

recently, Trippe et al. predicted the positive muon-induced SER for a 28-nm SRAM with ion-calibrated model [103] and reported that the muon SER contributes to less than 2% of the neutron SER in the worst case. It should be noted that the muon-induced SERs were predicted on the basis of the experimental data from irradiation tests of positive muons.

Until now, no negative muon irradiation test with modern devices has been reported. A recent simulation on 65-nm SRAMs by Serre et al. [104] has indicated the importance of the negative muon capture reaction as an additional mechanism of charge deposition for the negative muons stopping in the device. The stopped negative muon is captured by an atom in matter into high orbital momentum states, forming a muonic atom. The captured muon cascades down to the 1*s* orbital while emitting characteristic X-rays. A portion of the captured negative muon decays into an electron and two neutrinos in the 1*s* orbital. The remaining negative muons are finally absorbed by the nucleus, and a highly-excited nucleus is generated. Then, the nucleus is de-excited by the emission of neutrinos, photons, neutrons, and other light ions. When the negative muons stop in silicon, about 65% of them are captured by the nucleus and the remaining muons decay into electrons and neutrinos in the 1*s* orbital. Thus, the capture reaction generates a heavy recoiling nucleus with simultaneous emission of secondary light ions such as protons and α-particles. Since all the secondary ions have much larger stopping power than muons, the secondary ions are expected to deposit sufficient charge in the small sensitive volume of memory devices.

More recently, Manabe et al. [105] and Liao et al. [106] have conducted a series of irradiation experiments with both positive and negative muon beams at the muon science facility (MUSE) [107,108] in Materials and Life Science Experimental Facility (MLF) of the Japan Proton Accelerator Research Complex (J-PARC), to clarify the difference in SEUs induced by positive and negative muons. Two kinds of SRAM chips fabricated in 65-nm CMOS technology were used in the muon irradiation tests, i.e., bulk SRAM and SOTB SRAM. The details of the experimental procedure are reported in Refs. [105,106]. The device board was placed perpendicularly to the propagation direction of the muon beam, which passes through a beam collimator located between the beam exit and the device board. In the experiment, the cross section of SEUs was derived by dividing the number of the observed bit errors by the number of incident muons per unit area.

The experimental results are presented below. First, the measured SEU cross sections for SOTB SRAM with a supply voltage of 0.5 V are shown as a function of incident muon momentum in Fig. 48. Both the negative and positive muon SEU cross sections have the peaks around 38 MeV/c. The range of 38-MeV/c muon in the test device is almost equivalent to the depth to the sensitive volume of SRAM cell, and the maximum charge is deposited in the SV, resulting in a high probability of SEU occurrence. The negative muon SEU cross sections are approximately two to four times larger than the positive muon SEU ones in the peak region, while they are almost the same over 42 MeV/c where most of the muons pass through the device board. In Fig. 48, the solid and dashed lines present a Monte Carlo simulation with PHITS [71] using a simple SV model. The overall behavior of the SEU cross section is generally reproduced well by the PHITS-SV simulation. The detail of the simulation is described in Ref. [105]. In Fig. 49, the pie chart depicted with the simulation result reveals the relative proportion of charged particles and secondary ions to trigger SEUs. Fig. 49 suggests that secondary H and He ions generated from the negative muon capture reaction cause SEUs more seriously than muon direct ionization in the device.

Next, Fig. 50 shows the dependence of measured SEU cross sections on supply voltage for 65-nm bulk SRAM at 38-MeV/c [106]. The negative muon SEU cross section is much larger than the positive muon one, which indicates that negative muons are more likely to induce SEUs in SRAM than positive muons as in the above-mentioned SOTB SRAM. Also, the positive muon SEU cross section increases monotonically with

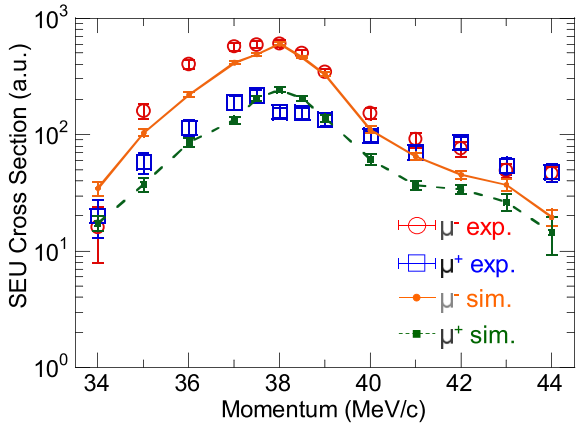

Fig. 48. Measured and simulated SEU cross sections for 65-nm SOTB SRAM as a function of incident muon momentum. ©[2018] IEEE. Reprinted, with permission, from Ref. [105].

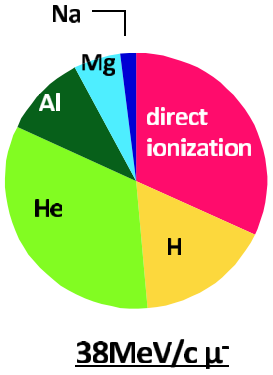

Fig. 49. Relative contribution of muon direct ionization and secondary ions to negative muon SEUs at 38 MeV/c.

a decrease in supply voltage. On the other hand, the negative muon SEU cross section reaches the minimum at 0.5 V, and increases moderately above 0.5 V and approaches to a saturated value. This observation suggests that the SEU mechanism is different between positive and negative muons. Moreover, it is found that negative muon irradiation causes MCUs with high frequency. Fig. 51 shows the observed MCU distributions at 1.2 V and 0.5 V. The ratio of larger-bit MCU event is

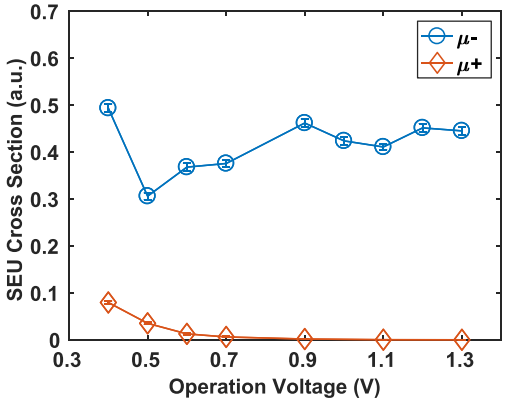

Fig. 50. Dependency of measured SEU cross section on operation voltage under positive and negative muon irradiation with momentum of 38 MeV/c. Zero body bias is given. ©[2018] IEEE. Reprinted, with permission, from Ref. [106].

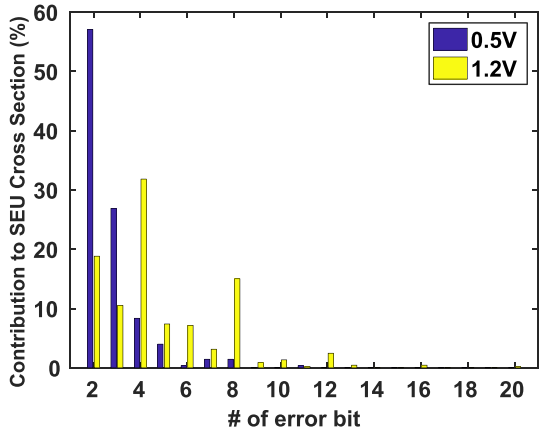

Fig. 51. MCU distributions at 1.2 V and 0.5 V. The data come from 0.5 V to 1.2 V at voltage dependence scanning under negative muon irradiation with 38 MeV/c. Zero body bias is given. ©[2018] IEEE. Reprinted, with permission, from Ref. [106].

smaller at the low voltage of 0.5 V, while large-bit MCUs, such as over 20-bit MCUs, are observed at a high voltage of 1.2 V. It should be noted that only two MCU events at 0.4 V and no MCU events at 0.5 V and above were observed under positive muon irradiation. From the investigation of the mechanism of muon-induced upsets in bulk SRAMs, it was concluded that negative muon induced upsets are caused by PBA in addition to drift and diffusion charge collection [106], which is similar to neutron-induced upsets.

The progress and current status of the studies of muon-induced soft errors are outlined in this section. In the future, further irradiation tests and simulations should be conducted for finer SRAMs than 65 nm to investigate the scaling effect on negative muon-induced SEUs and MCUs in advanced devices. Reliable estimation of muon SERs on the ground will require not only the experimental irradiation data and improved SEU simulation but also the actual measurement of cosmic-ray muons in the places where computers and electric devices are used. There is no experimental flux data of low-energy muons (e.g., below 10 MeV) which are expected to cause upsets with high probability in memory devices. Therefore, the flux measurement is required for accurate estimation of muon-induced SER.

7. Conclusion

This paper discussed soft errors occurring in SRAMs and flip-flops in bulk, FDSOI, and FinFET technologies. Technology scaling raises the risk of multiple upsets since sensitive nodes tend to be located in a smaller area and circuits operate at a lower supply voltage. On the other hand, recent transistor devices developed for mitigating short channel effects, such as FDSOI and FinFET, unintentionally have preferable characteristics for soft error mitigation. Leading edge products using such advanced fabrication technologies take advantage of these devices to satisfy the given error rate requirement. On the other hand, cost-effective products, such as IoT devices, will continue to use bulk devices. In this case, we need to pay attention to and avoid drastic error rate elevation caused by secondary protons. As SRAM SER decreases thanks to error countermeasures, FF SER determines the VLSI system reliability. To attain severe reliability requirements while keeping the performance overhead minimized, transistor-level redundant FFs play an important role in critical applications like autonomous driving. Our lives and properties are more and more dependent on electronic devices, and then we need to keep the project of soft error rate on future technologies, study error mechanism in future novel devices and develop countermeasures for more intelligent society in the future with both measurement and simulation.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.vlsi.2019.03.005.

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