Estimation of Muon-Induced SEU Rates for 65-nm Bulk and UTBB-SOI SRAMs

Seiya Manabe, Yukinobu Watanabe, Wang Liao, Masanori Hashimoto, and Shin-ichiro Abe

***Abstract*— Negative and positive muon-induced single-event upset (SEU) rates were estimated for 65-nm bulk and ultrathin body and thin buried oxide silicon-on-insulator (UTBB-SOI) static random access memories (SRAMs). The SEU cross sections for muon incidence on the two SRAMs were experimentally characterized and compared. The experimental results showed that the negative muon SEU cross sections for the bulk SRAM are significantly larger than those for the UTBB-SOI. Estimation of muon SEU rates at ground level was performed using the experimental results and the Monte Carlo simulation with the Particle and Heavy Ion Transport code System (PHITS). The estimated muon SEU rates were compared with the measured neutron SEU rates. The contribution of muons was found to be considerably smaller than that of neutrons. Attenuation effect of muons and neutrons in a five-story building was also investigated by particle transport simulation with PHITS. The muon SEU rate on the first floor was estimated to be at most 10% of the neutron SEU rate on the same floor.**

***Index Terms*— 65-nm bulk and silicon on a thin buried oxide (SOTB) SRAM, negative and positive muons, Particle and Heavy Ion Transport code System (PHITS), single event upset (SEU), SEU rate prediction.**

I. Introduction

COSMIC ray-induced soft errors have been recognized as a major threat for electronics used at ground level. So far, cosmic-ray neutrons have been considered as a major cause of soft errors in a terrestrial radiation environment. Recently, cosmic-ray muon-induced soft errors have received much attention due to the reduction of soft error immunity on static random access memories (SRAMs). To investigate the effect of cosmic-ray muons, a series of positive muon accelerating tests was performed for deep-submicrometer technologies by Sierawski *et al.* [1]–[3]. Furthermore, soft error rates (SERs) for different technology nodes (65, 45, 32, 22, and 16 nm) were predicted by simulation [2]. The prediction indicated that muon SER might become significant for 16-nm technology node. To test this prediction, Seifert *et al.* [4] conducted the experiment with positive muon beam for 32-nm planar and 22- and 14-nm 3-D trigate technologies. The estimated muon SERs for the 14- and 22-nm devices, however, were negligible compared to neutron SERs. Also, Gasiot *et al.* [5] reported the positive muon SERs for 28-nm ultrathin body and thin buried oxide (UTBB) FD-silicon-on-insulator (SOI) and bulk SRAMs with the measured error cross sections. However, the computed positive muon SERs are below 0.1 FIT/Mbit. Recently, Trippe *et al.* [6] predicted the muon-induced SER for a 28-nm SRAM with their ion-calibrated model. The model reproduced the experimental positive muon single-event upset (SEU) results well and was used to muon SER prediction. The result showed that the muon SEU rate contributes to less than 2% of the neutron SER in the worst case. In these past works, the muon-induced SERs were estimated by using the experimental data for the positive muon irradiation.

The recent simulation on 65-nm bulk SRAM by Serre *et al.* [7] showed that residual heavy nuclei and light particles generated by negative muon capture reactions cause SEUs significantly if the negative muons are stopped near the sensitive drain region and captured by constituent elements. To demonstrate this simulation result, we recently performed the negative and positive muon irradiations on the 65-nm bulk and UTBB-SOI SRAMs, which were fabricated in 65-nm complementary MOS technology with a deep well option [8], [9]. The experimental results clearly showed the effects of negative muon capture reactions on the occurrence of SEUs when negative muons stop near the sensitive volumes (SVs) of SRAMs. Moreover, it was found that negative muons frequently cause multiple cell upsets (MCUs) in the bulk device and the fraction of MCUs in total SEUs increases at a higher operation voltage due to the parasitic bipolar action (PBA) [9].

As mentioned above, muon SERs for various technology devices were predicted with only the positive muon irradiation tests and simulation. The experimental SEU data with negative muons were successfully measured in [8] and [9]. In this paper, the muon SEU rates for the 65-nm bulk and UTBB-SOI SRAMs are estimated by using the experimental data of both negative and positive muons. The SEU rates are calculated with a method of combining a simple SV model [10] and Monte Carlo simulation with the Particle and Heavy Ion Transport code System (PHITS) [11]. The experimental data are used for the calibration of the calculated SEU rates. The estimated muon-induced SEU rates are compared to the neutron SEU rates measured with the white neutron beam [12]

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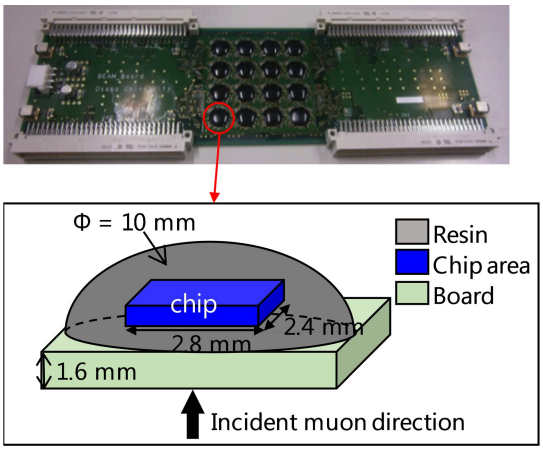

Fig. 1. Structure of device board. Sixteen chips are bonded on the board. The thickness of tested chips is approximately 0.3 mm.

in order to investigate the fraction of the muon SEU rates to the neutron SEU rates.

Next, muon transport simulation in a five-story building is performed to predict the muon SEU rates under more realistic environment and the muon flux on each floor is estimated. Then, the muon SEU rate on the first floor is predicted and the change in the ratio of the muon SEU rate to the neutron SEU rate is discussed in terms of flux attenuation in the building.

The rest of this paper is organized as follows. First, we briefly describe the test setup with the negative and positive muons in Section II. Next, the comparison of the experimental data for the bulk and UTBB-SOI SRAMs is reported in Section III. Then, a method of predicting SEU rates in the open air and the building is described and the results are presented in Section IV. The predicted muon SEU rates are compared with the measured neutron SEU rates for the same device reported in [12] in order to clarify the contribution of muons to the overall SEU rates. Finally, conclusions are given in Section V.

II. Experiment

A. Experimental Setup

The accelerated test with both the negative and positive muons was performed using the D2 experimental area at J-PARC Muon Facility, MUSE [13], [14]. The details of the experimental setup are described in [8] and [9]. Two types of SRAM chips, i.e., bulk and silicon on a thin buried oxide (SOTB) that is one of UTBB-SOIs, were tested in the experiment. Fig. 1 shows the structure of the tested device board. The tested device board is composed of 16 chips and each chip has 12-Mbit memories. The 12 chips on a single device board, namely, 144-Mbit memories were tested at the same time, while the remaining four chips were not irradiated in order to see the influence of background radiation in the environment. The remaining four chips were not irradiated by the muon beam in order to see the influence of background radiation in the environment. The muon beam was irradiated from the board side perpendicularly placed to the beam. The tested chips were bonded on the 1.6-mm-thick board. The structure of the tested device board, bulk, and SOTB, is the same except the transistor volume. Also, the bulk and SOTB device boards were placed at 340 mm from the beam exit. Hence, the ranges of incident muons in the transistor in two types of chip were the same. In addition, the J-PARC accelerator was operated with the average power of 150 kW during the tests of the two boards. Thus, the bulk and SOTB SRAMs were tested under the same muon beam condition.

The operation procedure of SRAM chips during the test is described in [9]. First, the supply voltage was set to be 1.2 V for write operation, and all SRAM memories were initialized by writing the data of "0." Then, the supply voltage was changed to an operating voltage and the memories were in hold operation during the beam irradiation. After that, the voltage was set back to be 1.2 V for read operation and the number of upsets was counted. In this way, the data in each memory bit were read and written at enough high supply voltage of 1.2 V to avoid failures in the read and write operations. The muon beam was irradiated on SRAMs during the period of voltage transition, but the transition time was less than 3% of the holding time. Since the SEU events in the transition time were negligible, the present irradiation test can be regarded as a static test.

B. Measured SEU Cross Section

We have obtained the experimental SEU cross sections as a function of muon kinetic energy. Note that the measured SEU cross section was given in arbitrary units as a function of muon momentum in the previous works [8], [9]. Since the muon beam in the MUSE had the momentum distribution, which can be approximated as a normal distribution with a 5% standard deviation, the experimental SEU cross section is defined by the following expression:

$$\langle \sigma_{\mathrm{SEU}}(E_{\mathrm{mean}}) \rangle = \frac{\int_0^\infty \sigma_{\mathrm{SEU}}(E).\phi(E, E_{\mathrm{mean}})dE}{\int_0^\infty \phi(E, E_{\mathrm{mean}})dE}, \quad (1)$$

where $\langle \sigma_{\mathrm{SEU}}(E_{\mathrm{mean}}) \rangle$ represents the mean SEU cross section with the muon beam in the MUSE, which has the momentum distribution with the mean kinetic energy E_{mean}, $\sigma_{\mathrm{SEU}}(E)$ is the monoenergetic muon SEU cross section at the kinetic energy E and $\phi(E, E_{\mathrm{mean}})$ is the fluence of incident muons with the kinetic energy E in the case of irradiation of the muon beam with the mean kinetic energy E_{mean}.

III. Experimental Results and Discussion

Irradiation tests with both negative and positive muons were performed in the kinetic energy range from 5.3 to 8.8 MeV. The incident kinetic energy and operating supply voltage dependence of SEU cross sections were investigated for the bulk and SOTB SRAMs in [8] and [9]. The observed operation voltage dependences for the two SRAMs by 6.6-MeV positive and negative muon irradiations are shown in Fig. 2(a) and (b), respectively.

The positive muon SEU cross sections for the bulk SRAM are approximately two to four times larger than those for the SOTB SRAM, except at 1.1 V where the statistics is poor.

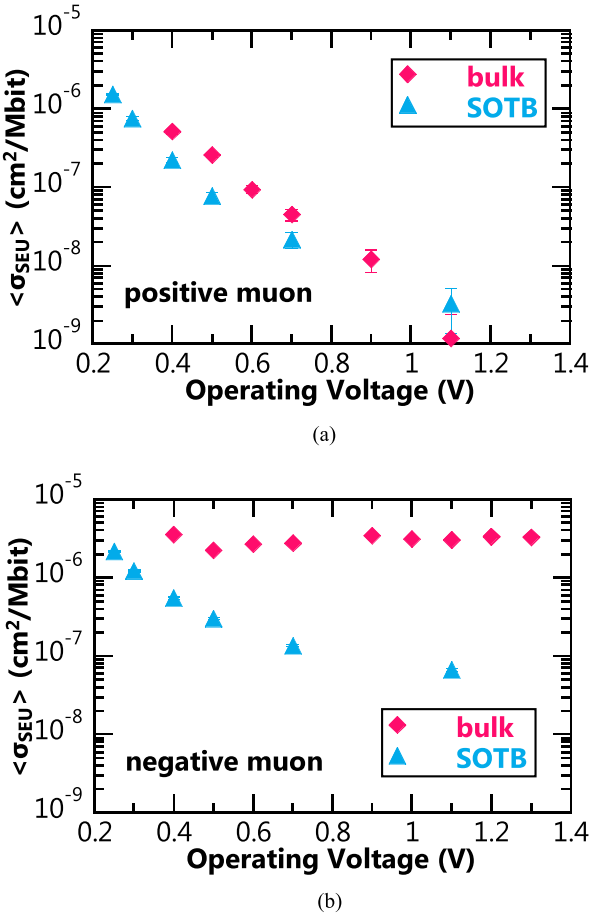

Fig. 2. Measured SEU cross sections for 65-nm bulk and SOTB SRAMs under 6.6-MeV (a) positive and (b) negative muon irradiations.

The positive muon SEU cross sections for both the bulk and SOTB SRAMs decrease similarly and monotonically with increasing supply voltage. On the other hand, the negative muon SEU cross section for the SOTB SRAM decreases more gradually compared to the positive muon one with increasing supply voltage. Moreover, the negative muon SEU cross section for the bulk SRAM reaches the minimum at 0.5 V and increases to a saturated value above 0.5 V because of a significant increase in MCU cross section due to PBA effects [9]. The PBA-induced MCU is caused by large charge deposited to the transistor volume of the bulk SRAM. The simulation in [9] clarified that negative muons can deposit sufficient charge (above 5 fC) to cause PBA due to the secondary ions emitted from the negative muon capture reaction. In addition, it was verified that direct ionization of muons cannot cause PBA because of lower stopping power than that of the secondary ions. Note that PBA does not occur in the SOTB SRAM. Under the negative muon irradiation, therefore, the SEU cross section for the bulk SRAM is at least 6.5X larger than those for SOTB SRAM shown in Fig. 2(b). Thus, our previous experiment demonstrated that negative muons have larger impact on the occurrence of SEU compared to positive muons, especially in the bulk SRAM. To investigate the impact of negative muons on SERs on the ground level, negative and positive muon-induced SEU rates under terrestrial radiation environment are calculated in Section IV.

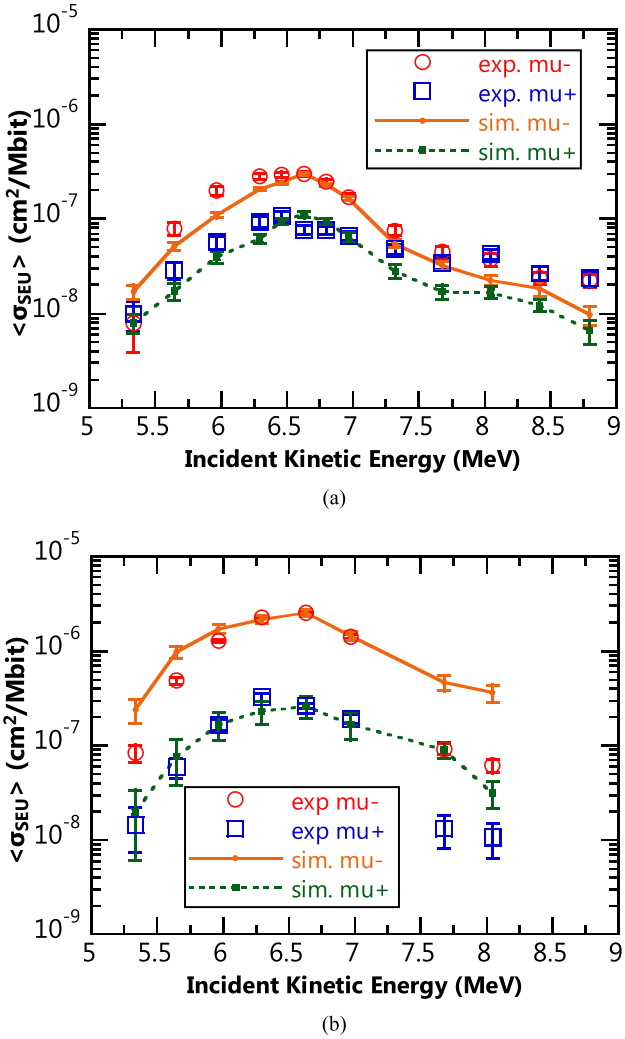

Fig. 3. Comparison between the measured SEU cross sections and the simulated ones for the 65-nm SOTB SRAM as a function of the incident kinetic energy. The operating supply voltage is 0.5 V and the critical charge used in the simulation is 0.08 and 1.5 fC for (a) SOTB and (b) bulk SRAM, respectively.

IV. SEU Rate Estimation

A. Method

To predict the SEU cross sections, we proposed a method of combining a simple SV model and Monte Carlo simulation with the PHITS ver 2.95 [11] in the previous work [8], which will be hereafter referred to as the PHITS-SV method. The SV of each SRAM cell was defined to the active volume of the OFF-state nMOS and pMOS as described in [8] and [9]. The same sensitive area for both the SOTB and bulk SRAMs was given, namely, 0.34 μm $\times$ 0.08 μm for nMOS and 0.26 μm $\times$ 0.12 μm for pMOS. The SV depth was 0.012 and 0.4 μm for the SOTB and bulk SRAMs, respectively. The same momentum distribution of incident muons as in the measurement was used for comparison with the measured mean SEU cross section given by (1).

Fig. 3 shows the comparisons of the simulated mean SEU cross sections and the measured ones as a function of incident kinetic energy for the SOTB and bulk SRAMs. The critical charge Q_c that is an adjustable parameter in the PHITS-SV method was chosen so as to reproduce the ratio of the negative

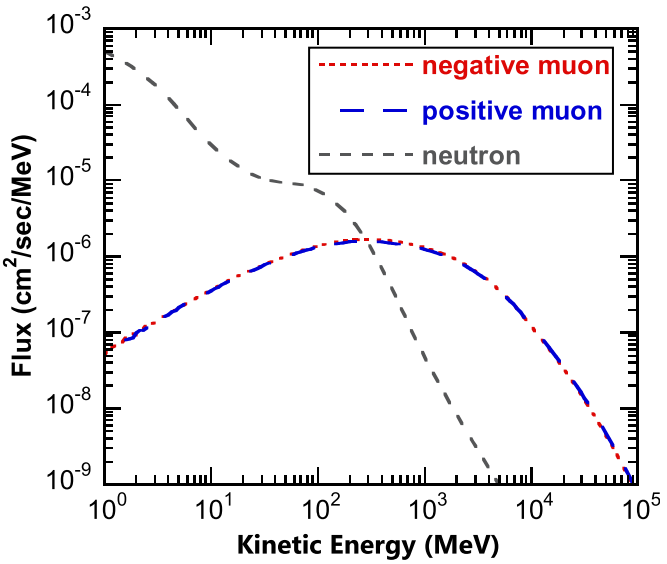

Fig. 4. Open-air omnidirectional energy spectrum of neutrons and negative and positive muons at sea level in Tokyo, Japan, which was calculated by the PARMA model [15], [16].

and positive muon-induced SEU cross sections measured at 6.6 MeV. As a result, the Q_c value was 0.08 and 1.5 fC at the operating supply voltage of 0.5 V for SOTB and bulk SRAMs, respectively. By normalizing the simulated mean SEU cross section to the measured one at 6.6 MeV, the overall behavior of the measured SEU cross section was reproduced well by the simulation as shown in Fig. 3. It should be noted that the normalization factor is used in the estimation of the SEU rates at ground level as mentioned below.

The PHITS-SV method can also be applied to estimate the negative and positive muon SEU rates for 65-nm bulk and SOTB SRAM at ground level. To calculate the muon SEU rate at ground level, the PHITS-SV simulation was performed by the following procedure. First, the muon energy spectrum at ground level is obtained by the PHITS-based analytical radiation model in the atmosphere (PARMA) model [15], [16]. Fig. 4 shows the calculated omnidirectional energy spectra of muons and neutrons in Tokyo, Japan. Next, muons with the PARMA energy spectrum are vertically injected on the 65-nm SRAM chip. The number of upset events, $N(q)dq$, with the charge deposited in the SV in $[q, q+dq]$ is obtained. The SEU rate is calculated as a function of operating supply voltage V_{op} by choosing Q_c as follows:

$$\mathrm{SEUrate}(V_{\mathrm{op}}) = C_{\mathrm{nor}} \times \frac{F \times A}{N_{\mathrm{in}} \times N_{\mathrm{bit}}} \int_{Q_c(V_{\mathrm{op}})}^{\infty} N(q)dq \quad (2)$$

where F is the total flux of incident muons in units of cm^{-2} sec^{-1}, A is the surface area of the test board, N_{in} is the number of the incident muons, N_{bit} is the number of bit cells in the device, and C_{nor} is the normalization factor given by the ratio of the mean negative muon SEU cross section to the simulated one at the incident kinetic energy of 6.6 MeV.

B. Open-Air SEU Rate

The estimated muon SEU rates for the SOTB and bulk SRAMs are compared to the measured neutron SEU rates

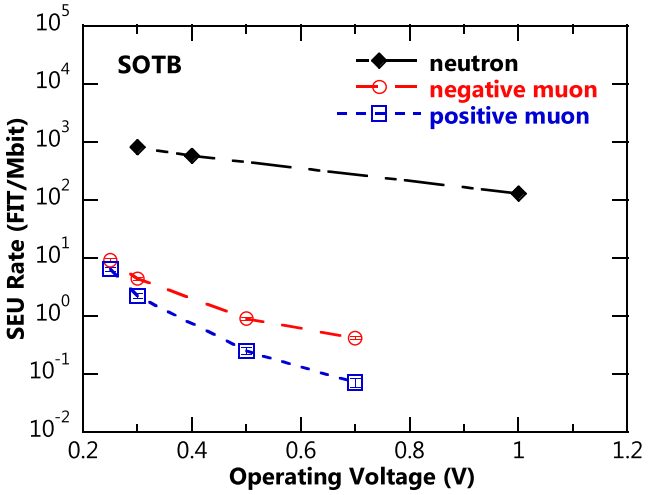

Fig. 5. Ground-level SEU rate induced by cosmic-ray neutron, negative muon, and positive muon on the 65-nm SOTB SRAM.

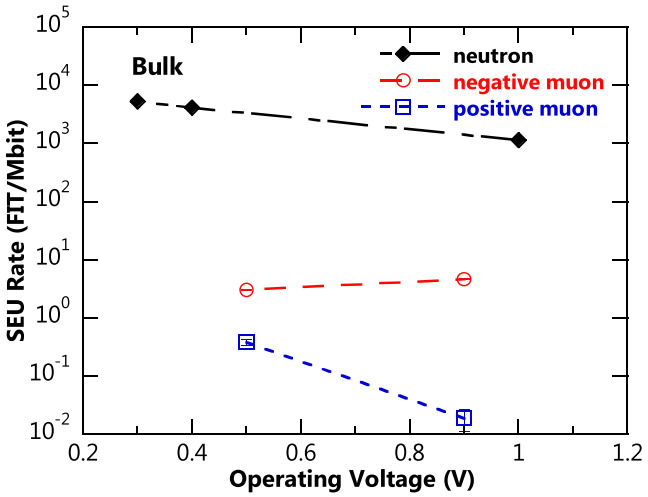

Fig. 6. Ground-level SEU rate induced by cosmic-ray neutron, negative muon, and positive muon on the 65-nm bulk SRAM.

in Figs. 5 and 6, respectively. The neutron SEU rates were measured using a white neutron beam at the Research Center for Nuclear Physics (RCNP) in Osaka University. The details of the measurement are described in [12].

First, we evaluate the negative and positive muon SEU rates for the two SRAMs. The negative muon SEU rates are larger than the positive muon SEU rates because of larger SEU cross sections due to the negative muon capture process shown in Figs. 5 and 6. The ratios of negative muon SEU rates for the SOTB SRAM to positive muon SEU rates are 3.6X and 5.8X at 0.5- and 0.7-V operating supply voltage, respectively. The charge deposited by the secondary ions generated from the negative muon capture is much larger than that deposited by muon direct ionization. Thus, negative muons can deposit sufficient charge to cause SEUs even at higher operation voltage (i.e., at larger critical charge). Hence, the difference between negative and positive muon SEU rates becomes larger for operation with higher voltage. This result indicates that careful consideration of negative muon capture reactions plays an important role in estimating muon SEU rates properly

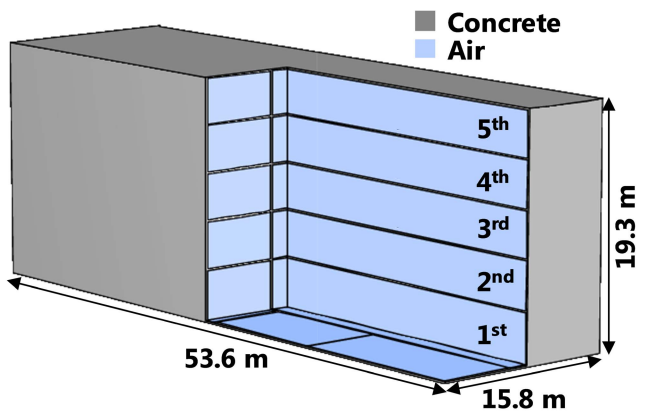

Fig. 7. Simulation structure of five-story building made of concrete and room air.

and accurately. In lower operating voltages of 0.3 and 0.25 V, however, both the SEU rates are almost the same because the direct ionization of muons causes SEUs mainly in the low critical charge. On the other hand, in the case of bulk SRAM, the negative muon SEU rates are approximately 8X and 247X larger the positive muon SEU rates at the operating voltages of 0.5 and 0.9 V, respectively. The reason for this significant difference between the bulk and SOTB SRAMs can be explained straightforwardly by the difference in the supply voltage dependence of negative and positive muon SEU cross sections as shown in Fig. 2. Consequently, the present result indicates that the impact of negative muon capture reaction for the bulk SRAM is much more significant than that for the SOTB SRAM.

Next, the estimated muon SEU rates are compared to the neutron SEU rates shown in Figs. 5 and 6. The PHITS-SV method can also be applied to the estimation of neutron SEU rates. For further validation of the method, the neutron SEU rate was calculated for the bulk SRAM using the same values of Q_c and C_{nor} as in the estimation of the muon SEU rate. As a result, the calculated neutron SEU rate underestimated the experimental one by a factor of about two. However, this is not serious in comparison between the neutron and muon SEU rates shown in Figs. 5 and 6, because the difference between them is significantly large. The muon SEU rate for the SOTB SRAM has the highest contribution at the operating voltage of 0.3 V among those estimated in this paper. Even in this case, we have found that the contribution from muons is approximately 1%.

C. Indoor Muon SEU Rate

In order to evaluate the muon SEU rates in a realistic radiation environment where SRAM devices are operated, we have made muon transport simulation in a five-story building by using PHITS. Fig. 7 shows the structure of the building made of concrete and room air, which is the same as in [17]. The thicknesses of the floor and wall are 15 and 20 cm, respectively. The height of the building is 19.3 m, and the width and the length are 53.6 and 15.8 m, respectively. The building is irradiated by muons having the energy and zenith angular distributions on the ground given by PARAMA model.

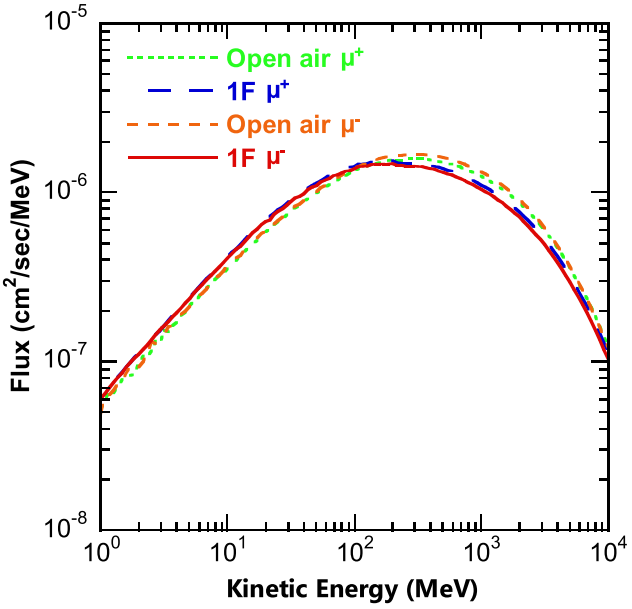

Fig. 8. Comparison of the calculated negative and positive muon energy spectra on the first floor and in the open air.

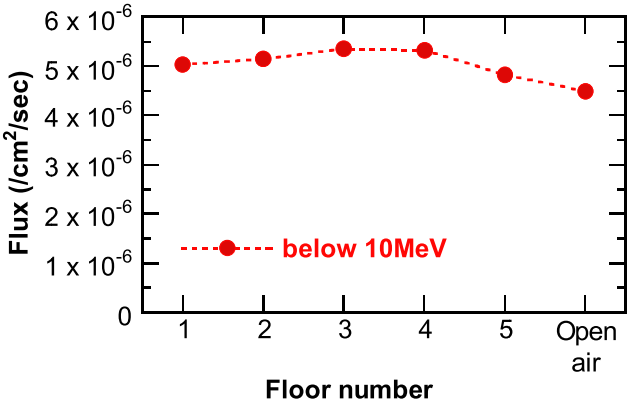

Fig. 9. Calculated muon fluxes below 10 MeV on each floor and in the open air.

The fluxes of negative and positive muons on each floor are calculated.

The calculated energy spectrum on the first floor is compared to that in the open air shown in Fig. 8. The flux on the first floor above 100 MeV is lower than that in the open air due to the energy loss in the building. Hence, the flux on first floor less than 100 MeV slightly increases compared to that in the open air. Our previous experimental result indicated that the SEU cross section for the device board has a peak around the incident kinetic energy of 6.6 MeV as shown in Fig. 3. Thus, the muon flux below 10 MeV is crucially important on the occurrence of SEUs. Fig. 9 shows the muon fluxes below 10 MeV on each floor and in the open air. The fluxes in the building are larger than the open-air flux and the floor dependence is found to be weak. Although the maximum flux value is given on the third floor, the difference from the open-air flux value is less than about 20%. The simulation result indicates that it is difficult to reduce the low-energy muon flux by shielding materials because the high-energy

muons slow down to low-energy region due to the energy loss in shielding materials. As a result, the muon SEU rate is almost constant regardless of the floor number. On the other hand, the previous simulation [17] presented that the neutron SEU rate on the first floor decreases to 13% of that in the open air. Based on the prediction [17], we conclude that the muon SEU rate on the first floor is at most 10% of the neutron SEU rate for the 65-nm SOTB SRAM with the operating voltage of 0.3 V at which the muon has the highest contribution among the estimated SEU rates as shown in Fig. 5.

V. Conclusion

The negative and positive muon-induced SEU rates for the 65-nm bulk and SOTB SRAMs in terrestrial radiation environment were estimated using the PHITS-SV simulation based on the experimental SEU cross sections. The measured negative and positive muon SEU cross sections for the bulk and SOTB SRAMs were compared and the observed differences between positive and negative muons were discussed.

The experimental results indicated that negative muons have the significantly larger impact on the occurrence of SEU in the bulk SRAM than that in the SOTB SRAM due to PBAs induced by secondary ions generated from the negative muon capture reaction. For the two SRAMs, the negative muon SEU rates are found to be larger than the positive muon SEU rates. It should be emphasized that the negative muon SEU rate was 247X larger than the positive muon SEU rate for the 0.9-V bulk SRAM. Hence, it is important to consider the effect of negative muons on SEU appropriately for the accurate prediction of muon-induced SERs. In addition, the estimated muon SEU rate was compared to the measured neutron SEU rate. As a result, it is concluded that the muon SEU rates for 65-nm technology devices are almost negligibly small compared to the neutron SEU rates even if the contribution from negative muons is considered. This result is generally consistent with other predictions by the previous works [2], [4]–[6].

In addition, the muon transport simulation in a five-story building was performed to evaluate the muon SEU rates in a realistic radiation environment. The result showed that the indoor muon flux below 10 MeV is almost constant regardless of the floor number. On the other hand, the simulation in [17] demonstrated that the neutron SEU rate on the first floor is 13% of the open-air SEU rate. Consequently, the muon SEU rate was estimated to be at most 10% of the neutron SEU rate on the first floor.

In the future, further experiments and simulations with smaller technology SRAMs will be required to investigate the effect of scaling on negative muon-induced SEUs and MCUs. Moreover, actual measurements of low-energy muon flux in the building will be necessary for reliable SER prediction.

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