Similarity Analysis on Neutron- and Negative Muon-Induced MCUs in 65-nm Bulk SRAM

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***Abstract*— Multiple-cell upset (MCU) in static random access memory (SRAM) is a major concern in radiation effects on very large scale integration (VLSI) since it can spoil error correcting codes (ECCs). Neutron-induced MCUs have been characterized for terrestrial environment. On the other hand, negative muon-induced MCUs, which are caused by secondary ions generated through muon capture process, were recently reported. Neutron- and negative muon-induced MCUs are both caused by secondary ions, and hence, they are expected to have some similarity. In this paper, we compare negative muon- and neutron-induced MCUs in 65-nm bulk SRAMs at the irradiation experiments using spallation and quasi-monoenergetic neutrons and monoenergetic negative muons. The measurement results show that the dependencies of MCU event cross section on operating voltage are almost identical. The high operating voltage makes both negative muon- and neutron-induced MCU cross sections larger due to parasitic bipolar action. Consequently, large-bit MCUs are observed under the irradiation using both neutrons and muons. On the other hand, at 0.4 V, neutrons induce larger-bit MCUs (> 12 bits) whereas negative muons cause up to 11-bit MCUs. Upsets of 3 or larger bits along word line (WL) are observed at spallation neutron beams. To explain the similarity of MCUs induced by neutrons and negative muons, the Monte Carlo simulation is conducted to investigate the deposited charge. The distributions of deposited charge obtained by the simulation are consistent with the above-mentioned experimental observations.**

***Index Terms*— Multiple-cell upset (MCU), negative muons, neutrons, single-event upset (SEU), static random access memory (SRAMs).**

I. Introduction

SOFT errors jeopardize the reliability of semiconductor devices. In the terrestrial environment, the dominant cause of soft errors has been considered as neutrons [1]. However, muon-induced soft errors are observed in submicrometer devices through experiments [2]–[6] and simulations [4]–[8]. In particular, negative muons are recently reported to have larger single event upset (SEU) cross section compared to positive muon due to muon capture reaction [7] and cause large-bit multiple-cell upsets (MCUs).

There are several reports on comparisons of SEU cross sections. Seifert *et al.* [4] show static random access memory (SRAM) SEU cross sections of spallation neutrons and monoenergetic positive muons for 32-, 22-, and 14-nm technology, and Trippe *et al.* [6] report cross sections for 28-nm technology. For the comparisons of the soft error rate (SER) under terrestrial cosmic ray, Infantino *et al.* [9] and Li Cavoli *et al.* [10] conducted the simulations and reported that the muon-induced SER has the possibility of exceeding the neutron-induced one at near 20-nm technology node. For this, MCU is a more serious concern since it can spoil the error correcting codes (ECCs). However, the characteristics of the muon-induced MCUs have not been compared to those of neutron-induced MCUs.

In this paper, we compare the characteristics of MCUs measured at the irradiation experiments using spallation neutrons, quasi-monoenergetic neutrons, and monoenergetic negative muons. The same 65-nm bulk SRAM chips were tested in the above-mentioned measurements. Our comparison results show that the negative muon-induced MCU has a strong similarity to neutron-induced MCU: the voltage dependency of the MCU cross section is almost identical, and both muons and neutrons can induce large-bit MCU. However, a detailed examination shows that neutrons induce larger-bit MCUs than negative muons, and this tendency is clearer at a low operating voltage. Finally, the Monte Carlo simulation is conducted to investigate the amount of charges deposited by negative muons and neutrons. The simulation results show the consistency with our experimental observations.

II. Experimental Setups

The same 65-nm bulk SRAM chips were tested at the irradiation experiments using neutron and muon beams. Fig. 1 shows the structure of the tested chips, each of which contains 12-Mbit memory cells of 6T design. The chips were designed with SRAM design rules and fabricated in 65-nm technology with eight metal layers and deep N-well option.

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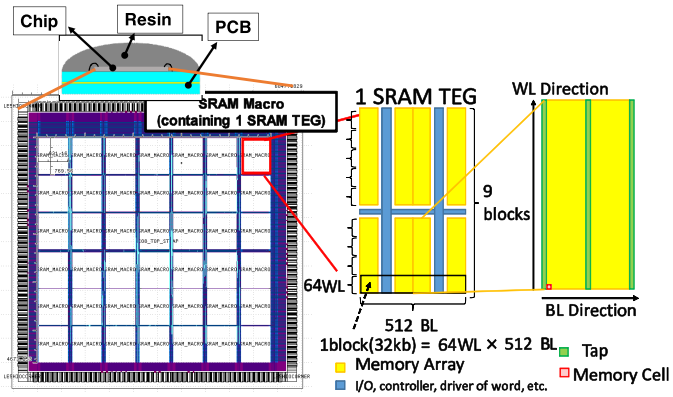

Fig. 1. Structure of SRAM chip under test. For each chip, there are 42 SRAM TEGs. Each TEG contains a 32-kbit SRAM macro. Bit cell distribution in the macro is shown in the right figure of the array. 64 BL × 2 WL cells share the same well.

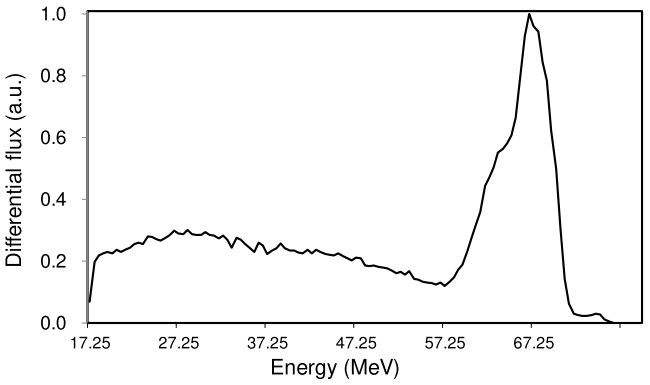

Fig. 3. Energy spectrum of quasi-monoenergetic neutron source generated by 70-MeV proton beam at CYRIC.

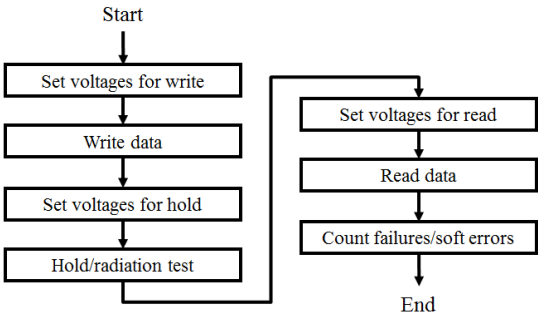

Fig. 2. Test flow. The holding time is much longer than others, and then, this test can be regarded as a static test.

Gasiot *et al.* [11] report that the deep N-well option enhances the parasitic bipolar action (PBA) and makes MCUs of large multiplicities (e.g., 16-bit MCU) in the cells containing nMOS transistors in the same P-well occur more easily compared to those without N-deep well. In our chips, 64 bitline (BL) × 2 word line (WL) cells share the same well.

Fig. 2 shows the common measurement flow in the irradiation tests using neutron and muon sources. We conducted static tests with a hold time of 600 s for spallation neutron and muon tests and 300 s for quasi-monoenergetic neutron test. The operating voltages during the processes of holding and writing/reading data were different. For keeping the values stored in SRAM cells unchanged after the voltage transition, the voltage transition proceeded slowly, which costs an extra time of at most 16 s. Even in this case, the holding time is much longer than others, and then, this test can be regarded as a static test. On the other hand, when the operating voltage for holding is very low, some cells cannot hold their stored values. We regarded these bits as failure bits and excluded them before the experiments.

The experiment of spallation neutron was conducted at the Research Center of Nuclear Center (RCNP) at Osaka University [12], which is included in JEDEC JESD89A [13] as one of the available white neutron sources and can provide up to 397.5-MeV neutrons. The beam was given perpendicularly from the resin side of two devices under test (DUTs) boards in series simultaneously, each of which has 16 bulk SRAM chips. Two operating voltages of 0.4 and 1.0 V were tested, and some results of this test were reported in [14].

Quasi-monoenergetic neutron test was conducted at the Cyclotron and Radioisotope Center (CYRIC) at Tohoku University [15]. The neutron beam is produced by 70-MeV proton source, and it has a flux peak at the energy near 70 MeV. Fig. 3 shows the energy spectrum of neutrons. The DUT board is the same with the one used in the experiment at RCNP, and one DUT board was tested at operating voltages from 0.4 to 1.2 V. The beam was injected from the printed circuit board (PCB) side perpendicularly.

Negative muon source at the Material and Life Science Facility (MLF) [16] of Japan Proton Accelerator Research Complex (J-PARC) was utilized for the muon irradiation experiment. The DUT board used in the other two neutron experiments above was irradiated. The beam was given from the PCB side perpendicularly. We scanned the energy to identify the energy at which negative muons stop near transistors inside the chips and the muon-induced SEU cross section becomes the maximum. After the energy scanning, the muon source of 6.6 MeV was selected for other tests. The range of operating voltage is 0.4–1.2 V. The spectrum of muons at this peak energy has a normal distribution with a 5% standard deviation [17]. The details for this experiment including energy scanning are found in [7]. It should be noted that positive muon-induced MCUs are negligible and hence are not discussed in this paper.

We define two cross sections: the first one is based on the number of error bits, which is hereafter called bit cross section, and the latter is based on the number of events and called the event cross section.

III. Similarity of Voltage Dependency and MCU Patterns

A. Voltage Dependency of SEU Cross Section

Fig. 4 shows the operating voltage dependency of SEU bit cross section induced by spallation neutrons, quasi-monoenergetic neutrons, and monoenergetic negative muons. The minimum energy of neutrons for the calculation of

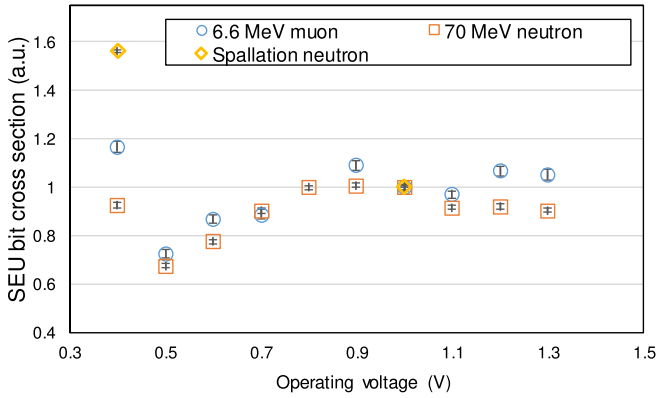

Fig. 4. SEU bit cross sections normalized by the cross section at 1.0 V for each beam. The cross section reaches the minimum at 0.5 V for negative muons and quasi-monoenergetic neutrons.

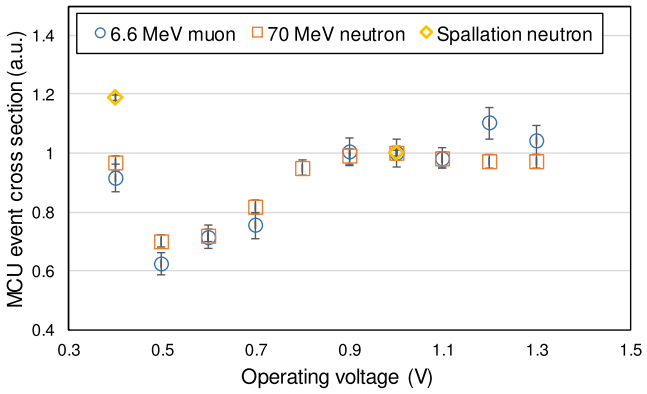

Fig. 5. MCU event cross sections normalized by that at 1.0 V for each beam.

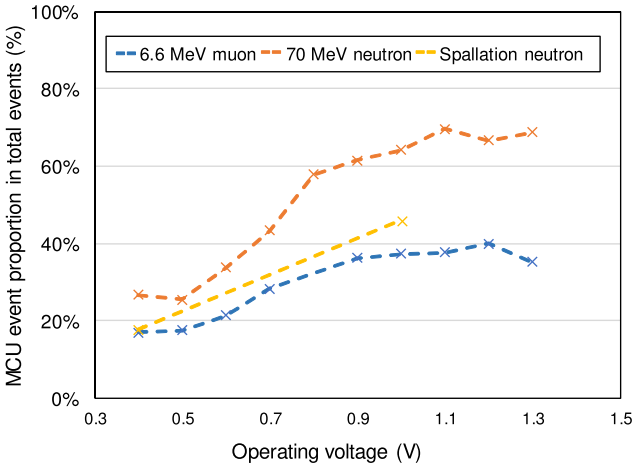

Fig. 6. Ratio of MCU events to total SEU events.

the cross section is 10 MeV for both spallation and quasi-monoenergetic neutrons, which is applied throughout this paper. The error bar represents one standard deviation. Here, we use the arbitrary unit with normalization to discuss the similarity in this paper. For the absolute values of the same device for SER calculation, Manabe *et al.* [18] conclude that the muon-induced cross section at the terrestrial spectrum is two to three orders less than that induced by terrestrial neutrons in the open air, whereas the contribution of muon increases to 13% in a building due to a stronger attenuation for neutrons compared to muons.

We can see that the voltage dependency of the SEU bit cross section is almost identical for quasi-monoenergetic neutrons and negative muons. These SEU cross sections reach the minimum at an operating voltage of 0.5 V and increase similarly to a saturated value with operating voltage rising. The reason accounting for this trend could be attributed to the balance between the voltage dependencies of critical charge and PBA, which was investigated in [7] for this device. For the comparison between spallation and quasi-monoenergetic neutrons, the cross sections at 0.4 V are different, which might originate from the difference in MCU cross section discussed in Section III-B.

B. Voltage Dependency of MCU Cross Section

Fig. 5 shows the operating voltage dependency of MCU event cross section with an error bar of one standard deviation, where the MCU event cross section is normalized by that at 1.0 V for each beam. The figure shows that the voltage dependencies of MCU event cross sections for quasi-monoenergetic neutrons and negative muons are well correlated and the cross sections reach the minimum at 0.5 V, which is similar to the SEU bit cross sections. On the other hand, the MCU event cross section induced by spallation neutrons at 0.4 V is higher than the others, which is similar to the SEU bit cross section and will be further discussed later.

Fig. 6 shows the ratio of MCU events to total SEU events. The MCU ratio follows an increasing trend according to the operating voltage for all the beams. On the other hand, for explaining the reason why quasi-monoenergetic neutron always has the highest MCU ratio among the three sources, a further investigation that takes into account the difference in the energy spectrum is necessary.

Here, let us clarify the reliability of the data set of MCU cross sections. For this purpose, the following discusses the maximum percentage of 2-bit pseudo-MCUs, which is referred to here as the adjacent upsets that are induced by multiple particles. The probability of SBU is calculated as

$$P_{\mathrm{SBU}} = \frac{N_{\mathrm{SBU}}}{N_{\mathrm{TotalBits}}} \tag{1}$$

where N_{SBU} represents the number of SBUs in a period of irradiation, and $N_{\mathrm{TotalBits}}$ stands for the total number of bits under test. Here, we consider all the upsets as SBUs to maximize P_{SBU} and, consequently, the probability of pseudo-MCU. Then, the probability of 2-bit pseudo-MCU is calculated as follows:

$$P_{\mathrm{pseudoMCU}} = {}_8C_1 \cdot P_{\mathrm{SBU}}^2 \tag{2}$$

where ${}_8C_1 = 8$ stands for eight possible positions next to the bit cell of interest in either horizontal, vertical, or diagonal direction. The maximum number of MCUs is calculated as the

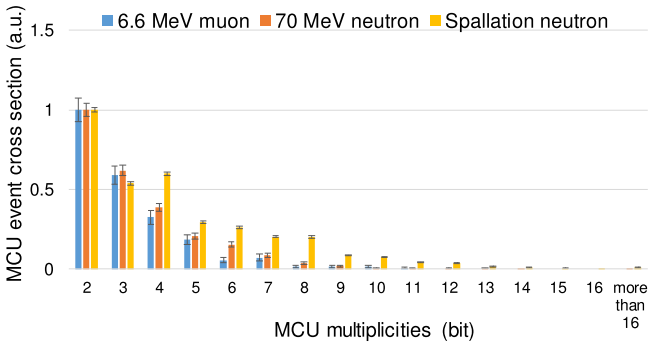

Fig. 7. MCU event cross sections at 0.4 V as a function of MCU multiplicity. The cross section is normalized by that of 2-bit MCU for each beam.

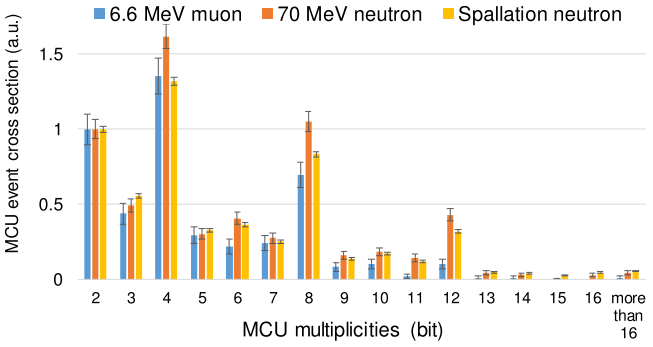

Fig. 8. MCU event cross sections at 1.0 V as a function of MCU multiplicity. The cross section is normalized by that of 2-bit MCU for each beam.

product of $N_{\text{TotalBits}}$ and $P_{\text{pseudoMCU}}$, and then, the maximum percentage of pseudo MCU over the number of measured MCUs N_{MCU} is

$$\frac{N_{\text{TotalBits}} \cdot P_{\text{pseudoMCU}}}{N_{\text{MCU}}}. \tag{3}$$

The calculated percentages of pseudo 2-bit MCU at 0.4 V are 0.1%, 0.2%, and 0.6% for the experiments using negative muons, quasi-monoenergetic neutrons, and spallation neutrons, respectively, while the percentages at 1.0 V are 0.1%, 0.3%, and 0.3% for the experiments using negative muons, quasi-monoenergetic neutrons, and spallation neutrons, respectively. We thus conclude that the observed MCUs can be regarded as true MCUs.

C. MCU Multiplicities

We next evaluate the distribution of MCU multiplicities, which significantly affects the performance of ECC. Figs. 7 and 8 show the MCU event cross sections at 0.4 and 1.0 V, respectively, as a function of MCU multiplicity. The MCU event cross section is normalized by that of 2 bit for each beam at each operating voltage. The voltages of 0.4 and 1.0 V are selected because the spallation neutron data are only available at these voltages.

We observe a common global trend in neutron- and negative muon-induced MCUs that the cross section becomes smaller as the number of MCU bits increases, while the cross sections

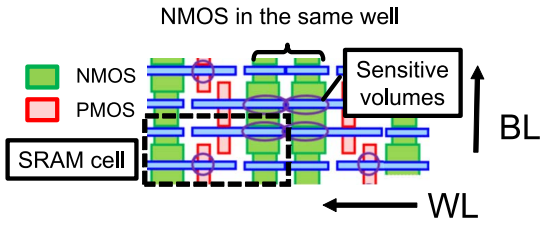

Fig. 9. Locations of SVs in 2 × 2 SRAM cells.

of 4-, 8-, and 12-bit MCUs are relatively higher than those of neighbors. This tendency can be explained in the locations of sensitive volumes (SVs) in 2 × 2 SRAM cells shown in Fig. 9. For each 2 × 2 SRAM cells, four SVs are located closely. When PBA is provoked, such four cells tend to upset for the same event. At 1.0 V, PBA occurs more frequently compared to 0.4 V operation, and hence, the peaks of 4-, 8-, and 12-bit MCU are more significant at 1.0 V. On the other hand, at 0.4 V, charge sharing causes MCU, which is suggested by a fact that the cross section of 2-bit MCU is the highest in Fig. 7.

Another key observation is that negative muons induce less large-bit MCUs than neutrons both at 0.4 and 1.0 V. Negative muons can deposit charge large enough to trigger PBA, but it seems that it is less probable to deposit large charge that can cause the MCUs of more than 12 bits. This tendency can be clearer at 0.4 V since larger charge is necessary to trigger PBA at lower operating voltage. The difference between spallation neutrons up to 392- and 70-MeV quasi-monoenergetic neutrons at 0.4 V is thought to be explained similarly. We will investigate the distribution of deposited charge with the Monte Carlo simulation to support the measurement results.

D. MCU Spatial Pattern

We finally investigate MCU spatial patterns. Fig. 10 shows the top four MCU spatial patterns observed for each beam at each operating voltage. We can see that at a high operating voltage of 1.0 V, 2 × 2 SRAM cells next to each other tend to upset simultaneously. This tendency, as we discussed in Section III-C, can be explained in the locations of SVs in 2 × 2 SRAM cells shown in Fig. 9. On the other hand, within the top four frequency MCU patterns, three out of the four muon-induced MCU patterns are the same with those of neutron-induced patterns. Also, their proportions to all the MCU events are similar. This result also suggests a similarity between neutron- and muon-induced MCUs. A distinct difference is that large-bit MCUs, such as 12 bits and larger, are scarcely caused by negative muons, whereas they are provoked by neutrons, especially spallation neutrons.

Also, we categorize the MCUs according to the width and the number of the upsets in BL and WL to compare the potential multiple bit upset (MBU) induced by negative muons and neutrons. Referring to the MCU pattern classification in [19] and counting the upset numbers along the same WL, we define the MCU pattern as

$$\text{TYPE\_}N_1\text{\_}N_2\text{\_}N_3 \tag{4}$$

TABLE I

MCU PATTERN CLASSIFICATION. PERCENTAGE OF EACH PATTERN IS CALCULATED AS # OF CORRESPONDING MCU EVENTS DIVIDED BY THE TOTAL # OF MCU EVENTS. "–" INDICATES NO SUCH MCUS WERE OBSERVED IN THE EXPERIMENTS, WHILE "0.0%" STANDS FOR THE PERCENTAGE LOWER THAN 0.05%

		b (%)	w (%)			c (%)				
		b_x_1_1	w_1_2_2	w_1_3_3	w_1_4_4	c_x_x_1	c_x_x_2	c_x_x_3	c_x_x_4	c_x_x_5
0.4 V	6.6 MeV Muon	22.1	16.0	–	–	10.6	51.1	0.2	–	–
	70 MeV Neutron	21.9	14.0	–	–	10.5	53.5	0.1	–	–
	Spallation Neutron	16.0	10.4	0.0	0.0	6.1	66.9	0.3	0.2	0.1
1.0 V	6.6 MeV Muon	14.9	8.0	–	–	1.1	76.0	–	–	–
	70 MeV Neutron	13.2	4.5	–	–	1.2	81.1	–	–	–
	Spallation Neutron	15.7	3.6	–	–	2.0	78.6	0.1	0.0	–

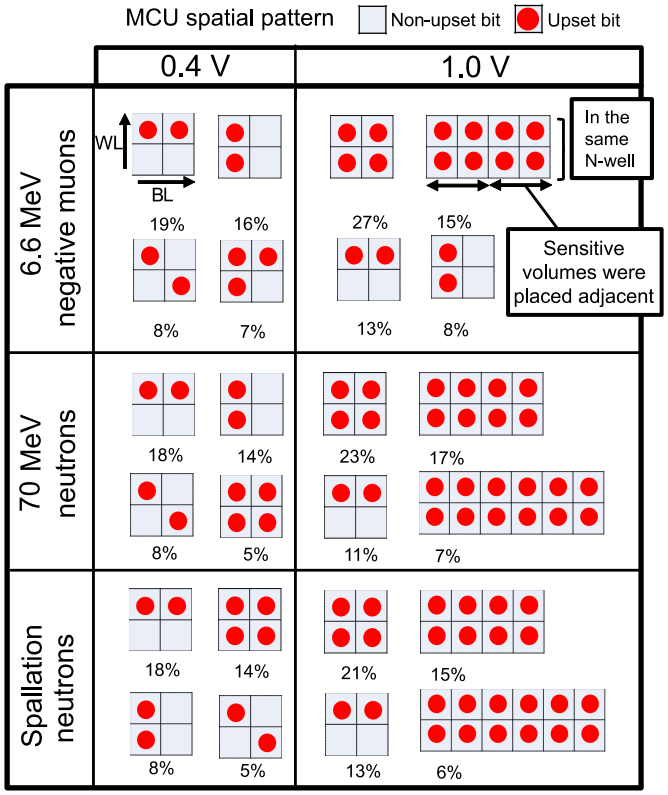

Fig. 10. MCU patterns in bitmaps. The top four patterns with their proportions to the total MCU events are illustrated.

where TYPE is the category consisting of b/w/c. Here, categories b, w, and c stand for a single line along BL, a single line along WL, and cluster, where cluster represents an MCU that has two or more bits along with both BL and WL directions. N_1 is the width in the BL direction, N_2 is the width in the WL direction, and N_3 is the maximum upset number along the same WL in a single MCU event. Any MCU with $N_3 \geq 2$ is an MBU in the SRAM without interleaving.

Table I gives the result. We can see that the proportions of errors along BL are larger than those along WL and they are close for negative muons and neutrons. The cluster type of MCUs achieving the largest proportion, which is c_x_x_2, is also the same, and this proportion increases as the operating voltage arises. As for the potential MBU, we find 2-bit errors along the WL account for more than 65% (w_1_2_2 + c_x_x_2) for both negative muon- and neutron-induced MCUs at either voltage. This result means that, for terrestrial MBU mitigation, 2-bit MBU should be considered with higher priority. On the other hand, at a low operating voltage, spallation neutrons induce 4- or 5-bit MBUs with a proportion of around 0.3%, and larger-scale interleaving is necessary to eliminate these MBUs.

IV. DISCUSSION ON SIMILARITY WITH DEPOSITED CHARGE

We showed the similarity of negative muon- and neutron-induced MCUs regarding voltage dependency of cross sections and spatial patterns. To further understand the similarity, we investigate the amount of charge that negative muons and neutrons deposit and discuss the relationship between the simulated deposited charge and the measured results.

A. Accumulated Deposited Charge for Muons and Neutrons

We conducted a Monte Carlo simulation with Particle and Heavy Ion (HI) Transport code Systems (PHITS) to estimate the deposited charges. For this simulation, we reproduced the experimental setups for each beam as 3-D models for PHITS similar to that in [7]. We selected the SV including the depletion region and calculated the charge deposited in the SV, where the locations of SV are consistent with the SRAM layout shown in Fig. 9 and the SV depth is 400 nm similar to the previous work [7]. Here, we focus on PBA-induced MCUs referring to Osada *et al.* [20] show that the charge deposited in a single SV has the positive relationship with the number of cells flipped in an MCU event. In the design with 32 cells sharing the same well/substrate, the maximum number of upsets due to PBA could reach 5 bits in 0.13-μm technology node [20]. With the same layout style and well tap placement strategy but technology scaling down to 65 nm with deep N-well option, which enhances the PBA [11], we think it is probable that more bits are flipped by the PBA in our 65-nm SRAM. Therefore, the amount of charge deposited in a single SV is utilized for discussion instead of the number of SVs that receive the charge larger than critical charge via charge sharing and hitting multiple SVs.

The source of 6.6-MeV negative muons and 70-MeV quasi-monoenergetic and spallation neutrons with the same spectra

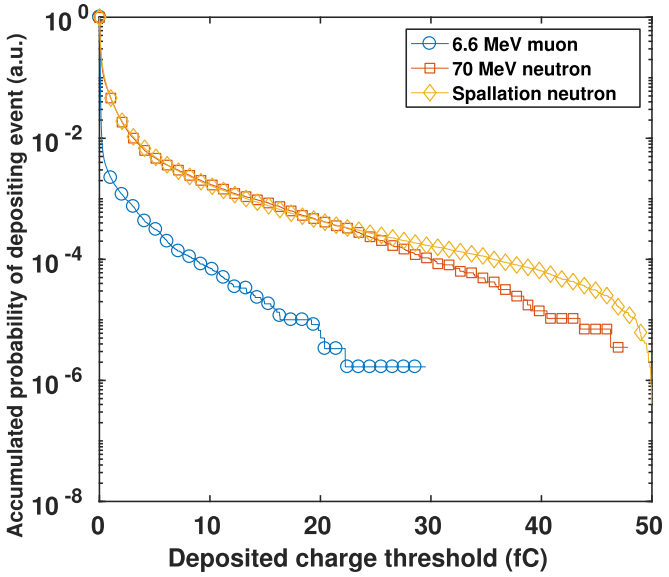

Fig. 11. Accumulated probability of the event as a function of charge threshold. In this evaluation, only the events that deposit nonzero charge in the SV are considered for probability calculation.

as those in the beam facilities are utilized to reproduce the experiments in the simulation. For each source, more than 1×10^9 of particles were injected.

Fig. 11 shows $P_{\mathrm{ac}}(C_{\mathrm{dep}})$, which is the accumulated probability of the events that deposit charge larger than C_{dep}. Here, only the events that deposit nonzero charge are considered, and then, most of the injected neutrons are not counted for this evaluation since neutron has a low probability of nuclear reaction. On the other hand, the proportion of the low-deposit events is larger for muons due to the direct ionization effect of negative muon itself and the decay electrons.

In Fig. 11, we observe that muons deposit less charge than neutrons, and the maximum charge in our simulation setup is around 30 fC for muons and 50 fC for neutrons. This observation is qualitatively consistent with our measurement result that the multiplicity of muon-induced MCUs is smaller than that of neutron-induced MCUs due to smaller charge leading to less upset bits in MCU [20]. It should be noted that, due to the definition of $P_{\mathrm{ac}}(C_{\mathrm{dep}})$ explained above, the absolute values of cross sections at the same C_{dep} cannot be compared directly.

For the comparison between quasi-monoenergetic and spallation neutrons, we note that spallation neutrons deposit larger charge. The difference comes from the energy of neutrons and the incident side of the board. The influence of the incident side of the board is discussed in [21], and as a conclusion, the incident side at the experiment using spallation neutron, namely, from the resin side of the DUT boards, causes larger deposit, which is consistent with the observation in Fig. 11.

B. Verification of MCU Charge Threshold

In this section, we estimate the charge thresholds for MCUs of different multiplicities at 1.0 V using Fig. 11 and the measurement result of the spallation neutron beam. We then apply these thresholds to quasi-monoenergetic neutron and negative muon beams and validate the simulation models for secondary ion analysis in Section IV-C.

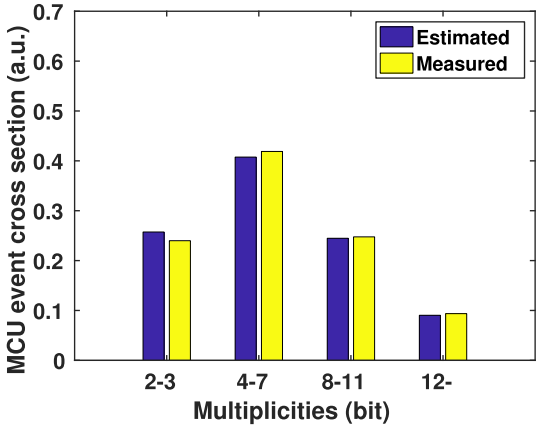

Fig. 12. MCU cross sections of 70-MeV quasi-monoenergetic neutrons at 1.0 V. The estimated cross section is obtained from Fig. 11, Table II, and (7).

A monotonic relationship between the amount of the charge in SV and the scales of MCU was shown in [20]. In [7], a linear relationship in the following was assumed to estimate MCU threshold:

$$\sigma_{N\text{-MCU}} = k_N P_{\mathrm{ac}}(C_N) \tag{5}$$

where $\sigma_{N\text{-MCU}}$ is the event cross section of MCU with multiplicities larger than N, k_N is a coefficient, and MCU threshold C_N is the parameter to be estimated. Here, $\sigma_{N\text{-MCU}}$ is available with the irradiation experiment and $P_{\mathrm{ac}}(C_{\mathrm{dep}})$ can be prepared with the simulation. However, there are two unknown parameters of k_N and C_N. To solve the two unknown parameter, we need to prepare two different data. In [7], we have several data sets of MCU cross sections and accumulated probability of depositing events that are obtained for different energies of muon beams. Suppose $\sigma^{(e1)}_{N\text{-MCU}}$, $\sigma^{(e2)}_{N\text{-MCU}}$, $P^{(e1)}_{\mathrm{ac}}(C_{\mathrm{dep}})$, and $P^{(e2)}_{\mathrm{ac}}(C_{\mathrm{dep}})$ are available for the momenta of $e1$ and $e2$. In this case, we can eliminate k_N from (5) as follows:

$$\frac{\sigma^{(e1)}_{N\text{-MCU}}}{\sigma^{(e2)}_{N\text{-MCU}}} = \frac{P^{(e1)}_{\mathrm{ac}}(C_N)}{P^{(e2)}_{\mathrm{ac}}(C_N)}. \tag{6}$$

By solving (6) with respect to $N = 2$, we can obtain C_2. In [7], we estimated C_2 from 6.5 to 7.6 fC at 0.9 V. The PBA threshold under 1.0 V is supposed to be lower than that of 0.9 V, and then, we adopted $C_2 = 6.5$ fC in this paper to calculate C_N for $N = 4, 8$, and 12 by

$$\frac{\sigma^{(\mathrm{SpallationNeutron})}_{2\text{-MCU}}}{\sigma^{(\mathrm{SpallationNeutron})}_{N\text{-MCU}}} = \frac{P^{(\mathrm{SpallationNeutron})}_{\mathrm{ac}}(C_2)}{P^{(\mathrm{SpallationNeutron})}_{\mathrm{ac}}(C_N)}. \tag{7}$$

By solving (7) with respect to C_N, we obtain C_N for MCUs with larger multiplicities and the result is given in Table II. From this table, we note that C_4 is larger than the estimate of 7.1–7.9 fC in [7]. A possible reason is the small statistic of large-bit MCUs observed in the experiments under the irradiation using 6.0- and 7.3-MeV muon beams. Next, we apply these thresholds to other two beams for estimating $\sigma_{N\text{-MCU}}$. The results are shown in Figs. 12 and 13. From

TABLE II
MCU THRESHOLD ESTIMATED FROM SPALLATION NEUTRONS AT 1.0 V

N	4	8	12
C_N(fC)	8.1	13.0	23.0

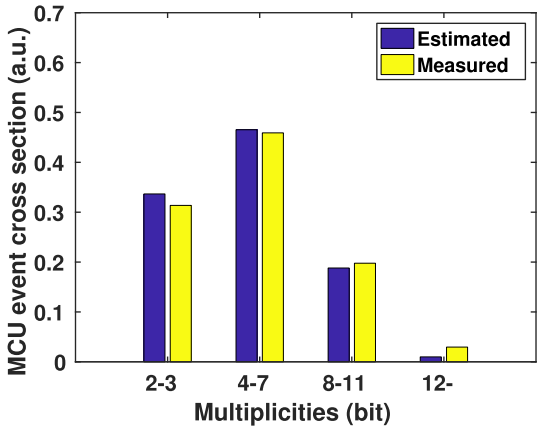

Fig. 13. MCU cross section of 6.6-MeV muon at 1.0 V. The estimated cross section is obtained from Fig. 11, Table II, and (7).

TABLE III
ENERGY AND LET RANGE OF SECONDARY IONS FOR NEUTRONS AND MUONS

Ions by 6.6 MeV muon	H	He	Mg	Al	Other HIs
Max energy (MeV)	47.0	33.0	4.0	2.0	11.5
Max LET (MeV/cm^2/mg)	0.5	1.4	9.4	6.6	8.4
Ions by 70 MeV neutron	H	He	O	Si	Other HIs
Max energy (MeV)	73.0	68.5	32.0	14.0	31.5
Max LET (MeV/cm^2/mg)	0.5	1.4	7.2	13.5	14.8
Ions by spallation neutron	H	He	O	Si	Other HIs
Max energy (MeV)	$>$100	$>$100	32.0	19.0	96.5
Max LET (MeV/cm^2/mg)	0.5	1.4	7.2	13.9	18.3

this figure, we confirm that the depositing event cross section and the MCU thresholds derived from spallation neutron beam reproduce the measured MCU cross sections of quasi-monoenergetic and negative muon beams. We consider the simulation setup is reasonable, and then, the deposited charge of secondary ions obtained in the simulation will be utilized for further similarity analysis.

C. Similarity in Deposited Charge of Secondary Ions

In the PHITS simulation, we dumped all the secondary ions generated in SV or passing through SV. The energy and linear energy transfer (LET) ranges are given in Table III. We observe that the maximum LET of secondary ions generated by neutrons is larger than that of muons. Although protons (H) and alpha particles (He) caused by neutrons have higher energy, this does not lead to higher LET or larger deposited charge because their LETs become maximum at the energy of around 0.5 MeV. On the other hand, neutrons, especially spallation neutrons generate HIs having higher LET. We replot the accumulated probability of depositing events by dividing them into nucleus as shown in Fig. 14. We can see that the HIs lead to the events of larger deposited charge for both

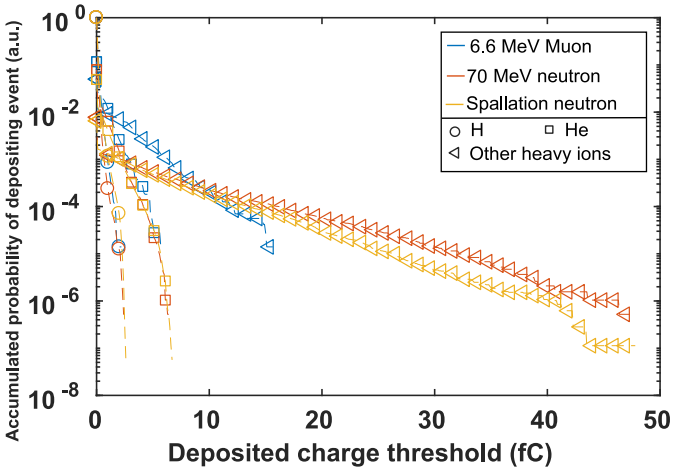

Fig. 14. Accumulated probability of the event with categorization into different nucleus. The ions of Mg, Al, O, and Si are included in HIs.

negative muons and neutrons. Despite this, the accumulated probability of depositing events of protons is almost identical to those of neutrons and negative muons. Similarly, those of alpha particles are close. The visible difference is that the nuclear reactions provoked by neutrons generate HIs with higher LET and consequently deposit larger charge.

V. CONCLUSION

In this paper, we compared the neutron- and negative muon-induced MCUs characteristics and examined their similarities. The voltage dependencies of MCU cross section are almost identical under irradiations of negative muons and neutrons. The analysis on multiplicities of MCUs indicates that both muons and neutrons have the ability to induce large-bit MCUs. On the other hand, neutrons induce larger bit (more than 12-bit) MCUs compared to negative muons, especially at high operating voltage, and consequently, larger scale interleaving is demanded for eliminating MBU with ECC. These observations are also supported by the deposited charge profiles obtained from Monte Carlo simulations.

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REFERENCES

[1] R. Silberberg, C. H. Tsao, and J. R. Letaw, "Neutron generated single-event upsets in the atmosphere," *IEEE Trans. Nucl. Sci.*, vol. NS-31, no. 6, pp. 1183–1185, Dec. 1984.

[2] B. D. Sierawski *et al.*, "Muon-induced single event upsets in deep-submicron technology," *IEEE Trans. Plasma Sci.*, vol. 57, no. 6, pp. 3273–3278, Dec. 2010.

[3] B. D. Sierawski *et al.*, "Bias dependence of muon-induced single event upsets in 28 nm static random access memories," in *Proc. IRPS*, Jun. 2014, pp. 2B.2.1–2B.2.5.

[4] N. Seifert, S. Jahinuzzaman, J. Velamala, and N. Patel, "Susceptibility of planar and 3D tri-gate technologies to muon-induced single event upsets," in *Proc. IRPS*, Apr. 2015, pp. 2C.1.1–2C.1.6.

[5] J. F. Dicello, "Microelectronics and microdosimetry," *Nucl. Instrum. Methods Phys. Res. B, Beam Interact. Mater. At.*, vols. 24–25, pp. 1044–1049, Apr. 1987.

[6] J. M. Trippe *et al.*, "Predicting muon-induced SEU rates for a 28-nm SRAM using protons and heavy ions to calibrate the sensitive volume model," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 2, pp. 712–718, Feb. 2018.

[7] W. Liao *et al.*, "Measurement and mechanism investigation of negative and positive muon-induced upsets in 65-nm Bulk SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1734–1741, Aug. 2018.

[8] S. Serre, S. Semikh, J. L. Autran, D. Munteanu, G. Gasiot, and P. Roche, "Effects of low energy muons on electronics: Physical insights and Geant4 simulation," in *Proc. Eur. Conf. RADECS*, Sep. 2012, pp. 1–7. [Online]. Available: http://www.im2np.fr/news/articles/RADECS2012_Muons_Proceedings.pdf

[9] A. Infantino, R. G. Alía, and M. Brugger, "Monte Carlo evaluation of single event effects in a deep-submicron bulk technology: Comparison between atmospheric and accelerator environment," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 596–604, Jan. 2017.

[10] P. Li Cavoli, G. Hubert, and J. Busto, "Study of atmospheric muon interactions in Si nanoscale devices," *J. Instrum.*, vol. 12, no. 12, Dec. 2017, Art. no. P12021.

[11] G. Gasiot, D. Giot, and P. Roche, "Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2468–2473, Dec. 2007.

[12] Y. Iwamoto *et al.*, "Evaluation of the white neutron beam spectrum for single-event effects testing at the RCNP cyclotron facility," *Nucl. Technol.*, vol. 173, no. 2, pp. 210–217, 2011.

[13] *Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray Induced Soft Errors in Semiconductor Devices*, JEDEC Standard JESD89A, 2001.

[14] S. Hirokawa, R. Harada, K. Sakuta, Y. Watanabe, and M. Hashimoto, "Multiple sensitive volume based soft error rate estimation with machine learning," in *Proc. 16th Eur. Conf. Radiat. Effects Compon. Syst. (RADECS)*, Sep. 2016, pp. 1–4, Paper H17.

[15] Y. Sakemi, M. Itoh, and T. Wakui, "High intensity fast neutron beam facility at CYRIC," *Int. Atomic Energy Agency*, vol. 46, no. 9, pp. 229–233, 2014.

[16] Y. Miyake *et al.*, "J-PARC muon source, MUSE," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 600, no. 1, pp. 22–24, Feb. 2009.

[17] Y. Miyake *et al.*, "Current status of the J-PARC muon facility, MUSE," *J. Phys., Conf. Ser.*, vol. 551, Dec. 2014, Art. no. 012061.

[18] S. Manabe, Y. Watanabe, W. Liao, M. Hashimoto, and S. Abe, "Estimation of muon-induced SEU rates for 65-nm bulk and UTBB-SOI SRAMs" presented at the 19th Eur. Conf. Radiat. Effects Compon. Syst., Gothenburg, Sweden, Sep. 2018.

[19] E. Ibe, H. Taniguchi, Y. Yahagi, K.-I. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1527–1538, Jul. 2010.

[20] K. Osada, K. Yamaguchi, Y. Saitoh, and T. Kawahara, "SRAM immunity to cosmic-ray-induced multierrors based on analysis of an induced parasitic bipolar effect," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 827–833, May 2004.

[21] S. Abe *et al.*, "Impact of irradiation side on neutron-induced single event upsets in 65-nm bulk SRAMs" presented at the 19th Eur. Conf. Radiat. Effects Compon. Syst., Gothenburg, Sweden, Sep. 2018.